A 100-kHz to 50-GHz Traveling-Wave Amplifier IC Module

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***Abstract*— Broad-band microwave packaging of a traveling-wave amplifier with an on-chip bandwidth of 2–50 GHz is described. Techniques to reduce overall insertion losses and to extend the low-frequency cutoff of the amplifier while maintaining gain-flatness are discussed. The packaged amplifier modules exhibit excellent performance from 100 kHz to 50 GHz. They are demonstrated as modulator drivers and receiver amplifiers in a 30-Gbit/s digital optical communication system.**

***Index Terms*—Coplanar waveguides, MMIC amplifiers, optical communication, packaging, traveling-wave amplifiers.**

I. Introduction

THE SPEED of optical fiber telecommunication systems based on electrical time division multiplexing has increased rapidly over the last decade. Systems operating at 10 Gbit/s are beginning to be deployed while the expected next generation of 40 Gbit/s-per-wavelength optical communication systems has already been demonstrated in various laboratory experiments [1], [2]. Baseband amplifiers used as modulator drivers, preamplifiers, and postamplifiers are key components for such high-speed systems. A linear response with little magnitude variation and a constant group delay over a broad bandwidth is essential for low bit error rates with long pattern lengths. Amplifiers with these characteristics have been demonstrated in various integrated circuit (IC) technologies (see for example [3]–[5]). The packaging of high-speed IC's is a real challenge since the overall package parasitics (the transmission line, discontinuities, wire bonds and lumped elements used in the module) become significant at high frequencies and can severely limit the performance of the broadband IC being packaged. Some very impressive high-speed modules have been demonstrated for in-house IC's either by optimizing the module for the given IC [6]–[8] or by designing the IC according to the known package parasitics [9], [10].

In this letter, we present the packaging of a commercially available traveling-wave amplifier that has an on-chip bandwidth of 2–50 GHz [11]. We describe packaging techniques on reducing the overall insertion losses as well as the design of the drain bias circuitry to extend the low-frequency cutoff of the amplifier down to 100 kHz while maintaining gain-flatness over a broad bandwidth. The packaged modules were used as modulator drivers and receiver amplifiers in a 30-Gbit/s optical transmission system [12].

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II. Amplifier Packaging

A. IC Characteristics

The frequency response for on-wafer measurements and other characteristics for the commercial amplifier are given in [11]. Bonding pads are provided to allow the amplifier to operate at frequencies lower than 2 GHz and to supply the drain and gate biases by means of external circuit components. However, since the output of the amplifier is directly connected to the drain bias pad, any parasitic coupling in the drain bias circuitry reflects as resonances and frequency response deterioration. In addition to these constraints, the input and the output of the amplifier need to be externally AC-coupled without introducing excess insertion loss.

B. Package Design

A coplanar waveguide (CPW) transmission line was chosen for the ease of providing a low-inductance ground between the chip and the surface ground of the substrate. A quartz substrate was used to minimize CPW radiation and skin losses since it has a low dielectric constant ($\varepsilon_r = 3.92$). In order to suppress cavity resonances and microstrip modes, the quartz substrate was suspended over an air gap with a microwave absorber. The 3350-μm-long identical substrates used at the input and the output of the amplifier were designed to have minimum insertion and return losses. Fig. 1 shows a photograph of the packaged IC.

An important package parasitic comes from the wire bond connection between the chip and the CPW transmission line, which introduces inductance for both the signal and the ground connections. It was shown in [9] that this parasitic could be reduced by designing the IC according to the outer bonding wire inductance. However, this technique is not possible for the packaging of a commercial IC; therefore, an optimization of this interconnection is required. We observed experimentally that gold ribbon with a width of 75 μm has less inductance than the conventionally used wire bonds. The bonding pads of the IC were aligned with the top surface of

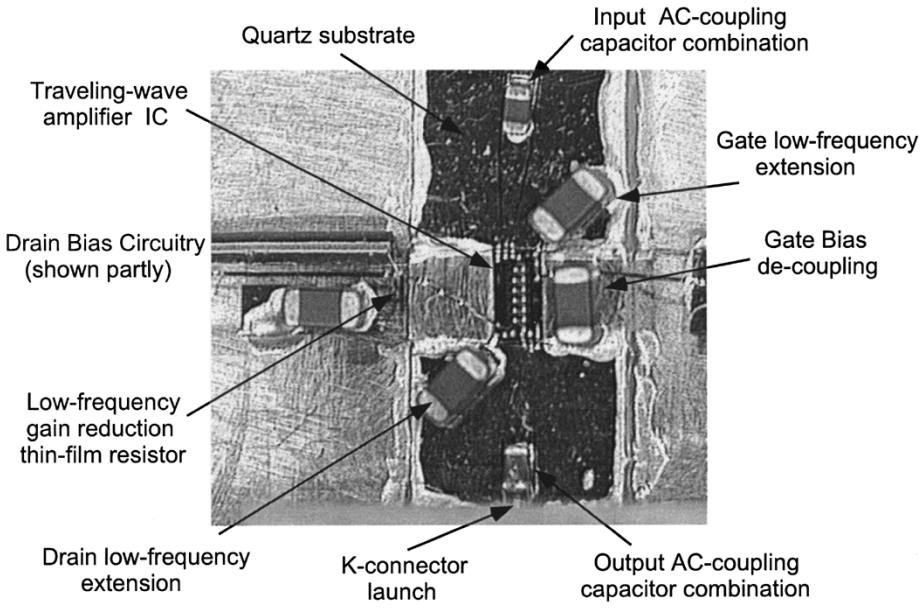


Fig. 1. Photograph of the packaged amplifier IC.

the substrate to minimize the length and the inductance of the ribbon. The length of the ribbons was approximately 150 μm long with an estimated inductance of less than 1 nH/mm.

The AC-coupling of the input and the output of the amplifier are conventionally achieved by mounting a surface mount dielectric (SMD) capacitor across a gap on the signal line. However, since broad-band (100 kHz to 50 GHz) SMD's are commercially unavailable, a parallel combination of a 180-pF dielectric capacitor (di-cap) and a 33-nF SMD was chosen [Fig. 2(a)]. In order to simulate the input and output substrates simultaneously, a pair of the capacitor combination was epoxied on a 7-mm-long CPW line. Frequency response measurements showed that there was about 2.4-dB extra insertion loss due to the two gaps and the capacitor combinations at 40 GHz. In order to eliminate the discontinuities on the CPW, the module was designed such that the capacitors would be placed directly under the K-connector launch [Fig. 2(b)]. This new design improved the insertion loss by 1 dB at 40 GHz and allowed for slightly shorter CPW lines.

A similar parallel configuration of capacitors was connected to the low-frequency extensions of the amplifier. The parasitics of the capacitors or the gold ribbon were not seen to be significant on the frequency response of the amplifier. However, at frequencies below 2 GHz, a gain rise was caused due to the increase in the drain termination resistor value from 50 to 65 Ω ([11, Fig. 1]). This is overcome in the drain bias circuitry as will be described in the following section.

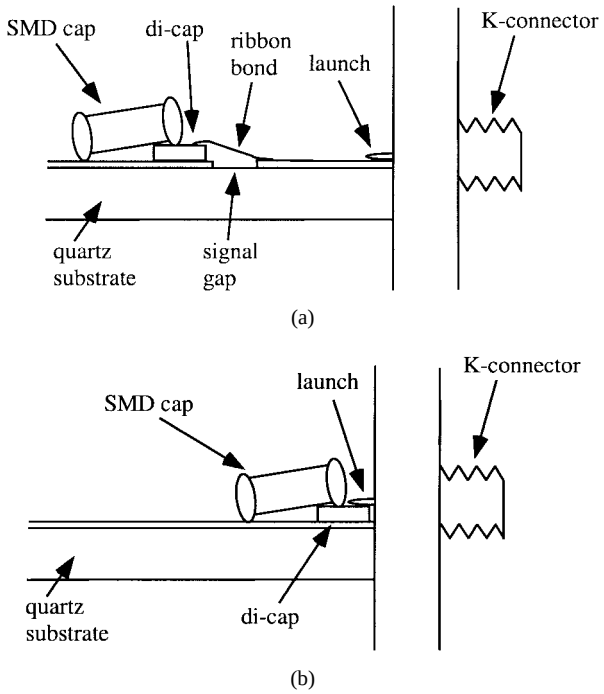


Fig. 2. Illustrative diagrams of different AC-coupling schemes: (a) capacitor combination mounted on the signal line next to a gap. Ribbon bonds are used to connect the capacitor and the signal line over the gap and (b) capacitor combination mounted under the K-connector launch, thereby eliminating the gap (signal line discontinuity) and the ribbon bonds.

III. Drain Bias Circuit Design

The challenge of the drain bias circuit design was to use commercial components (with limited bandwidth and uncertain parasitics) while also incorporating an external resistor to reduce the low-frequency gain; it was essential that the whole circuit looked like an open from the output pad up to 50 GHz. This design turned out to be the most crucial aspect of the package since any coupling of the parasitics resulted in huge resonances in the frequency response of the module. The circuit schematic that gave a consistent flat response for a broad bandwidth is shown in Fig. 3. The inductor/resistor combination L1/R1 through L4 ensures gain-flatness from 100 kHz to 2 GHz. It is significant to mention that the components were chosen by simulation to minimize any resonance between a pure inductor and the preceding parasitic capacitance. In order to minimize the coupling between the ribbon inductance (L6) and its preceding parasitic capacitance (which resonates strongly in the gigahertz range), an inductor

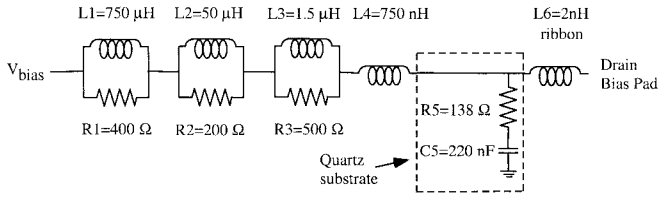


Fig. 3. The drain bias circuitry used for biasing the amplifier. R5 is the low-frequency gain reduction thin-film resistor patterned on a quartz substrate.

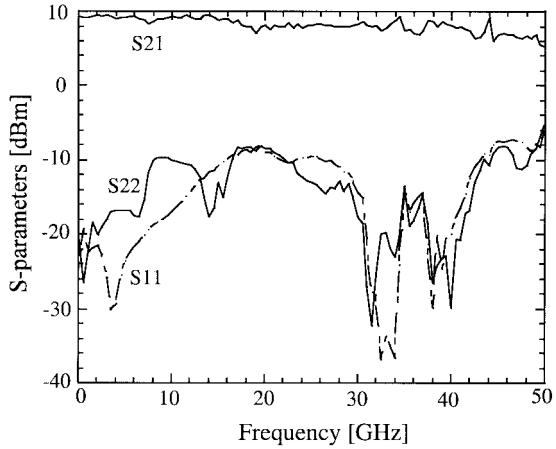
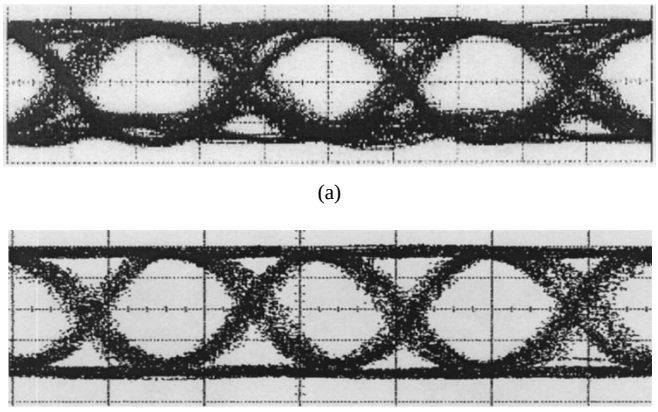


Fig. 4. Measured insertion and return losses of the amplifier module.



(a)

(b)

Fig. 5. The 30-Gbit/s transmission performance of three cascaded amplifier modules: (a) 30-Gbit/s NRZ input (H: 13 ps/div, V: 100 mV/div) and (b) 30-Gbit/s output from the amplifiers (H: 20 ps/div, V: 750 mV/div).

with a high self-resonating frequency and a thin-film resistor with minimal parasitics and a small bonding pad were used. The purpose of the R5 thin-film resistor was to reduce the low-frequency gain described in the preceding section. The ribbon length of 2.5 mm was very critical for the high-frequency (>2 GHz) response of the module. It was chosen to be long enough to act as a broadband high-frequency inductor, but short enough to shift the resonance due to the preceding parasitic capacitance out of the operational bandwidth.

IV. Performance of Packaged Amplifier

Fig. 4 shows the measured gain and return losses for the module. The gain is at an average of 8.5 dB with a gain-flatness within ±1.5 dB from 100 kHz to 50 GHz. The packaged amplifier's response is in good agreement with the chip performance with the exception of a resonance at 45 GHz and a deterioration of the return losses. The resonance around 45 GHz is due to the bandwidth limit of the K-connectors used, which will be improved by using V-connectors. We also believe that the return loss will be improved once broad-band capacitors for ac-coupling are available. The amplifier modules were used as modulator drivers and receiver postamplifiers in a 30-Gbit/s NRZ transmission experiment [12]. Fig. 5(a) shows the 30-Gbit/s input and (b) the 3 $V_{p\text{-}p}$ output of three cascaded amplifier modules. No significant degradation of the eye is observed. Bit error rate measurements confirmed this with error free operation for input signals above −22 dBm.

V. Conclusion

In summary, we presented the microwave packaging of a commercially available traveling-wave amplifier with an on-chip bandwidth of 2–50 GHz. By using techniques to reduce excess insertion loss and a careful design of the drain bias circuitry, a bandwidth of 100 kHz to 50 GHz was achieved. These amplifier modules are suitable for high bit-rate transmission systems, which was successfully demonstrated in a 30-Gbit/s transmission experiment.

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