III-V Based Heterostructure Integrated Thermionic Coolers

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ABSTRACT

Solid state coolers based on III-V material can be monolithically integrated with optoelectronic and high-speed electronics components. The use of thermionic emission in heterostructures will permit to enhance cooling capacities beyond linear transport regime. Monte Carlo calculations are used to study main energy relaxation mechanisms in III-V thin barrier heterostructures, i.e., polar optical phonon and intervalley scattering. The bias dependence of electron energy relaxation length is analyzed and important parameters for the design of heterostructure integrated thermionic (HIT) coolers are identified. Single-stage InGaAsP based HIT coolers have been fabricated and characterized. Cooling up to 0.7K over one micron thick barrier has been measured.

INTRODUCTION

Thermoelectric coolers are of increasing use with high power or low noise electronic and optoelectronic devices. Many high speed GaAs VLSI circuits or InP-based semiconductor lasers will benefit from integrated coolers based on III-V compounds. These coolers can also be fabricated in large quantities using mature integrated circuit fabrication techniques. Thermionic emission in heterostructures can be used as an additional mean to tailor thermal and electrical properties of devices beyond what is achieved with conventional Peltier coolers [1,2]. In a heterostructure integrated thermionic (HIT) refrigerator, selective emission of hot carriers over a barrier layer from the cathode to the anode will cool down the emitter junction.

HIT COOLING

The overall cooling capacity of a single barrier HIT cooler, with cathode side barrier height of ϕ_C, barrier thickness d and its thermal conductivity β, can be expressed as

$$Q_{TI} = \left[\Phi_C + 2\frac{k_B T_C}{e}\right]\cdot I - IV\left[\left(\frac{1}{2}-\frac{\lambda_E}{d}\right)-\frac{{\lambda_E}^2}{d^2}\left(e^{-d/\lambda_E}-1\right)\right]-\frac{\beta}{d}\Delta T$$

where k_B is the Boltzmann constant, e the electric charge, T_C the cold side (cathode) temperature, and $\Delta T=T_H-T_C$. λ_E is the energy relaxation length for carriers [2]. The dependence on electrical conductivity of the barrier (carrier mobility) is hidden in the I(V) relationship [2].

This energy balance equation has three terms that describe thermionic cooling at the cathode, "Joule" heating in the barrier and heat conduction from the hot to the cold side. Thermionic cooling is equal to average energy of emitted electrons time the current. Assuming Boltzmann distribution for carriers, which is valid for barrier heights > $2k_BT$, this average energy is $(\phi_C+2k_BT_C/e)$. The Joule heating term is IV times a coefficient, which takes into account the finite electronic energy relaxation length λ_E. In the limit of very thick devices, this coefficient reduces to 1/2 which is the result for pure diffusive transport. In the other limit of very short devices, the Joule heating term vanishes. In this case of ballistic transport, all of the electron's energy is deposited at the anode side.

MAJOR ENERGY RELAXATION MECHANISMS

In order to optimize HIT cooling devices, it is important to minimize Joule heating in the barrier. It is thus necessary to understand what are the main mechanisms that determine electronic energy relaxation length (λ_E) in semiconductors. For this purpose we will use Monte Carlo simulations of electron transport in GaAs. Other III-V semiconductors such as InP have similar characteristics. Ternary and quartenary compounds have in addition alloy scattering, but this is not expected to change energy relaxation considerably.

Fig. 1 displays the Joule heating as a function of distance for 5000 electrons injected over a 0.1 eV barrier into a 3-micron thick GaAs layer. The energy deposited is averaged over 50nm intervals.

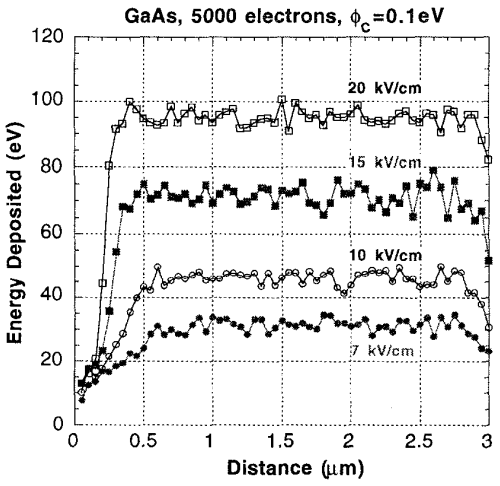

Fig.1 Joule heating generated in the barrier as a function of distance for different values of applied electric field.

It can be seen that, depending on applied electric field, it will take 0.2 to 1 micron before electrons reach equilibrium and lose energy equal to what they gain at steady state from the external electric field. In the first order of approximation, the curves in Fig. 1 can be fitted by an exponential expression that includes energy relaxation length λ_E:

$$\frac{dQ_{Joule}}{dx} = I\frac{V}{d}\left(1 - e^{-x/\lambda_E}\right)$$

Fig. 2 displays the electric field dependence of electron energy relaxation length in GaAs, deduced from Monte Carlo results. It is interesting to notice that λ_E has a maximum value of about 0.3 micron at 6 kV/cm.

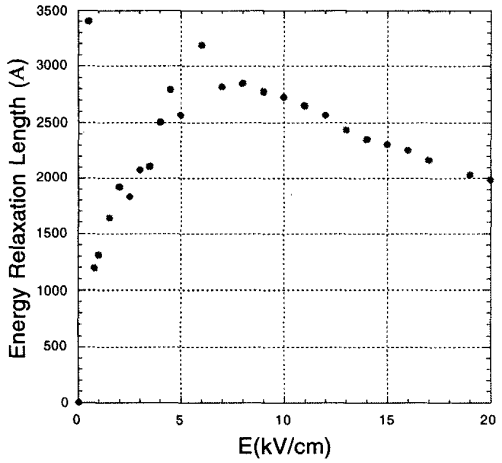

Fig.2 The electric field dependence of electron energy relaxation length in GaAs.

In order to understand why λ_E has a peak, the microscopic origin of carrier energy relaxation has to be studied. Fig. 3 displays the contribution of major scattering processes to electron energy relaxation as a function of distance for an electric field of 5 kV/cm. It can be seen that major scattering events responsible for energy relaxation at short distances (< 0.5μm) are polar optical phonon emission and absorption in the Gamma valley. At longer distances, there is a substantial population in the L valley. In this case, L-valley polar optical phonon emission and absorption and inter L-valley scatterings will start to contribute to the electronic energy loss mechanisms. In this respect, the form of λ_E versus electric field is very similar to velocity versus electric field that is manifested through negative differential resistance and Gunn effect in bulk GaAs [3].

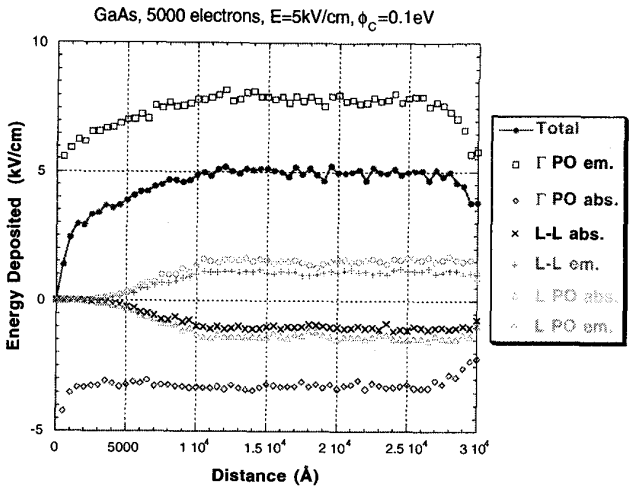

Fig.3 Monte Carlo simulation of various energy loss mechanisms in a thin barrier heterostructure device.

Fig. 4 displays the rate of energy relaxation due to polar optical phonon interaction as a function of electron's energy. Below the threshold to emit an optical phonon ($\hbar\omega_{POP}$=36 meV for GaAs), electrons have almost a constant rate to absorb energy from the phonons. For electrons that have energy bigger than $\hbar\omega_{POP}$, the emission of polar optical phonons is a major relaxation mechanism. However, one should notice that the rate of phonon emission reaches a maximum for electrons with energy equal to 2 or 3 times $\hbar\omega_{POP}$, and for higher energies this rate is rapidly decreasing. Thus, as long as intervalley scattering do not occur, under higher electric fields electrons will travel further before they thermalize.

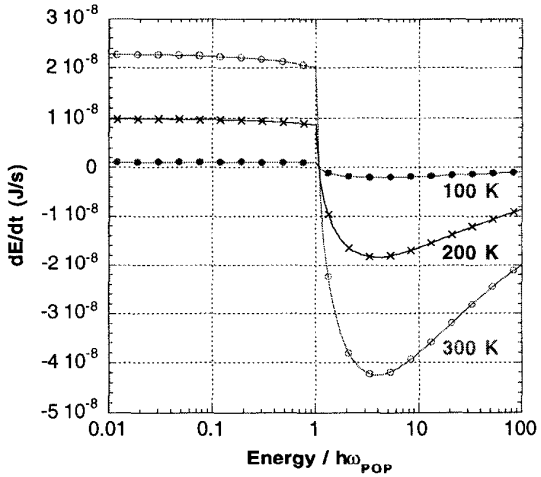

Fig.4 Energy relaxation rate due to polar optical phonon emission and absorption.

InGaAsP BASED HIT COOLERS

In order to investigate experimentally thermionic emission cooling in heterostructures, a single InGaAsP barrier (λ_{gap}=1.3 μm) surrounded by n^+ InGaAs cathode and anode layers was grown using metal organic vapor phase epitaxy (MOCVD). Cathode and anode layer thickness were 0.3 and 0.5 μm and the barrier thickness was one micron. 1.5 μm tall, 100x200 μm^2 mesas were etched down using dry etching techniques. Ni/AuGe/Ni/Au was used for top and bottom contact metallization. Fig. 5 displays the temperature on top and on the bottom of the device as well as the substrate temperature far away form the device as a function of current. All temperatures are relative to the value at zero current. We can see that despite poor performance of InP substrate as a heat sink, a net cooling of ~0.1K is observed on top of the device. Taking the literature value for thermal conductivity of the barrier material, 4-5 W/mK, the measured electron mobility of 3000 cm^2/Vsec and other material parameters of InGaAsP, we expect up to 3-4 degrees of cooling. One of the main reasons for poor performance is the Joule heating in the wirebonds connected to the top of the device, and also heat conduction from package to the cold junciton through these wirebonds. In order to minimize the effect of series and contact resistances, a number of p- and n-type HIT coolers connected electrically in series and thermally in parallel should be used (similar to conventional thermoelectric cooling modules).

Even though the absolute cooling temperature is dominated by non ideal effects, one can study the effect of different barrier structures using similar substrates and packaging. Fig. 6 shows the cooling $|T_C-T_H|$ for two samples with identical

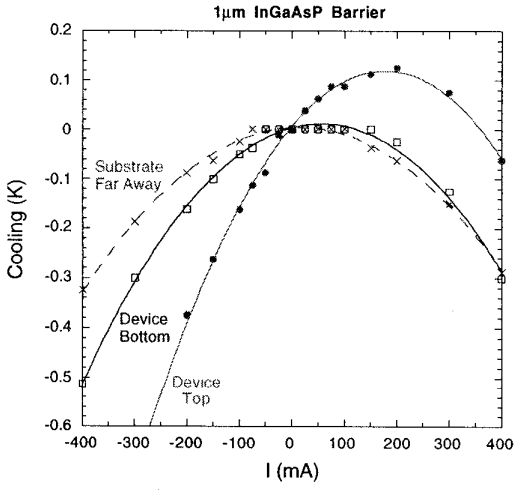

Fig.5 Temperature on top and on the bottom of the device as well as the substrate temperature far away form the device as a function of current. All temperatures are relative to the value at zero current. The device is a single-stage HIT cooler with bulk InGaAsP (λ_{gap}=1.3 μm) barrier layer.

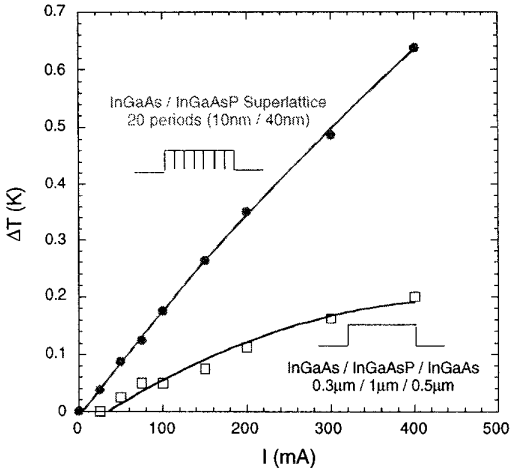

Fig.6 Experimental $|T_C-T_H|$ versus current for 100x200 μm^2 single-stage HIT coolers with bulk InGaAsP (λ_{gap}=1.3 μm) barrier and with superlattice barrier (20 periods of 10nm InGaAs and 40nm InGaAsP).

cathode and anode InGaAs layers and different barrier compositions. One can see that the superlattice sample has a superior cooling performance. This is due its increased thermal resistance as well as improved transport of hot carriers.

SUMMARY AND CONCLUSION

Major electronic relaxation mechanisms for carriers injected in thin barrier III-V semiconductors are analyzed. The energy relaxation length is determined by polar optical phonon emission at small fields, and by intervalley scattering at large fields. There is a maximum in thermalization distance at intermediate fields that can be exploited to improve the performance of heterostructure integrated thermionic coolers. Finally, cooling up to 0.7K over one micron thick barrier has been measured in InGaAsP-based HIT coolers.

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