Terman’s method was used to evaluate the density of interface states in the MIS structures by calculating the difference in the slope between the experimental and theoretical surface potential-voltage dependencies. The analysis showed a low minimal interface state density \( D_{i,s} \) of \( 1 \times 10^{11} \text{cm}^{-2} \text{eV}^{-1} \) in the AlN/GaN MIS structure. The interface state density was found to decrease when the surface potential varies from \( E_2 \) to 1 eV below the conduction band edge. The increase of the interface state density for energies below \( E_2 \) is attributed to measurement errors due to increased MIS leakage. The studies reported in this Letter show that good interface properties can be obtained from AlN/GaN heterostructures.

![Graph showing C-V characteristics of AlN/GaN MIS structures.](image)

**Fig. 3** C-V characteristics of AlN/GaN MIS used to evaluate interface density of states of AlN/GaN heterojunction.

- measured
- calculated

In summary, AlN/GaN heterostructures using thin epitaxially grown AlN barrier layers have been investigated for the purpose of developing III-V-based MISFETs. C-V characterisation and Terman’s method were used to demonstrate a low interface state density of the AlN/GaN interface. The high quality of the interface is confirmed by very high values of transconductance and current density obtained from HFETs fabricated on the AlN/GaN layers. These results indicate a high potential of AlN/GaN MISFETs for microwave power applications.

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References


SiGe micro-cooler

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Thin film SiGe heterostructure coolers have been fabricated and characterised. Cooling by as much as 1 K at room temperature and 1.6 K at a substrate temperature of 70°C over a 3mm SiGe superlattice barrier has been measured. This corresponds to cooling power densities of hundreds of watts per square centimeter.

Increased demand in the optical communications industry has led to many advances in semiconductor laser sources. These sources are efficient and operate at low threshold currents. As a result, heat dissipation is low (hundreds of milliwatts) and temperature dependent parameters can be stabilised with little cooling (<20°C). Still, the low heat dissipation in conjunction with very small surface area (hundreds of square micrometers) results in a high heat flux density. Recent work on the miniaturisation of thermoelectric coolers (TECs), has shown the advantages of smaller coolers in these applications [1]. Thin film thermoelectric coolers that can be monolithically integrated with high speed, high power electronic and optoelectronic devices can improve the performance of these devices.

SiGe is a good thermoelectric material for high temperature applications [2]. It has been used for thermo-nuclear power generation in satellites for deep space missions. In this Letter we will describe the fabrication and characterisation of single-element thin film superlattice SiGe/Si coolers used for room temperature applications. Superlattice structures can enhance the cooler performance by reducing the thermal conductivity between the hot and cold junction [3], and by selective emission of heat carriers above the barrier layers [4].

The sample was grown in a Perkin-Elmer Si molecular beam epitaxy (MBE) growth chamber on a 125 mm diameter, (001)-oriented Si substrate, doped to 0.007–0.020Ωcm with Sb.

The structure of the sample consisted of a 3μm thick SiGe/Si superlattice grown symmetrically strained on a buffer layer designed so that the in-plane lattice constant was approximately that of relaxed SiGe/Si. The buffer sequence, superlattice, and surrounding layers were doped to \( \sim 2 \times 10^{16} \text{cm}^{-3} \) by first pre-doping a 1/2 monolayer (ML) of Sb and then growing the various layers at a temperature of \( \sim 390°C \). A supplemental Sb flux was provided at a cell temperature of 408°C throughout the growth in order to replenish the surface Sb concentration.

**Fig. 1** Schematic diagram of SiGe thin film cooler

For the relaxed buffer layer, we used a 10 layer structure, alternating between 150 nm \( \text{Si}_x\text{Ge}_{1-x} \) and 50 nm \( \text{Si}_{0.76}\text{Ge}_{0.24}\text{C}_{0.05} \). Anneals were performed at 750°C for 10 min after the growth of each \( \text{Si}_x\text{Ge}_{1-x} \) layer, so that complete relaxation was obtained. Following the method of Ostrem et al. [2], the \( \text{Si}_{0.76}\text{Ge}_{0.24}\text{C}_{0.05} \) layers were used to drive the dislocations into the Si substrate.
Fig. 2 SEM image of processed SiGe micro-cooler devices

Fig. 3 Cooling measured on top of thin film SiGe/Si cooler and on substrate

Devices were tested from room temperature up to 70°C. Large devices (150 × 150 μm²) were measured directly with probes, and small devices were mounted in packages and wire-bonded.

Fig. 4 Measured cooling at various substrate (heat sink) temperatures

SiGe micro-coolers were fabricated and cooled up to 1.6K has been measured. Joule heating in the wirebonds connected to the cold junction, as well as the large thermal resistance of the substrate, are the major factors that hamper the device performance. Methods for improving the properties of these micro-coolers are now under consideration.

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References


