Heterogeneous Integrated Circuits for On-Chip Interconnection

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Abstract
This talk reviews recent advances on chip level interconnections and low cost heterogeneous integrated photonics circuits for high speed optical links. We review recent breakthroughs in silicon photonic technology and components and describe progress in silicon photonic integrated circuits.

1. Introduction

Photonics interconnects are a promising solution for future chip-level communication due to its high capacity I/O, large bandwidth and low power consumption. One approach is the heterogeneous silicon photonics platform,which has been intensively investigated since its first demonstration in 2006. Its key advantages include the compatibility between the design experience with functional materials including III-V system as well as the large volume CMOS fabrication technology, silicon-on-insulator (SOI) substrate. Fig. 1 shows the evolution of PIC complexity, comparing heterogeneous integrated circuits compared with InP platform and silicon photonics without integrated lasers. The rapid development of integration level and multi-functionality is evident [1]. Heterogeneous silicon integration has applications and advantages for inter-chip and on-chip photonics interconnection due to its compatibility with Si substrate and CMOS technology. In this talk we review the recent progress on components and circuits on the heterogeneous integrated platform used for photonics interconnection on chip.

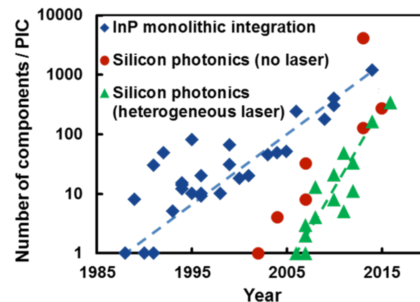

Fig. 1 Evolution of PIC integration level: Number of photonic components integrated on a single waveguide on InP or silicon substrates.

2. Heterogeneous integrated circuits

In order to satisfy the demand of chip level interconnection for high bandwidth density and low power consumption, an on-chip light source is preferred to minimize the energy loss during coupling from off chip. Multiple on-chip laser formats have been demonstrated on the heterogeneous integrated platform. Here we compare two integration methods: direct epitaxial growth and the molecular bonding method. Epitaxial growth can reduce cost by eliminating the expensive III-V substrate by utilizing large and low cost silicon wafer, however, the lifetime is not yet adequate. In contrast, the low temperature bonding technique has excellent reliability and is more flexible in combining materials and processes. Fig.2 (a) shows the molecular beam epitaxial method to grow InAs quantum dots (QDs) on silicon substrate. A ridge laser with InAs QDs active region shows low threshold current density, large output power and high operation temperature up to 119 °C [2]. Fig. 2 (b)-(d) shows results of heterogeneous silicon lasers with gain materials transferred to SOI substrate by wafer bonding. One drawback of SOI wafers is the thick buried oxide layer that blocks the heat generated in active devices from dissipating into the substrate. The micro-ring lasers with 50 μm diameter, shown in Fig. 2 (b), used a novel thermal shunt as alternative thermal path between device core and heat sink, with over 30% improvement on thermal impedance and maximum lasing temperature [3].

Wavelength division multiplexing (WDM) is widely used in long-haul communication. It's also attractive in chip-level interconnection due to its large capacity within restricted electro-optical interface. On-chip lasers with tuning ability is preferred in WDM systems to align the lasing wavelength to the WDM channels. Fig. 2 (c) shows monolithically-integrated tunable laser using ring reflectors. Over 54 nm in O band tuning was achieved with the Vernier effect by thermally tuning two ring mirrors. The best lasing linewidth was around 50 kHz with the

enhancement of negative feedback from the ~4 cm integrated cavity, which makes it also attractive for coherent communication systems [4]. The downside of the tunable laser is the power consumption that goes into thermal tuner of rings. Short cavity distributed feedback (DFB) lasers on Si shown in Fig. 2 (d) have low threshold currents (< 10 mA) with maximum output power of more than 5 mW in the C band. Less than 20 mW electrical input power is needed for 1 mW optical output corresponding to less than 1 pJ/bit power consumption at 25 Gbps channel transmission rate.

Fig. 3 shows more building blocks for an on-chip WDM communication system. As illustrated in Fig. 3 (a), a ring-based magneto-optic isolator was designed based on magnetic Ce:YIG bonded on a SOI substrate. The magnetic field is applied to the micro-ring by current in the metal micro-strip above the Ce:YIG layer and leads to resonant peak splits between clockwise and counter clockwise transmission [5]. A record 32 dB of isolation near 1550 nm was achieved with only 2.3 dB excess loss. Fig. 3 (b) shows a 1×8 array waveguide grating (AWG) which can be used as (de)multiplexer or router in a WDM system. With appropriate design, the AWG has footprint around 1.1×1.1 mm^2 with total insertion loss around 2 dB. The cross-talk between channels is as low as -28 dB.

An electro-absorption modulator (EAM) was adopted on our platform due to its small footprint, wide optical bandwidth as well as low power consumption. With multiple die bonding technique, III-V materials with different band-gaps were integrated to one SOI substrate for laser, modulator and photodetector. As shown in Fig. 3 (c), the heterogeneous EAM with 100 μm cavity length had an extinction ratio larger than 6 dB for 1 V voltage swing with the optical bandwidth over 20 nm in C band. We have worked with Oracle to integrate the photonics chip with an electrical driving chip, as shown in Fig. 3 (d). The silicon photonics transmitter chip was integrated with a low power CMOS driver with a high-yield flip-chip bonding method [6]. The integrated EAM array had an open eye at 12.5 Gbps with 3.5 dB extinction ratio at 1510 nm, with a maximum driving voltage swing from zero to 2.4 V.

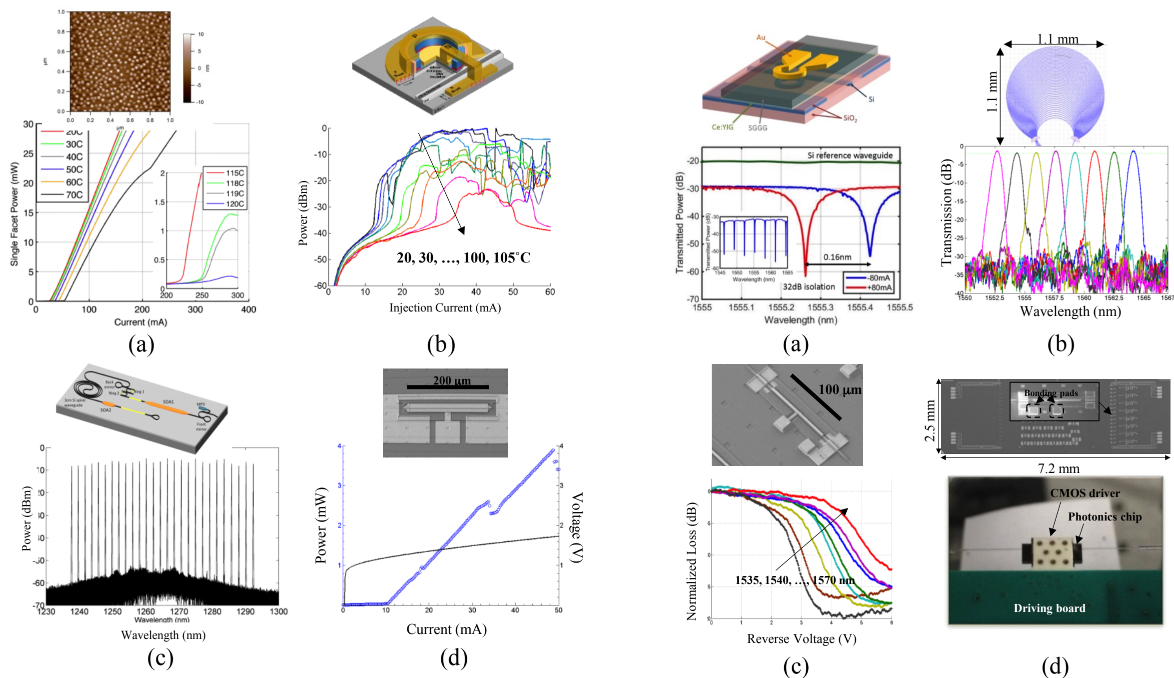

Fig. 2 Heterogeneous integrated lasers with (a) epitaxial grown InAs QDs on Si; (b) ring based Vernier tunable laser with silicon external cavity; (c) micro-ring lasers with thermal shunt and (d) short cavity DFB lasers on Si.

Fig. 3 Heterogeneous integrated components with (a) Ce:YIG isolator on SOI; (b) low loss AWG; (c) EA modulator integrated with 100 μm active length and (d) integrated EAM array with CMOS driver.

3. Summary

We reviewed the recent progress on the heterogeneous integration platform for on-chip interconnection, including breakthrough results for tunable and low power laser, ring isolator, low loss AWG, and integrated transmitter circuit.

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