Evolution of Photonic Integrated Circuits

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Abstract: Photonic Integrated Circuits (PICs) are evolving rapidly for applications from interconnects to sensors. We present the evolution of four different platforms for photonic integration: pure III-V/InP, pure SOI (monolithic silicon photonics), III-V heterogeneously integrated on SOI (heterogeneous integration), and III-V epitaxially grown on silicon. Presently, thousands of optical devices are integrated into PICs to achieve multiterabit per second transceivers, LIDARs, and chemical sensors.

Photonic integrated circuits (PICs) are currently fueling high bandwidth density interconnection links, and are primed to serve other growth markets such as LIDAR and chip-scale wearable sensors. Various material platforms for photonic integration exist, each with their own unique advantages and shortcomings. Four different approaches are differentiated among these based on potential to deliver high performance with a monolithically integrated solution combining both active and passive functionalities, and the ability to scale at low cost with the expected growth of the overall photonic integrated circuit market: 1) pure III-V (InP), 2) silicon on insulator (SOI), 3) heterogeneous integration of III-V on SOI and 4) epitaxial growth of III-V on silicon. The level of integration (e.g. number of devices integrated onto one waveguide) for the first three approaches that has been demonstrated to date is summarized in Fig. 1. In the sections below, a brief description of each of the four approaches is given, along with some prominent commercial examples where applicable.

1) III-V/InP generic integration

Photonic integration on InP, whereby InP and related ternary or quaternary epitaxial stacks are grown on a common InP substrate for the subsequent fabrication of optoelectronic devices, provides a platform for complete monolithic integration of passive and active functions [1]. Active and passive interfaces are joined via vertical twin or single guide growths, quantum well intermixing, and/or butt-joint regrowth [1]. The most prominent foundry example is the joint European platform for InP-based components and circuits - JePPIX – which offers foundry services through Oclaro, the Fraunhofer Heinrich Hertz Institut (HHI) in Berlin, and the COBRA spinoff company SMART Photonics, located in Eindhoven. Infinera, Finisar, Lumentum and others all offer products based on InP PICs.

2) Monolithic silicon photonics (with Ge/Si laser or no integrated laser)

Silicon-on-insulator is the natural platform for mainstream silicon photonics, whereby the majority of optical functions are derived from devices constructed from the silicon device layer, while selective area epitaxy of germanium is used for photodetection. Many foundries today offer a relatively complete suite of technologies based on this platform including AIM Photonics, IMEC, Global Foundries, ST Microelectronics, among others. However, an integrated laser is missing from these processes. Commercial products based on this process have been released by companies such as Acacia, Luxtera, Cisco, and PETRA, whereby an external III-V laser is coupled to the silicon photonic chip as the light source. Epitaxial growth of Ge-Si on Si for an integrated laser is not technically viable since the threshold currents are more than 1000x higher than the other three approaches, and low power is a key requirement for most datacom and telecom applications.

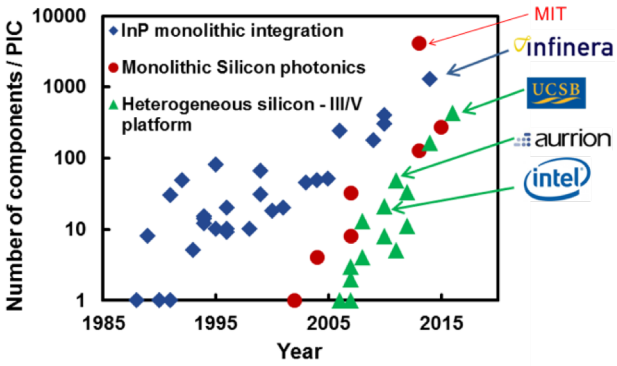

Fig. 1. Photonic Moore's Law

3) Heterogeneous Integration on SOI

Heterogeneous integration takes advantage of the silicon based processing in a monolithic silicon photonics process, but also utilizes III-V materials for some active optical functionalities such as gain, photodetection, and phase/amplitude modulation [2].

As an added benefit, integration of multiple epitaxial materials on a single PIC connected by a common Si waveguide is possible. A number of foundries such as CEA-LETI, IMEC and IME are currently exploring this process. Intel has recently released products formed by this technology, while Juniper Networks (Aurrion) and HPE are actively investing in the technology as well.

4) III-V epitaxially grown on silicon

The potentially lowest cost approach is to combine III-V with silicon via epitaxial growth, eliminating the need for III-V substrates altogether and taking advantage of the processing, testing, and packaging equipment for 300 mm substrates. There are two potential variations of this approach for the fabrication of PICs. One option is to couple light generated in a III-V section to passive photonic circuitry in silicon on an SOI substrate, which has been proposed previously [3]. The two disadvantages of this approach are the increased thermal resistance of the SOI substrate and coupling from the laser to the SOI waveguide through a relatively thick III-V base layer that is needed for defect reduction. Here, focus is given to an alternative approach where the entire PIC is fabricated from epitaxially deposited III-V layers, as is done in the case of integration on InP, but with the difference being the III-V layers are grown on a much cheaper and larger silicon substrate. Multiple bandgaps may be obtained from selective area growth, regrowth steps or intermixing as is done in the case of InP. This process is an active area of research both within academia as well as commercially by AIM, IMEC, and NTT, among others. In particular, many traditional CMOS foundries are exploring epitaxial growth of III-V on silicon as a "More-than-Moore" technology to extend the performance scaling of transistors past gate length scaling limits, and there is synergy in leveraging the same technology for photonics.

An important technological differentiator is the performance of the light source and how it is integrated[4-7]. Coupling losses can significantly reduce the efficiency of the overall circuit and limit performance scaling [5]. Off-chip coupling of an external laser for monolithic silicon photonics typically results in 2-8 dB of coupling losses (including coupling from the laser to fiber and fiber to SOI). Integrated laser transitions can have much lower losses through proper butt-joint regrowth (0.1 dB) or well-designed taper transitions (0.2-0.5 dB). Semiconductor lasers from epitaxial III-V lasers on silicon are already showing reasonable performance, with additional room for improvement as this scheme provides the best natural heat-sinking for the laser.

Epitaxial growth of III-V on silicon stands to become a competitive solution as it is potentially the lowest cost solution and able to match or exceed the performance of the other approaches. While a fully functional PIC has not yet been demonstrated on this platform as most research efforts have gone towards engineering discrete devices, many building blocks are currently being set in place. Recent work on quantum dot lasers epitaxially grown on silicon have shown excellent performance with much improved lifetimes over previous iterations of epitaxial lasers on silicon [3, 8-9]; however, commercially acceptable lifetimes have not yet been demonstrated. Recently, several demonstrations of similar lasers grown on on-axis (001) CMOS compatible silicon substrates with no germanium or offcut have been reported [10-11]; and epitaxially grown photodetectors on silicon have been demonstrated with good performance [12]. Under the American Institute for Manufacturing (AIM) Integrated Photonics, work is on-going to develop modulators as well as photodetectors from III-V materials epitaxially grown on silicon, improve laser performance on this platform, transfer the growth processes to 300 mm wafers, and accumulate data for a process design kit (PDK).

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