A Tunable Hybrid III-V-on-Si MOS Microring Resonator with Negligible Tuning Power Consumption

Di Liang[1*], Geza Kurczveil[1], Marco Fiorentino[1], Sudharsanan Srinivasan[2], John E. Bowers[2], Raymond G. Beausoleil[1]

1. Hewlett Packard Labs, Hewlett Packard Enterprise, Palo Alto, CA 94304, USA
2. Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106, USA
**di.liang@hpe.com*

Abstract: We demonstrate a novel hybrid microring resonator with an integrated III-V-on-Si metal-oxide-semiconductor (MOS) capacitor structure for essentially zero-power resonance tuning. Over **1,000,000,000** times better tuning efficiency than conventional thermal tuning approach has been achieved.

OCIS codes: (140.4780) Optical resonators; (140.3945) Microcavities

1. Introduction

Power consumption is a primary physical and practical obstacle in conventional metal interconnect to keep Moore's Law valid in complimentary metal-oxide semiconductor (CMOS) circuits, and photonic interconnects are being heavily researched and invested in world-wide effort to decrease input-output (IO) power consumption and increase capacity. High-performance photonic interconnect systems such as the HP Corona architecture [1] employ thousands of optical microring resonators in lasers, modulators, switches, DEMUX, etc. [1] A microring resonator is attractive for its compactness and extremely low operational power consumption, is of great use for wavelength selection and data modulation [2]. However, slight dimensional variations and environmental changes can result in microring resonance shifts from the design target. Thermal tuning is the conventional method for resonance tuning. The typical tuning power efficiency is in the μW/GHz (mW/nm) regime [3], and can easily dwarf the power consumption for carrier-injection or depletion modulation thus impacting the overall advantage of microrings.

Carrier injection and depletion with the associated free-carrier plasma dispersion effect can also be used for resonance tuning. Carrier injection is always accompanied by joule heating in the PIN diode which offsets the plasma effect. Carrier depletion results in higher background/insertion loss. A metal-oxide-semiconductor (MOS) capacitor can also generate this plasma effect in a waveguide. High-speed modulators based on poly-Si/gate oxide/crystalline-Si MOS structures have been demonstrated [4, 5]. In this work, for the first time to the best of our knowledge, we demonstrate a hybrid III-V-on-Si microring resonator with an integrated III-V-on-Si metal-oxide-semiconductor (MOS) capacitor, resulting in a power reduction by a factor of over a **billion**.

2. Device design

The hybrid MOS-type microring is based on the same integration approach as our hybrid Si microring lasers [6]: lighting-emitting III-V epitaxial layers (e.g. InP-based compound semiconductors) are transferred to a Si-on-insulator (SOI) substrate by a wafer bonding process [7]. As shown in a transmission-electron microscope (TEM) image in Fig. 1(a) [8], a bonding oxide interface layer forms as a result of either O_2 plasma-assisted bonding process itself [7] or intentional and controllable dielectric deposition [9]. The dielectric layer here, called gate oxide, along with the Si and III-V layers forms a MOS capacitor. The refractive index and free-carrier absorption loss in InP and Si materials change as a result of free carriers accumulating or depleting near the gate oxide under an external bias. Since minimal current penetrates through the gate oxide barrier and flows between anode and cathode under direct-current (DC) bias, it consumes zero DC power and has no device joule heating. Furthermore, compared with poly-Si

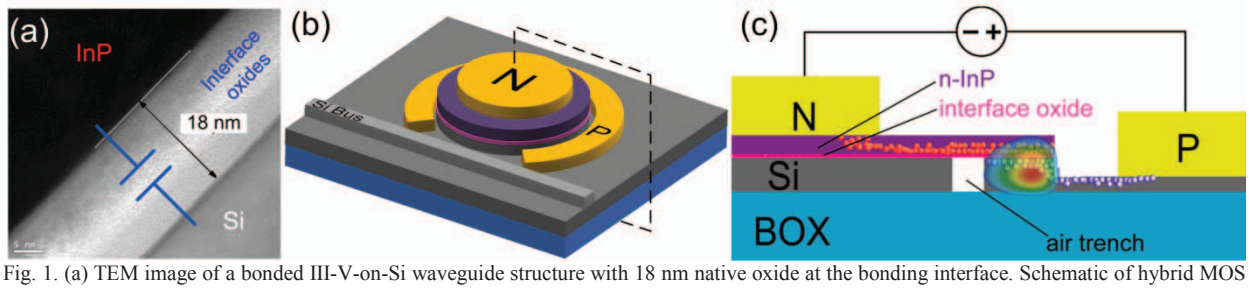

Fig. 1. (a) TEM image of a bonded III-V-on-Si waveguide structure with 18 nm native oxide at the bonding interface. Schematic of hybrid MOS Si microring resonator in (b) side-view and (c) cross-sectional view with simulated optical mode.

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in other MOS structure, the III-V layer in this hybrid case has lower material loss and better plasma dispersion effect for the same variation of free carrier concentration owing to its single-crystalline structure, and smaller electron and hole effective mass and higher mobility, respectively.

Figs. 1(b) and (c) show the device side-view and cross-sectional view schematic geometry, respectively. The electrodes are placed on n-type InP and p-type Si to apply electrical field across the gate oxide. The III-V epilayer stack on top of 250 nm-thick Si is 150 nm in total thickness including 2 periods of InP/InGaAsP superlattice close to the bonding interface. This epilayer design is the same we used for most of the devices in the hybrid Si platform [10, 11]. Therefore the material and fabrication cost impact of integrating MOS-type devices with hybrid Si lasers, photodetectors, etc. is negligible. Fig. 1(c) shows that the simulated optical fundamental mode overlaps the MOS capacitor region. An air trench is formed on the Si device layer prior to wafer bonding in order to confine the MOS capacitor region only to the fundamental mode of the hybrid microring resonator. With proper design, it also filters out the higher order transverse modes.

Fig. 2(a) shows simulated majority carrier concentration, i.e., free electron and hole in InP and Si, respectively, as a function of bias voltage. Due to the different doping levels (10^{18} cm^{-3} in III-V and 10^{16} cm^{-3} in Si), free carriers around the gate oxide (15 nm Al_2O_3 in this work) are depleted at zero bias indicated by the band diagram in Fig. 2(a) inset. As shown in Fig. 2(b), once forward bias is applied to p-Si the hybrid MOS capacitor operates in accumulation mode. The hole concentration at the oxide/Si interface increases by over 9 orders of magnitude at 1 V bias. Both hole and electron concentrations at the oxide/semiconductor interface reach 10^{20} cm^{-3} level at 8 V bias. Simulated 2D hole distribution profiles under 0, 4 and -4 V biases are shown in Fig. 2(c). Clearly air trench confines the carrier variation in the fundamental transverse mode region to effectively reduce the capacitor area, which potentially benefits the device high-speed performance. At -4 V reverse bias, hybrid MOS capacitor operates in carrier inversion mode, and plasma dispersion effect is a lot weaker than accumulation mode in this device design.

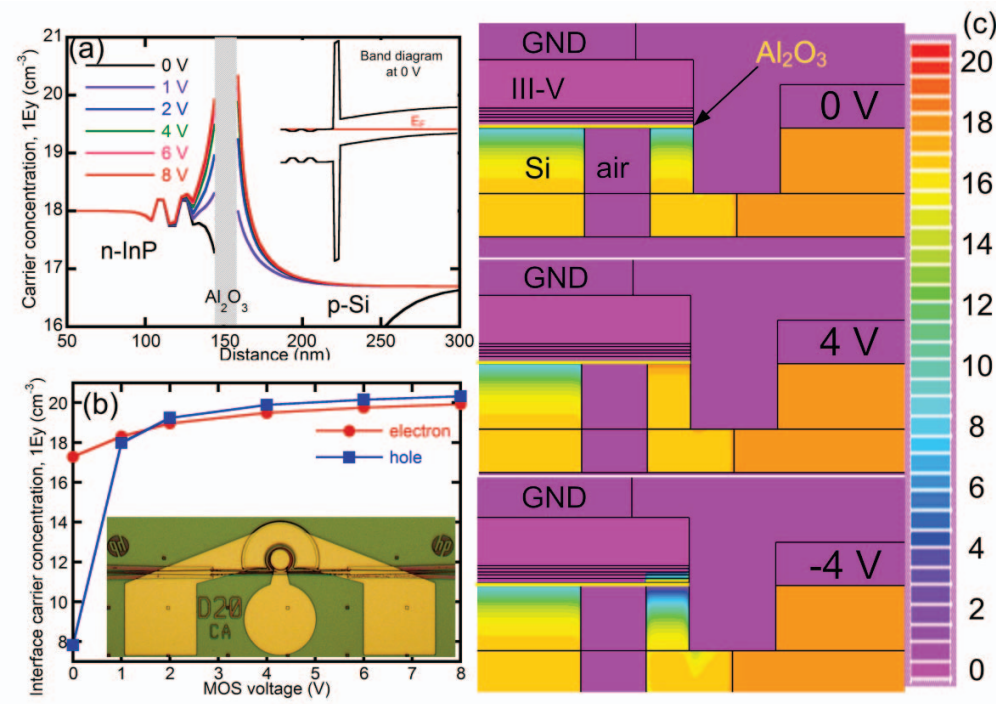

Fig. 2. (a) Simulated electron and hole concentration distribution in n-InP and p-Si as a function of bias voltage and band diagram at 0 V as inset, (b) and their concentration at the gate oxide interface vs. MOS bias voltage. Inset: a fabricated device microscopic image; (c) simulated 2D free hole concentration profile at 0, 4 and -4 V. Scale bar in (c) is in unit of 1×10^{x}.

3. Experiment and results

The microscopic image of a fabricated hybrid MOS microring (20 μm in diameter) resonator is shown in the inset of Fig. 2(b). Si grating couplers are used for optical signal input and output. Fig. 3 shows the resonance wavelength shift under (a) positive voltage and (b) negative voltage bias. As simulation indicates, microring resonance wavelength shifts towards shorter wavelength noticeably under the forward bias. This blue shift confirms its plasma dispersion effect rather than thermal effect which leads to red shift. A relative low quality factor Q ~ 2300 is measured due to rough sidewall-induced scattering loss and likely high bending loss from an unexpectedly shallow

Si etch in this batch of devices. Nevertheless, over 8 dB extinction ratio is achieved at 4 V bias. At biases ranging from 4 V to -4 V we measured extremely low leakage currents of 20-50 fA (limited by our instrument) using a high-resolution Keithley current meter. The wavelength shift of 0.055 nm/V under forward bias can be translated into a tuning power efficiency of 8 fW/GHz (assuming 35 fA average leakage current). This is 9 orders of magnitude better than conventional thermal tuning in μW/GHz regime [3]. For practical purposes the DC tuning power consumption can be neglected. This also allows a pre-set bias to be applied in order to enable resonance tuning to both shorter and longer wavelength. As expected, zero or little shift is observed within -4 V bias in Fig. 3(b). Typical capacitance-voltage (CV) characteristic of a test structure with much larger capacitor area is also measured at both low and high frequency in Fig. 3(c).

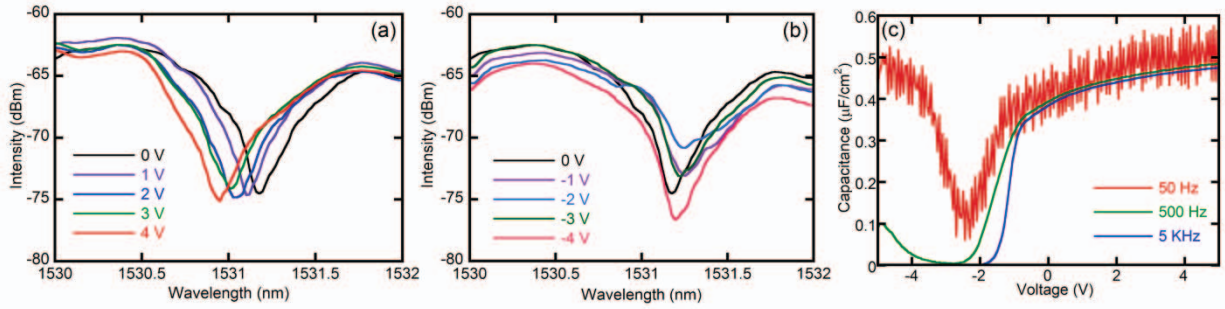

Fig. 3. Spectra of hybrid MOS microring modulator under (a) positive and (b) negative bias voltage; (c) low- and high-frequency CV characteristic of a hybrid MOS capacitor testing structure.

4. Summary and future work

We demonstrated a tunable microring resonator which is a hybrid III-V-on-Si waveguide in optical domain and simultaneously a hybrid MOS capacitor in electrical domain. A model was built to study this MOS capacitor's different operation regimes. This microring resonator under capacitor accumulation mode enables an ultra-low tuning power consumption of **9 orders** of magnitude lower than conventional thermal tuning. This is also the first experimental demonstration to actively utilize the electrical property of Si portion in this hybrid Si device platform.

We expect to achieve a larger tuning range and a better tuning efficiency by further optimizing the waveguide geometry and gate oxide properties. With improved dry etching technique and better process control, cavity loss and grating coupler loss can be reduced yielding lower insertion loss. Device dynamic properties will be presented in detail later. This device could be of great use in MUX/DEMUX, add/drop, switch and potentially high-speed modulation applications with attractive convenience to integrate with other hybrid photonic devices.

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