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Chapter 15
Silicon Lasers and Photonic Integrated Circuits

Sudharsanan Srinivasan, Alan Y. Liu, Di Liang, and John E. Bowers

Abstract This chapter discusses photonic integration on silicon from the material property, device as well as photonic circuit point of view. The progressive growth of silicon-based electronic integrated circuits (ICs) has followed Moore's Law and has been driven by the roadmap of conventional electronic ICs. Silicon is arguably the primary host material platform for future photonic integrated circuits (PICs) as well, particularly for applications beyond conventional fiber-optical telecommunications. Until recently, the lack of a laser source on silicon has been seen as the key hurdle limiting the usefulness and complexity of silicon photonic integrated circuits. In this chapter, we review the numerous efforts including bandgap engineering, Raman scattering, monolithic heteroepitaxy and hybrid integration to realize efficient light emission, amplification and lasing on silicon. The state-of-the-art integration technologies for narrow linewidth lasers and high-speed modulators are also discussed.

15.1 Silicon as a Platform for PICs

An integrated circuit (IC) is a miniaturized electronic circuit that consists of a large number of individual components, fabricated side-by-side on a common substrate

S. Srinivasan (✉)
Aurrion Inc., 6868, Cortona Drive, Suite C, Goleta, CA 93117, USA
e-mail: sudha.srinivasan@aurrion.com

A.Y. Liu
Materials Department, University of California, Santa Barbara, CA 93106, USA
e-mail: Alanyoungliu@gmail.com

D. Liang
Hewlett Packard Labs in Hewlett Packard Enterprise (HPE), 1501 Page Mill Road, MS 1123, Palo Alto, CA 94304, USA
e-mail: di.liang@hp.com

J.E. Bowers
Electrical and Computer Engineering Department, University of California, Santa Barbara, CA 93106, USA
e-mail: bowers@ece.ucsb.edu

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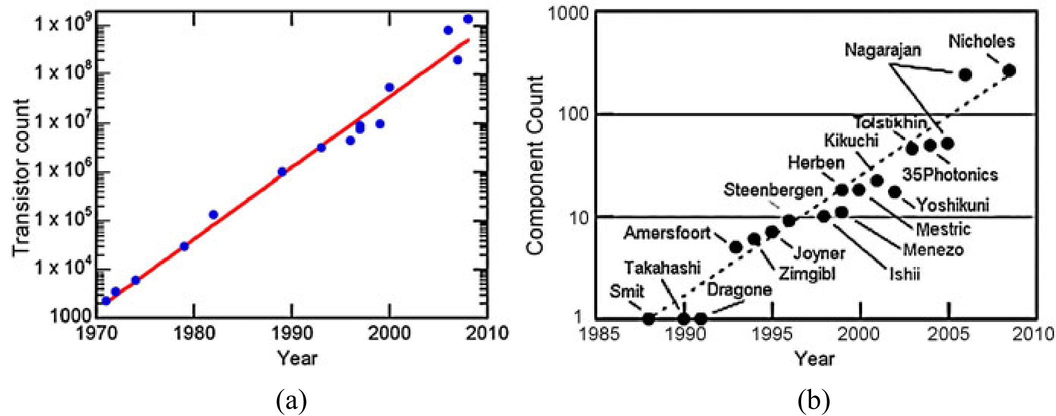

Fig. 15.1 (**a**) Electronic [1] and (**b**) Photonic integrated circuit evolution [5, 7]

and wired together to perform a particular task. In 1943, the first working transistor was demonstrated [1], and eleven years later, the invention of the IC began a new era. The inherent advantages in *cost and performance* have been the driving force in the IC industry since then. Moore's Law has set the progressive pace in these advances. Gordon Moore foresaw exponential growth, with the number of transistors on an IC doubling approximately every two years [2], as illustrated in Fig. 15.1(a). Large-scale integration and mass production also resulted in the enormous reduction of the chip size and system cost and tremendous improvement in performance and applications. The first UNIVAC computer in 1951 weighed 13 metric tons and occupied more than 35 m^2 of floor space with a clock speed of 2.25 MHz [3]. Sixty-five years later, a personal computer now easily delivers 1000$\times$ faster speed and is small and light enough to fit into a shirt pocket. Moore's Law was actually the fifth paradigm to provide accelerating price-performance [4]. The exponential technology advance in computing devices (computing speed per unit cost) has existed for the entire past century. Integration is the leading driver in the semiconductor world in the 20th and 21st centuries, both technologically and economically.

While the term IC generally refers to microelectronics, the analogous term photonic integrated circuit (PIC), also sometimes referred to as planar lightwave circuits, offers functionality of information signals imposed on an optical carrier ranging from the ultraviolet to near infrared. Though the growth of PICs can also be depicted and predicted by a photonic "Moore's Law" [5, 6], several figures of merit including critical dimensions, integration scale, complexity of function, and cost per unit component show that present PICs are many generations behind electronic ICs. PICs appeared much later than ICs and have grown more slowly (Fig. 15.1(b)). The reasons that PIC integration advances have occurred more slowly are partially market based, partially technology based, and partially the result of the choice of host material. Most telecom devices are based on Indium Phosphide (InP) substrates, which have required custom fabrication lines dedicated to InP photonics.

The first transistor and one of the first two ICs were demonstrated on germanium (Ge), but silicon (Si) quickly became the dominant host material for electronic ICs. Si is the second most abundant element on earth, but more importantly, Si has out-

bowers@ece.ucsb.edu

performed Ge and even many compound semiconductors from the early stage of IC development due to large bandgap and thermal conductivity, stable and high crystal quality/purity, excellent mechanical properties and an ideal native oxide, SiO_2. Unlike Si-dominated electronic ICs, PICs have been fabricated in a variety of host material systems, including element semiconductors (Si- and Ge-related), compound semiconductors (InP- and Gallium Arsenide (GaAs)-based), dielectrics (SiO_2 and SiN_x-related), polymers and crystalline materials (e.g. $LiNbO_3$). The material properties of different material systems place them into desirable but discrete functionality regimes. For example, InP and GaAs are flagship materials for light sources, while silica- and Si-based waveguides exhibit more than an order of magnitude lower propagation loss than III–V counterparts with the same dimensions.

Material incompatibility between different material systems has been the largest barrier to singling out a unitary host material for large-scale PICs. Analogous to a long-term debate in electronic ICs about whether to integrate high-performance electronics on Si, InP or GaAs, the same question surfaced lately in the PIC community. This debate did not shake the dominance of Si in electronic ICs, though several successful compound semiconductor-based IC chip companies, such as Vitesse, RF Micro Devices, Skywork solutions, and Broadcom, etc., were successful in target markets. The success of Si-based electronic ICs proves the wisdom in determination of a primary host material, which is reflected by the International Technology Roadmap for Semiconductors (ITRS) [8]. The solidification of silicon's role resulted in rational technology development and deployment, drastically reducing the uncertainties in investments, critical research directions and resource allocations. The past half-century technology revolution in design tools, circuit architecture, substrate manufacturing and epitaxy, device processing, packaging, testing and quality control led to the present Si IC industry with about 200 billion U.S. dollars in revenue per year [9]. The annual research and development investment in electronic ICs, particularly in device innovation, is about $45 billion/year. This level of R&D spending is unaffordable for the PIC industry due to a much smaller volume and revenue.

It is therefore important to determine the primary host material for PICs. InP-based compound semiconductors and Si compete for the mainstream adoption as the host material for future PICs. A 40 Gb/s InP-based single-chip all-photonic transceiver has been demonstrated [10]. It includes a high-gain, high-saturation power semiconductor optical amplifier-uni-traveling receiver and a widely tunable transmitter that combines a sampled grating distributed Bragg reflector (DBR) laser with an electroabsorption modulator (EAM) [10, 11]. The first InP monolithic tunable optical router with error-free 40 Gb/s operation per port was demonstrated successfully by Nicholes et al. [7]. The device has eight wavelength converters and an 8×8 arrayed-waveguide grating router (see Sect. 9.6), yielding more than 200 on-chip functional elements. InP chip maker Infinera has introduced two new PICs: the sliceable ePIC-500 (supports a 500 Gb/s super-channel) and the application-optimized oPIC-100 (supports one wavelength channel at 100 Gb/s), for terabit scale metro and regional DWDM networks. This new coherent PIC technology integrates over 600 optical functions into just two optical chips. Infinera also sees a technology pathway that will allow their future PICs to scale and support 2 Tb/s, 4 Tb/s and

bowers@ece.ucsb.edu

even greater capacity per line card in the future. Luxtera, now acquired by Molex, is an industry leader in complementary metal oxide semiconductor (CMOS) photonics and have developed a four channel 25 Gb/s product for the 100 Gb/s Ethernet and InfiniBand markets. PICs are presently moving forward on parallel Si and III–V platforms, but the future requirement for higher capacity, lower power on-chip and off-chip *optical* interconnects in microprocessors may tilt the balance. Larger bandwidth, lower power consumption (i.e., lower heat dissipation), smaller interconnect delays, and better resistance to electromagnetic interference are attractive advantages over the conventional Cu and Al electrical interconnects [12]. By leveraging the mature CMOS technology along with low-cost and high-quality Si substrates, redundant investments in money and time for fundamental research, infrastructure, and business model development can be largely reduced. With the compensation and assistance of mature electronic ICs, Si PICs are able to tolerate more error, lowering the design and fabrication criteria. Furthermore, the potentially enormous volume of optical interconnects (on-chip, inter-chip, rack-to-rack) is several orders of magnitude larger than the sum of conventional PIC markets. Exciting results in CMOS optical components, such as continuous-wave (cw) Si Raman lasers, modulators, detectors, optical buffers and switches, have been demonstrated in succession in university and industrial labs in the past few years. The basic operation principles of key devices for transmitters are discussed in the following sections, starting from a major question still being investigated: how to deploy a high-performance electrically-driven cw light source on Si?

15.2 Lasers (Emitters) and Amplifiers on Silicon

As discussed in Sect. 15.1, GaAs- and InP-based III–V materials have been dominant candidates for semiconductor light emitting devices for nearly half a century. Si has not been widely used because it has an indirect bandgap, and hence is a poor light emitting material. The band structure for Si is shown in Fig. 15.2(a) where it can be seen that free electrons tend to reside at the X valley, which is the lowest point in the conduction band. However, the X valley doesn't align with the peak of the valence band where holes find their lowest energy to stay. This momentum mismatch determines that free electrons have to bridge to the Γ valley through phonons in order to recombine with holes in the valence band *radiatively*. This transition has a low probability, resulting in a long radiative lifetime of ∼milliseconds. Meanwhile, these free carriers (electrons and holes) can recombine *nonradiatively*, resulting in extremely poor internal quantum efficiency η_i of light emission in Si, which is in the order of 10^{-6} and is defined as [13]

$$\eta_i = \frac{\tau_{nonrad}}{\tau_{nonrad} + \tau_{rad}} \tag{15.1}$$

where τ_{nonrad} and τ_{rad} are recombination lifetimes for nonradiative and radiative processes, respectively.

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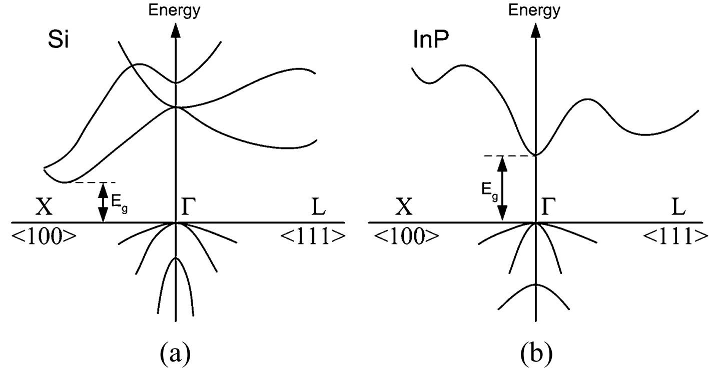

Fig. 15.2 Energy band diagrams of (**a**) Si and (**b**) InP at 300 K

The band diagram of InP is shown in Fig. 15.2(b), and has a direct bandgap, which means electrons and holes can recombine radiatively with high efficiency ($\eta_i \sim 1$).

A major source of nonradiative recombination in processed Si is trap recombination. Another major nonradiative process is Auger recombination where an electron (or hole) is excited to a higher energy level by absorbing the released energy from an electron-hole recombination. The Auger recombination rate R increases with injected free carrier density ΔN and is inversely proportional to the bandgap. Since the Auger recombination is a three-particle process, the Auger recombination rate for high-level carrier injection with $\Delta N \approx \Delta P$ is proportional to ΔN^3

$$\tau_a = N/R = N/C_a \Delta N^3 \approx 1/C_a \Delta N^2 \tag{15.2}$$

where C_a is the ambipolar Auger coefficient around 10^{-30} cm^6/s [14]. It is the dominant recombination mechanism for high-level carrier injection ($\Delta N \sim 10^{19}$ cm^{-3}) in Si.

Free carrier absorption represents another hurdle to realizing lasing in Si. The free electrons in the conduction band can jump to higher energy levels by absorbing photons. This process leads to higher optical loss as governed by (15.3) [15],

$$\alpha_f = \frac{q^3 \lambda_0^2}{4\pi^2 c^3 n \varepsilon_0} \left(\frac{N_e}{m_{ce}^{*2} \mu_e} + \frac{N_h}{m_{ch}^{*2} \mu_h} \right) \tag{15.3}$$

where q is the electronic charge, λ_0 is the vacuum wavelength, n is the refractive index of Si, ε_0 is the permittivity of free space, $N_e(N_h)$ is the free electron (hole) concentration, and $\mu_e(\mu_h)$ is the electron (hole) mobility. In high-level carrier injection devices (e.g. lasers and amplifiers) or heavily-doped situations, free carrier loss is orders of magnitudes higher than the material gain [15]. It explains why intrinsic or lightly-doped Si is used as low-loss waveguide material, but excessively high free carrier absorption stands as another major limitation for achieving lasing in heavily doped cases.

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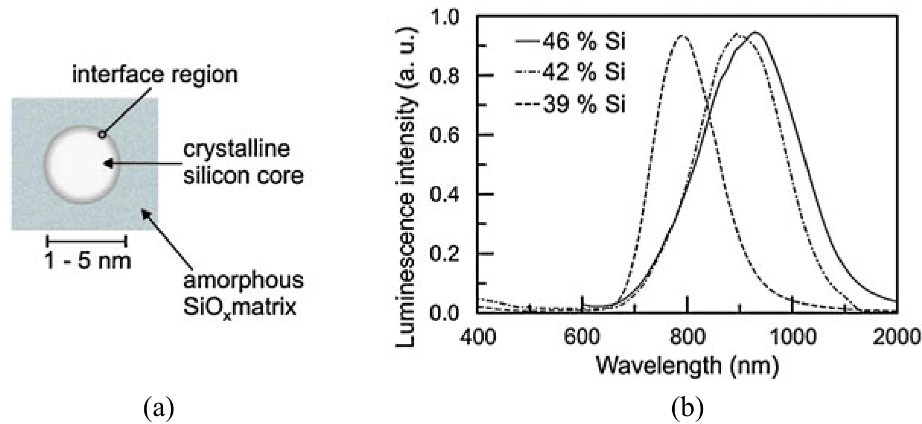

Fig. 15.3 (**a**) TEM cross-section of a typical Si-nc embedded in the SiO_x dielectric. (Courtesy Lorenzo Pavesi, University of Trento, Italy.) (**b**) Luminescence spectrum of Si-nc in dielectric [16]

15.2.1 Low-Dimensional Silicon Approaches

Recently, a number of groups have reported enhanced light-emitting efficiency in low-dimensional (i.e. in the order of the de Broglie wavelength) Si including porous Si [17–20], Si nanocrystals [21, 22], SOI superlattices [23], and Si nano-pillars [24, 25]. The motivation is to achieve the quantum confinement of excitons in a nanometer-scale crystalline structure [22]. In the meantime, the spatial localization of carriers by dielectrics also decreases the probability of nonradiative recombination with defects or trap centers, i.e. increases nonradiative recombination lifetime τ_{nonrad} and subsequently internal quantum efficiency η_i, and form radiative states [26].

For the first time Pavesi et al. reported the observation of optical net gain and modal gain in Si nanoclusters (Si-nc) dispersed in a silica matrix [27]. The Si-nc can be formed by introducing Si nanoparticles into ultra-pure quartz, thermal SiO_2 or plasma-enhanced chemical vapor deposition (PECVD) SiO_2, etc. by deposition, sputtering, ion implantation, cluster evaporation, etc. The excess Si (excess with respect to the SiO_2 stoichiometric quantity) clusterizes after a thermal annealing process (∼1100 °C) which leads to phase separation. The thermal process and the starting excess Si content determine the final sizes of the clusters and the Si-nc crystalline nature. As shown in Fig. 15.3(a), the Si-nc embedded in an amorphous SiO_x matrix have a core-shell structure with a crystalline Si core (1–5 nm) and a thin (∼0.5 nm) transition layer of a suboxide (Si-nc interface) [28]. Figure 15.3(b) shows luminescence spectra of Si-nc for various Si concentrations [16]. As can be seen the emission shifts to shorter wavelengths with decreasing Si concentration which goes along with a smaller mean Si-nc radius. Furthermore, the width of the luminescence bands gets narrower and the luminescence intensity increases as the Si-nc size decreases [16]. It is believed that the luminescence comes from confined exciton recombination in the Si-nc at around 800 nm [29] and radiative interface states around 700 nm [30]. The luminescence spectral broadening is intrinsic in nature [27].

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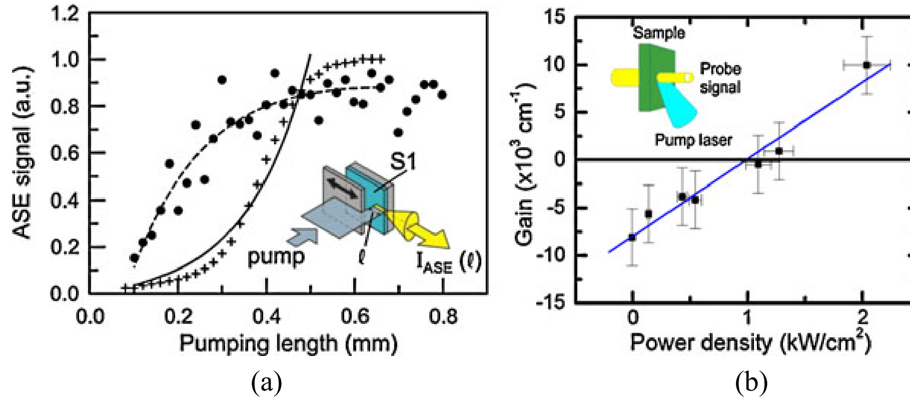

Fig. 15.4 ASE vs. pumping length of Si-nc for pump powers of 10 W/cm^2 [16] and 1 kW/cm^2 [31]. (**a**) Corresponding modal gain at 800 nm: $g = -20$ cm^{-1} and $g = 100$ cm^{-1}, respectively, (**b**) dependence of material gain on pump power density geometry. *Insets*: (**a**) Schematic of variable stripe length (VSL) method and (**b**) pump-probe measurement geometry (Courtesy Lorenzo Pavesi, University of Trento, Italy)

The optical gain from Si-nc formed by many different techniques was measured by the variable stripe length method (VSL) [16] and the pump-probe technique [31], as shown schematically in Figs. 15.4(a), inset and (b), inset, respectively. VSL measures the amplified spontaneous emission (ASE) signal coming out of an edge of a waveguide with a Si-nc-rich core. Figure 15.4(a) shows the ASE signal intensity I_{ASE} vs. pump length l for Si-nc formed by PECVD. The ASE signal intensity increases sublinearly with the pumping length when the pump power ($\lambda = 390$ nm) is lower than threshold. But when the pump power is above this threshold and net modal gain becomes positive, the ASE signal increases more than exponentially, which can be fitted with [27]:

$$I_{ASE}(l) = \frac{I_{sp}(\theta) \cdot l}{g_{mod}}(g_{mod}l - 1) \tag{15.4}$$

$$g_{mod} = \Gamma g - \alpha \tag{15.5}$$

where I_{sp} is the spontaneous emission intensity emitted within the observation angle (θ) per unit length, α is the overall loss coefficient, Γ is the optical confinement factor in the active layer, and g is the net material gain. A modal gain g_{mod} of -20 cm^{-1} at 800 nm emission wavelength was deduced when the pump power was 10 W/cm^2, while 1 kW/cm^2 pump power leads to 100 cm^{-1} modal gain. For pump length $l > 0.5$ mm, I_{ASE} saturates as expected for any finite power supply amplification mechanism.

The pump-probe transmission measurement (Fig. 15.4(b), inset) involves the use of an intense laser pump beam (390 nm in this case [27]) to excite the Si-nc to reach population inversion while a weak probe signal at ~800 nm simultaneously passes through the sample with active region thickness d. The Si-nc in the quartz substrate are formed by negative ion implantation and thermal anneal [27]. In the presence (absence) of a sufficiently strong pump beam the probe signal is amplified

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(absorbed). Figure 15.4(b) shows the net material gain extracted from (15.6) as a function of pump power.

$$I_{tr} = I_{in} e^{(g-\alpha)d} \tag{15.6}$$

where I_{tr} and I_{in} refer to transmitted and incident probe beam intensities, respectively. Up to 10,000 cm^{-1} average material gain is obtained, comparable to that of self-assembled quantum dots made of III–V semiconductors [32]. No change in probe signal intensity is observed when the same measurement is performed on an identical quartz sample without Si-nc. A four-level system model has been proposed to interpret the population inversion scheme in Si-nc. A more detailed discussion can be found in [13].

Several approaches have been demonstrated lately to achieve electrically-injected light emission, including a light-emitting diode (LED) structure [33] and a field-effect LED [34, 35] with the demonstration of 1 MHz direct modulation speed [36]. The critical design element of all is to embed Si-nc into an ultrathin dielectric layer which is sandwiched by a poly-Si layer and a single crystalline Si substrate to allow efficient carrier injection by tunneling. A large amount of effort is focused on reducing leakage current in the dielectric and achieving high enough current density without excessive device heating and premature failure for amplifiers and lasers. Another intrinsic limitation for Si-nc-based emitters is the difficulty of integration with conventional SOI waveguides due to emission around 800 nm.

Incorporating rare earth doping (e.g. Er, Tb, Yb, Gd) into Si-nc is a way to shift emission to the important communication wavelengths of 1.3–1.6 μm [37]. Following the revolution that the Er-doped fiber amplifier (EDFA) led in fiber optic telecommunications, research in Si emitters has been concentrated to doping Si with rare earth elements [38, 39]. However, it has been shown that Si is not a good host material to accommodate rare earth elements. Dopant clustering and back transfer of energy from the rare earth element are main obstacles to obtaining high emission efficiency [40]. SiO_2 dielectric with Si-nc therefore seems a better host choice for Er^{3+} [37] because the SiO_2 environment is an excellent natural host material for Er^{3+}, and Si-nc are shown to act as a good sensitizer as well [37, 41]. The energy of excitons excited by optical or electrical pumping from Si-nc is transferred to Er^{3+} ions which are coupled to adjacent Si-nc. Up to 70% energy transfer efficiency has been reported from Si-nc to Er^{3+} [42]. By employing a light-emitting device structure with 5.5 A/cm^2 injection current density in Fig. 15.5(a), room-temperature electroluminescence (EL) at 1.54 μm, corresponding to typical Er first-excited multiplet $^4I_{13/2}$ to the ground state $^4I_{15/2}$ transitions, is demonstrated [40]. Two metal rings provide the electrical contacts to the n-type poly-Si and to the p-type Si substrate. Emission is detected from the metal-free central area. The disappearance of the intrinsic EL peak around 800–900 nm for Si-nc in Er-doped Si-nc samples clearly proves the efficient energy transfer from excitons formed in Si-nc to the rare earth ions.

However, significant light emission diminishes quickly from low temperature (30 K) to room temperature under electrical pumping, a much faster decay than in the case of optical pumping [40]. Studies of PL (488 nm, 10 mW) under different

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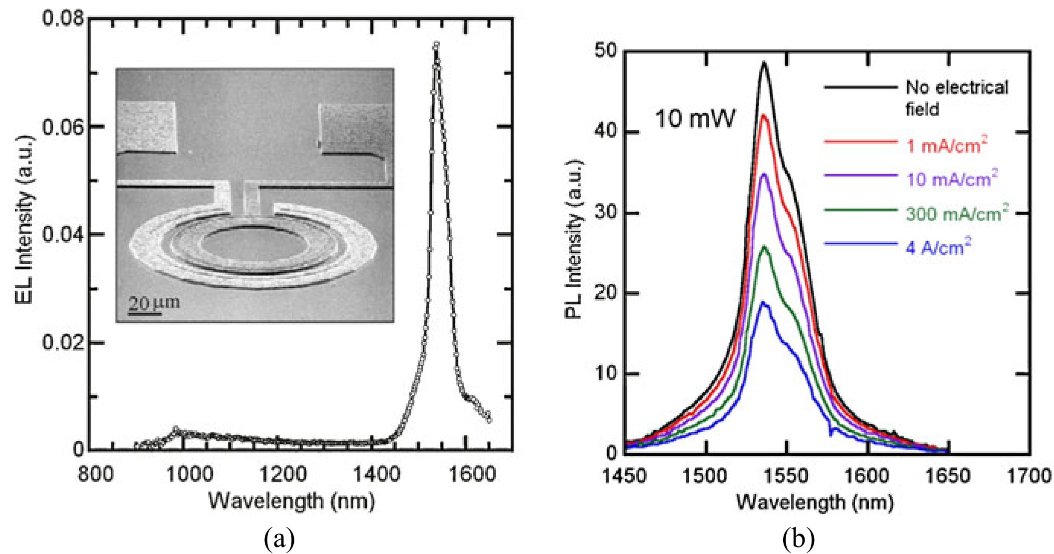

Fig. 15.5 (**a**) EL spectrum of a device based on Er-doped Si-nc obtained at room temperature under forward bias conditions with a current density of 5.5 A/cm^2. *Inset*: SEM image of an LED device structure with ring-type electrodes. (**b**) PL spectra of a device based on Er-doped amorphous Si-nc for the unbiased device (*black line*) and in the presence of different current densities flowing through the device (Courtesy Fabio Iacona, Center of Materials and Technologies for Information and Communication Science (MATIS CNR-INFM), Catania, Italy)

electrical biases have been performed to investigate the effect of injected carriers on the luminescence properties. Figure 15.5 shows the PL spectra with the device under different forward bias, compared with that of the unbiased case. A clear quenching of the PL signal with increasing electrical pumping is noticed, indicating the new possible nonradiative paths with the presence of electrically-injected carriers. Iacona et al. [40] believe that independent but unbalanced electron and hole injection causes the Auger de-excitation of Er ions. For the conventional PL, on the other hand, electron-hole pairs are generated simultaneously in the active region and then undergo a rapid recombination with subsequent Er excitation. For electrical pumping, measurements suggest that more electrons than holes are injected into the active region in these devices. It results in wasting a certain amount of current since they do not recombine with holes and cause the Auger de-excitation of Er ions [40]. In addition to the major challenge of increasing the injection current density in all Si-nc-based light emitting devices, how to overcome the EL efficiency degradation with increasing injected current density is a problem for Er-doped devices.

In another promising experiment, utilizing low-dimensional Si, Cloutier et al. observed optical gain and stimulated emission in nanopatterned crystalline Si [43]. Figure 15.6, inset, is an SEM side-view of periodic nanopatterned Si with a highly ordered array of holes in the top Si layer of a conventional SOI wafer. The top Si is about 100 nm thick with 3 μm buried oxide underneath. An anodic aluminum oxide nanopore membrane serves as a mask for patterning holes with 60 nm diameter and 110 nm center-to-center spacing in Cl_2–BCl_3 plasma dry etch. Figure 15.6(a) shows the edge emission from a cw optically-pumped sample at 10 K. In the spectrum of

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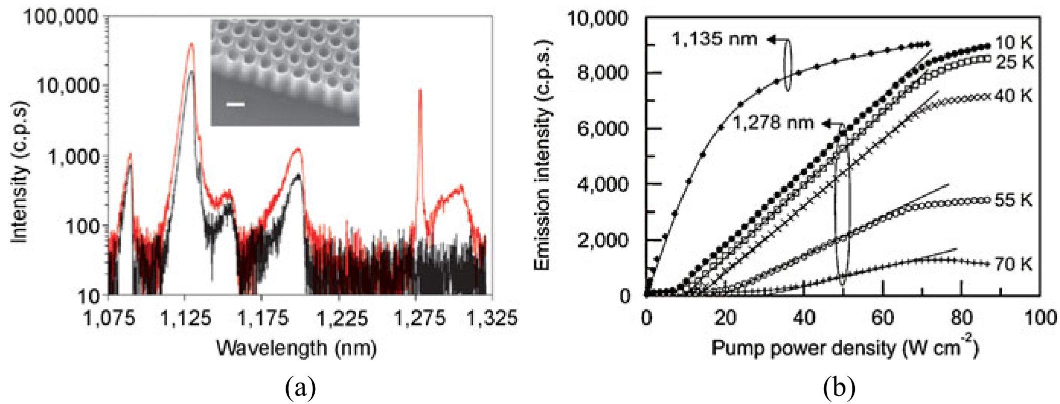

Fig. 15.6 (**a**) Edge-emission spectra from cleaved nanopatterned (*red*) and unpatterned (*black*) samples at 10 K. *Inset*: Side-view SEM image of nanopatterned Si; scale bar: 100 nm. (**b**) Evolution of the edge-emission intensity of the 1278 nm line as a function of pump power at 10, 25, 40, 55 and 70 K temperatures. The evolution of the 1135 nm phonon-assisted free-exciton line at 10 K is shown for comparison. Its intensity has been divided by 7 to plot all curves on the same scale (reproduced from [43] under permission of Macmillan Publishers Ltd.)

this gain-guided slab waveguide, a sharp peak at 1278 nm is observed and remains detectable till 80 K. The other emission bands in the spectrum below 1250 nm, believed to be emission from the crystalline Si substrate, are similar to the classical spontaneous PL emission bands of an unpatterned reference SOI sample. The temperature-dependent 1278 nm-peak intensity vs. cw pump power density characteristic is shown in Fig. 15.6(b). Transition from spontaneous to stimulated emission is observed in the 10–70 K range. Linewidth narrowing after passing pump power threshold presented additional evidence of stimulated emission. The phonon-assisted free-exciton recombination PL band at 1135 nm is also plotted to show no stimulated emission observable at this wavelength. The optical gain in nanopatterned Si is measured with the variable stripe length method discussed previously. Modal gains g_{mod} of 260, 247, 230, 165, and 88 ± 5 cm^{-1} [44] are measured at 10, 25, 40, 55 and 70 K, respectively, with a fixed pump power density of 65 W/cm^2. In contrast, a modal loss of -31 ± 5 cm^{-1} at 10 K is measured when the pump power density is only 8 W/cm^2, i.e. below pump threshold [43].

The optical gain and stimulated emission in nanopatterned Si is attributed to the bistable carbon-substitutional-carbon-interstitial (C_sC_i) complex known as the *G-center* [44]. It is well-known that substitutional carbon (C_s) atoms occur naturally in Si wafers at concentrations between 10^{15} and 10^{17} cm^{-3} depending on the crystal growth technique [45], and are necessary for *G-center* formation. A *G-center* is created when a mobile interstitial carbon atom (C_i) binds with a substitutional carbon atom (C_s), a consequence of a damage event and following C_s–Si_i exchange (where Si_i represents a Si interstitial) [46]. The density of *G-centers* depends on the densities of C_s in the lattice and introduced C_s–Si_i. Recent studies show that nanopatterned carbon-rich Si generates higher gain. Figure 15.7(a) exhibits a 33× enhancement in the PL intensity at 25 K for a nanopatterned Si with $\sim 10^{19}$ cm^{-3} carbon atoms implanted (background carbon concentration: 2.5×10^{16} cm^{-3}), compared

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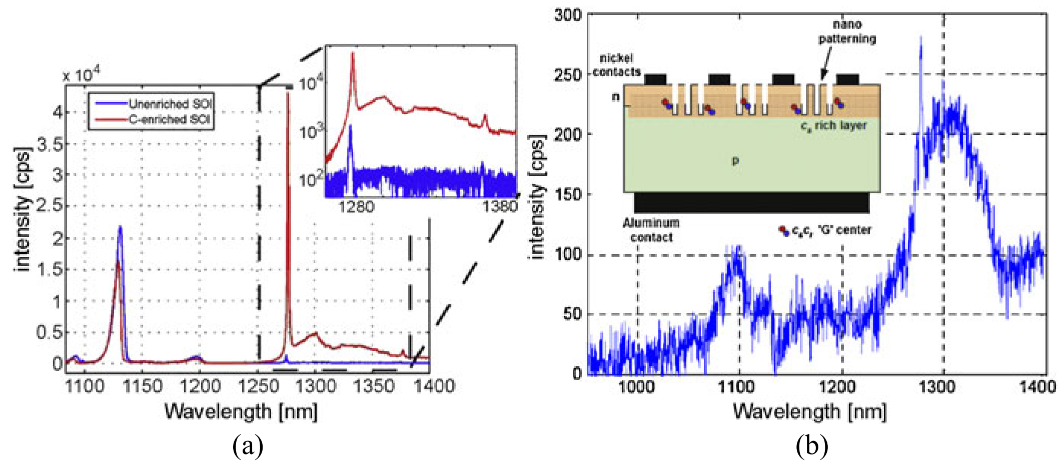

Fig. 15.7 (**a**) Photoluminescence spectrum at 25 K of nanopatterned Si and nanopatterned C-enriched Si. The *inset* shows a semi-logarithmic plot of the region containing the G line and phonon replicas. (**b**) Electroluminescence spectrum of *G-center* LED at 60 K and a current of 50 mA. *Inset*: Schematic of the *G-center* LED in nanopatterned Si (reproduced from [44] under the permission of American Institute of Physics)

with the PL response from a base-line nanopatterned SOI sample with background carbon concentration. These results confirm that the carbon in the silicon crystal is responsible for the creation of *G-centers*, rather than the dry etching process [44]. It also provides a path for increasing the efficiency and gain of this material. Electroluminescence at 1287 nm is demonstrated in the nanopatterned Si pn junction with a 100 nm-thick carbon-rich layer at the junction interface (Fig. 15.7(b), inset) [44]. Figure 15.7(b) shows the electroluminescence from the device at 60 K with a current of 50 mA. The mechanism of the electroluminescence can be described briefly in the following way: the *G-center* is bistable and can be excited below 50 K. The excited/injected carriers occupy the *G-center*-induced acceptor and donor states existing inside the conventional Si bandgap, resulting in a sub-bandgap of 0.97 eV. The trapped electrons and holes can recombine directly producing a phonon-less emission at 1278 nm, or indirectly producing an emission band extending from 1250 nm to 1350 nm. However, emission is quickly diminished at higher temperatures when carriers in the *G-center*-induced states move back to the conduction and valence bands [44].

With the availability of nanotechnology, the phonon-selection rule can be relaxed or broken by crystal-symmetry breaking or phonon localization; however, it still remains challenging to achieve room-temperature cw lasing based on these temperature-dominated processes presently.

15.2.2 Raman Effect

Raman scattering is an inelastic scattering mechanism where photons propagating through the medium give up energy or gain energy from surrounding opti-

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cal phonons. This results in a frequency shifted output photon of −15.6 THz and +15.6 THz in bulk silicon for the Stokes and anti-Stokes, respectively [47]. The anti-Stokes can typically be neglected over the Stokes under equilibrium temperature conditions and no external crystal phonon excitation due to Boltzmann statistics.

Spontaneous Raman emission occurs in a linear regime where the scattered light intensity is linearly proportional to the pump light intensity. Above a certain threshold this interaction is no longer linear and Stimulated Raman Scattering (SRS) occurs. The SRS relation for the change in Raman power can be written as:

$$\frac{dP_R}{dz} = g_R \cdot P_R \cdot P_P \tag{15.7}$$

where P_R is the power of the Raman signal at the Stokes wavelength, P_p is the pump power, and g_R is the SRS gain coefficient. The Raman gain coefficient is [47]:

$$g_R = \frac{8\pi c^2 \omega_p}{\hbar \omega_s^4 n_s^2 \omega_s (N+1) \Delta\omega_s} S \tag{15.8}$$

where ω_p and ω_s are the frequencies of the pump and Stokes wavelengths, respectively. n_s, N, and $\Delta\omega_s$ are the index of refraction at the Stokes wavelength, the Bose occupation factor (0.1 at room temperature), and the full-width-half-maximum of the spontaneous Raman spectrum, respectively. S is the spontaneous scattering efficiency.

Although the 1.3 and 1.5 μm operating wavelengths are well below the bandgap energy of silicon and single photons are not absorbed, two photon absorption (TPA) still occurs. TPA is a nonlinear loss mechanism that increases as the number of photons increases in a waveguide. During TPA, two photons are absorbed by an electron in the valence band, exciting it as a free carrier into the conduction band. The free carriers generated through TPA add an additional carrier induced loss, free carrier absorption (FCA), discussed previously, to the signal [48].

The first demonstration of a pulsed silicon Raman laser [49] overcame TPA by using a long delay within the laser cavity (an 8 m long cavity), and a short optical pulse such that the carriers generated during TPA would recombine prior to the next pass of the optical pulse (Fig. 15.8(a)). The experimental light output versus pump light (L–L) characteristic is shown in Fig. 15.8(b). Most demonstrations in silicon have been conducted with a pump wavelength of ∼1550 nm and a lasing wavelength near 1690 nm.

In order to achieve net gain under continuous wave operation, the conduction band carrier lifetime needs to be reduced. This can be achieved in a few ways. One method is to reduce the volume-to-surface ratio of the waveguide in order to increase the surface recombination rate of the carriers. Imbedding a p–i–n structure into the waveguide to sweep carriers away [52] resulted in the first cw demonstration of a silicon Raman laser [50] and is the approach most widely used [53]. Figure 15.9(a) shows the cross section of a waveguide with an imbedded p–i–n structure, along with the first cw L–L curve [50]. Although the p–i–n structure reduces the carrier lifetime to achieve lasing, TPA and FCA increase the cavity loss at higher pump powers leading to compression of the L–L curve (Fig. 15.9(b)).

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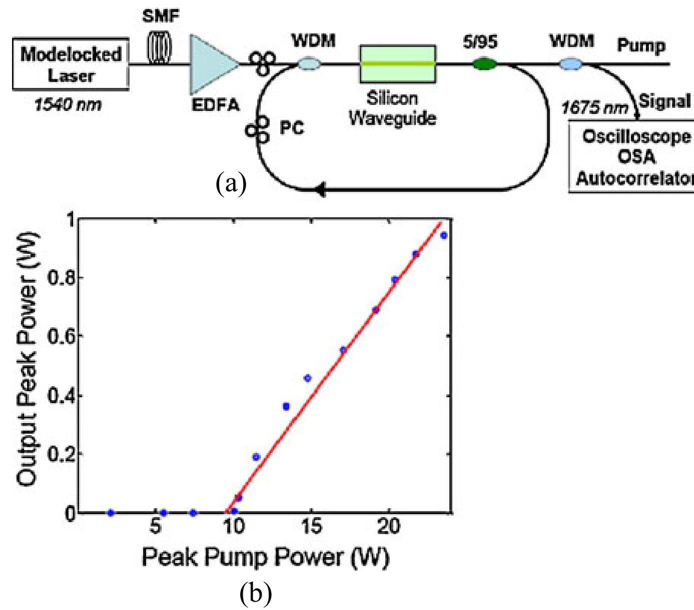

Fig. 15.8 (**a**) Experimental setup and (**b**) laser light vs pump light from the first pulsed silicon Raman laser [49] (reproduction under permission of the Optical Society of America)

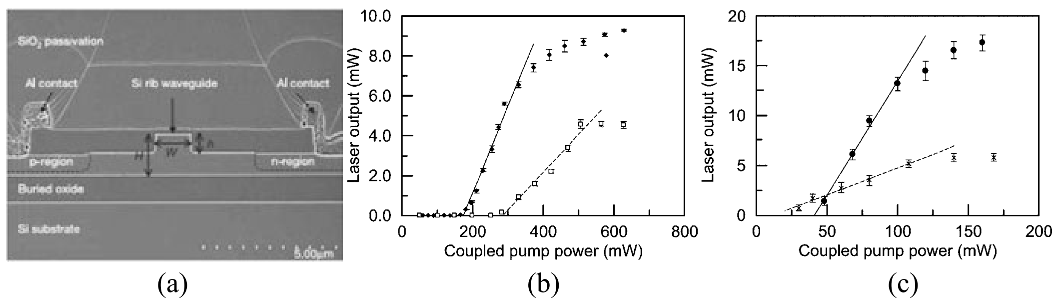

Fig. 15.9 (**a**) Waveguide cross section with imbedded p–i–n cross section for carrier lifetime reduction. (**b**) *L*–*L* curve of first continuous wave silicon Raman laser [50]. (**c**) *L*–*L* curve of racetrack Raman laser [51] (reproduction under permission of Macmillan Publishers Ltd. and American Institute of Physics)

Further improvements in laser performance have been made by utilizing a specially designed ring cavity that enhances the pump wavelength in the cavity while still allowing power at the lasing wavelength to efficiently exit the cavity [53]. This has led to a reduction in threshold pump power from 200 mW to 20 mW while increasing the maximum laser output power from 10 mW to 18 mW (Fig. 15.9(c)). Another configuration of this ring has been used to generate lasing at longer wavelengths (1848 nm) not typically accessible by InP or GaAs based semiconductor lasers [51]. The cavity of this cascaded Si Raman laser is designed such that lasing at 1680 nm acts as a pump for second order lasing at 1848 nm. Figure 15.10 shows the spectra of the pump, the first order lasing mode, and the second order lasing mode.

Silicon Raman amplifiers and lasers are unlikely to be integrated with CMOS chips due to the optical pump sources required. However, their excellent wavelength purity and emission wavelength are of interest in medical or sensing applications.

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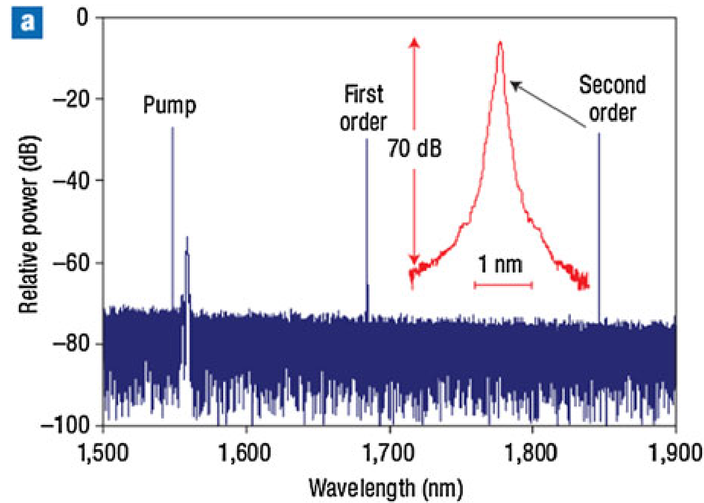

Fig. 15.10 Cascaded silicon Raman laser output spectrum measured with a grating-based optical spectrum analyser with a resolution of 0.01 nm, showing three peaks corresponding to the pump, the first- and the second-order laser outputs. *Inset*: high-resolution scan of the second-order lasing peak, showing 70 dB side-mode suppression ratio (SMSR) [51] (reproduction under permission of Macmillan Publishers Ltd.)

Table 15.1 Linear thermal expansion coefficients and bandgaps (300 K) of selected important semiconductors as a function of their lattice constants (300 K)

Semi-conductor	Lattice constant (nm)	Lattice mismatch to Si (%)	Bandgap (eV)	Linear TEC (10^{-6}/K)	Linear TEC (relative)
GaN	0.3189	−41.2815	3.20	3.17	1.22
Si	0.5431	0.0000	1.12	2.60	**1.00**
GaP	0.5451	0.3683	2.26	4.65	1.79
Ge	0.5646	3.9588	0.66	5.90	2.27
GaAs	0.5653	4.0876	1.42	5.73	2.20
InP	0.5869	8.0648	1.35	4.60	1.77
InAs	0.6058	11.5448	0.36	4.52	1.74

15.2.3 Monolithic Integration Approaches

An on-going effort for nearly four decades has been to achieve epitaxially grown compound direct bandgap materials on Si substrates. However, overcoming the mismatch in lattice constant and thermal expansion coefficient is a major challenge to achieving sufficiently low threading dislocation density [54]. Table 15.1 compares these two parameters of several important semiconductors. GaAs and InP have a lattice (thermal expansion coefficient) mismatch of 4.1% (120.4%) and 8.1% (76.9%), respectively. Thus, they lead to 10^8–10^{10} cm^{-2} threading or misfit dislocation density when GaAs or InP is grown on Si substrates [55]. Numerous approaches including special surface treatment [56], strained superlattices [57, 58], low-temperature buffers [59] and growth on patterned substrates [60] have been employed to re-

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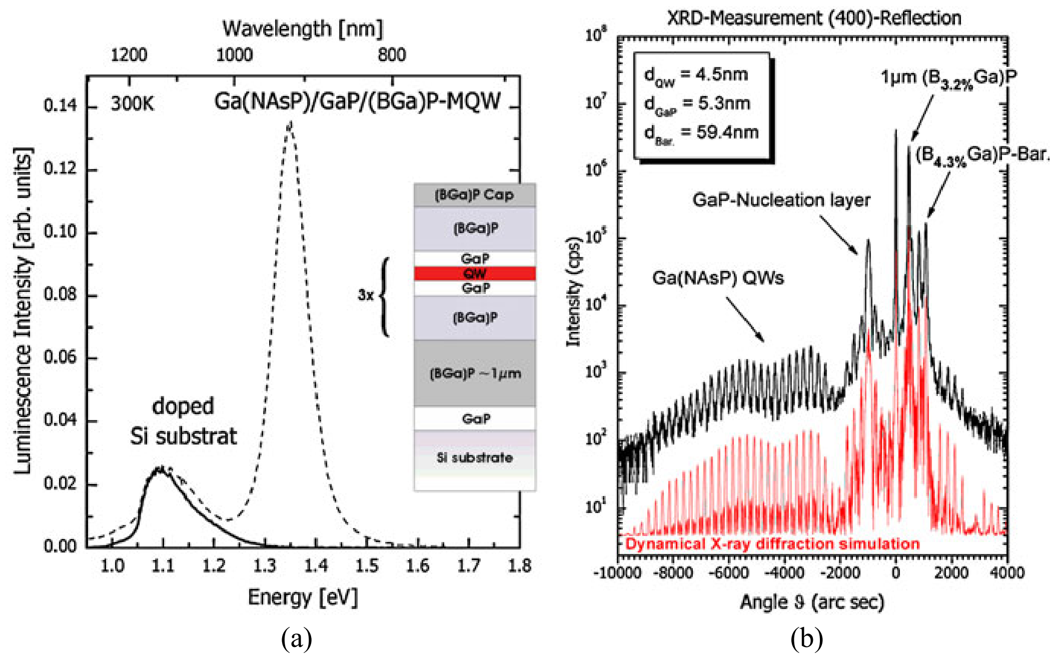

Fig. 15.11 (**a**) Room temperature PL spectrum of Ga(NAsP)/GaP/(BGa)P MQW structure (*dashed line*) in comparison to a doped Si substrate (*solid line*). *Inset*: Epitaxial layer structure. (**b**) High-resolution XRD pattern around the (400)-reflection of Si (*upper trace*: experimental, *lower trace*: modeling by dynamical X-ray diffraction theory) [61] (Courtesy Wolfgang Stolz, Philipps-Universität Marburg, Germany)

duce the dislocation density to around 10^5–10^6 cm^{-2}, still two orders of magnitude higher than the typical number ($<10^4$ cm^{-2}) in InP- or GaAs-based epitaxial wafers used to achieve room-temperature cw lasers. In this section we discuss several pertinent approaches to achieve high-quality heteroepitaxy thin films for Si photonics applications.

GaP is the binary compound semiconductor with smallest lattice mismatch with Si. Kunert et al. have demonstrated the monolithic integration of a Ga(NAsP)-based multiple quantum well (MQW) active region on Si with a (BGa)P/GaP buffer layer [61]. Ga(NAsP) pseudomorphically grown on GaP substrates has been introduced as a direct bandgap material [62]. By incorporating small percentages of N or B into GaP, it is also possible to adjust the lattice constant to match with Si. Tensile (BGa)P was selected to be the buffer and barrier material to balance the compressive strain of Ga(NAsP) quantum wells. The inset in Fig. 15.11(a) shows the MQW structure with a 100 nm GaP nucleation layer on (001) Si, followed by a 1 µm ($B_{0.0032}$Ga)P buffer. Each 4.5 nm Ga(NAsP) quantum well (QW) is sandwiched by a 5 nm GaP intermediate layer to avoid the formation of N–B bonds and a 60 nm ($B_{0.0043}$Ga)P barrier layer. Figure 15.11(a) shows the room-temperature PL spectrum of the sample, exhibiting a strong peak at 930 nm originating from the active region in addition to a broad peak at the Si bandgap. The relative intensity of the peak at 930 nm from 13 nm quantum wells is a good sign of appreciable material gain. High-resolution X-ray diffraction (XRD) is employed to probe the dislocation-induced MQW satellite fringe shifting or broadening. The good agreement between

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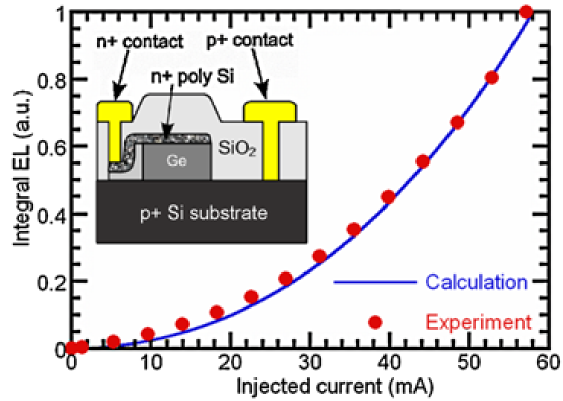

Fig. 15.12 Integral EL intensity of a 20 μm × 100 μm 0.2% tensile-strained Ge/Si p–i–n LED increases superlinearly with injected current, which agrees with theoretical calculations. *Inset*: Schematic cross-section of the Ge/Si LED [66] (courtesy Xiaochen Sun, MIT, Cambridge, MA, USA)

experimental and simulated data in Fig. 15.11(b) indicates excellent integrity of the active region. It is promising to obtain high-quality active region growth on a Si substrate when utilizing quaternary or even higher order compound semiconductor material systems, which give more freedom to compensate lattice-mismatched and thermal expansion- mismatched materials. More recently, demonstrations of lasing from an InGaAs/GaAs QW grown on GaP/Si template [63], as well as experiments on cryogenic laser operation using GaNAsP lattice matched to silicon [64] have been published and are relevant papers suggested for further reading.

Since the debut of the first transistor and integrated circuits on Ge, Ge(SiGe)-on-Si heteroepitaxy is of great interest for building light emitters on a Si substrate. Compatibility with modern CMOS technology and potential ~1.55 μm emission from direct band-to-band transitions (0.8 eV) are important reasons for corresponding research. Crystalline Ge is an indirect bandgap material with a minimum bandgap energy of 0.66 eV, close to the direct transition band. Theoretically, a 2% tensile strain is required for converting Ge into a direct bandgap material, while experiment shows a large emission wavelength red shift to 2.5 μm (0.5 eV) [65], which is of less interest for optical interconnects and telecommunications.

Strain engineering and heavy n-type doping were used to achieve room-temperature direct bandgap electroluminescence [66, 67]. Sun et al. selectively grew Ge on p^+ Si substrates and with moderate tensile strain of 0.2%–0.25% to reduce the direct bandgap between the minimum of the direct Γ valley and the maximum of the light-hole band to 0.76 eV [66]. Heavily doped poly-Si was used for the electrode, resulting in a p–i–n diode structure as shown schematically in Fig. 15.12, inset. Figure 15.12 demonstrates a superlinear relationship between the integral direct bandgap room-temperature electroluminescence intensity and the injected current. The electroluminescent intensity is proportional to both the total injected carrier concentration and the fraction of electrons scattered to the direct Γ valley. A model based on the Fermi-Dirac distribution has been developed to fit the experimental data very well [66]. An important question is whether the relatively high threading dislocation density of around 1.7×10^7 cm^{-2} could be a major hurdle to realizing diode lasers on this Ge-on-Si substrate.

Another room-temperature Ge LED has been demonstrated by n-type heavy doping, resulting in the Fermi level above the indirect L valley and good electron occu-

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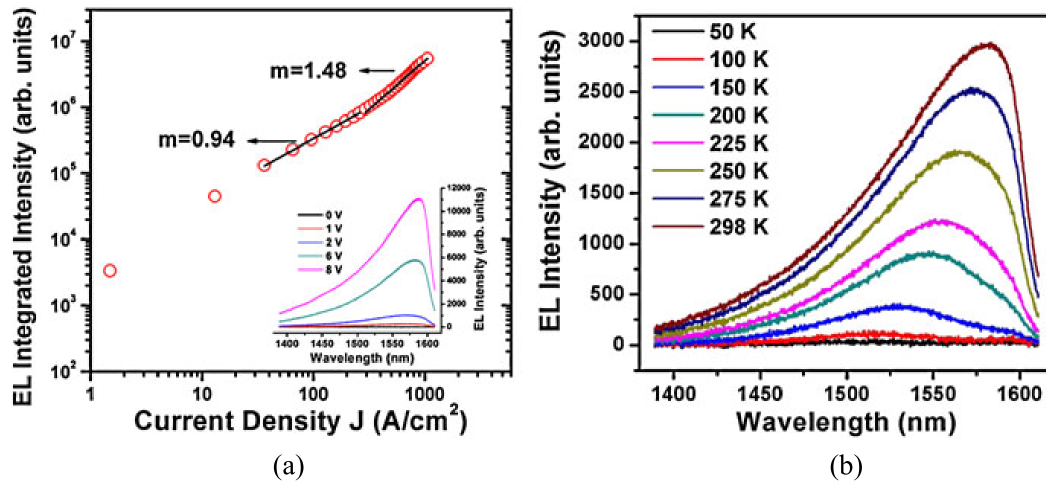

Fig. 15.13 (**a**) Integrated luminescence vs. current density (L–J^m) characteristics of a Ge LED. *Inset*: Electroluminescence spectra of the Ge LED under different applied biases. (**b**) EL spectra measured at various temperatures. Better radiative efficiencies are observed for higher temperatures (courtesy Szu-Lin Cheng, Stanford University, Standford, CA, USA)

pation of the direct Γ valley of Ge [67]. An n^+/p Ge homojunction LED structure (300 μm in diameter) on a Si substrate is employed. The doping concentrations of phosphorous and boron are 7.5×10^{18} cm^{-3} and 3.6×10^{17} cm^{-3}, respectively, achieved by in-situ doping to achieve an abrupt junction profile. Room temperature EL spectra of the Ge LED under different applied biases (Fig. 15.13(a), inset) show the EL peak located near 1.6 μm, indicating emission from the direct bandgap of Ge. The onset of the EL is at 0.75 V, closely matching the indirect bandgap (0.66 eV) of Ge. The corresponding injected current density vs. EL intensity in Fig. 15.13(a) exhibits a superlinear current density-EL intensity dependence and a fitting exponent m of 1.48 is observed for currents greater than 300 A/cm^2. This implies that the device is more effective when operating under high current, contrary to typical LEDs which suffer from low radiative efficiency at higher injection current levels due to enhanced Auger recombination. The hypothesis of this enhanced EL intensity is Joule heating-induced larger overlap of the Fermi-Dirac distribution of the carriers in the Γ valley, which is confirmed by temperature-dependent EL in Fig. 15.13(b). The wavelength peak shifts towards longer wavelength due to the shrinkage of the direct bandgap. The observation of this band filling effect in Ge LEDs is inverse to the EL quenching in devices which rely on quantum confinement effects like Si–Ge quantum-dot and quantum-well devices [68] and those discussed in Sect. 15.2.1, giving an edge to achieve room temperature lasing in the future. The use of high Q ring cavities together with these structures holds promise for room temperature lasing.

In 2012, electrically pumped room temperature lasing from a Ge-on-Si heterostructure was demonstrated [69]. This was achieved by doping Ge with phosphorous with concentrations in excess of 4×10^{19} cm^{-3}. A gain spectrum of 200 nm width and an output power of 1 mW were measured. More recently, lasing in a direct bandgap GeSn alloy grown on Ge/Si virtual substrate was reported [70]. The lasing

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wavelength is closer to 2 μm and required cryogenic cooling. Surface passivation and design optimization regarding doping, optical mode confinement and carrier injection is expected to increase the operation temperature as well as decrease the threshold excitation density.

Another exciting approach is the epitaxial growth of direct gap III–V semiconductors directly on silicon substrates [96, 97] with the use of epitaxial lateral overgrowth (ELO) to achieve high quality III–V layers. More recently, Z. Wang et al. showed an optically pumped InP based laser grown on (001) silicon operating at room temperature [98]. This novel epitaxial technology suppresses threading dislocations and anti-phase boundaries to a less than 20 nm thick layer not affecting the device performance. Future advances in these technologies can make them a competing platform for realizing lasers on silicon.

In the next section, we show recent results of quantum dot (QD) growth on silicon substrates using molecular beam epitaxy (MBE) and review laser performance to date using this approach.

15.2.4 Quantum Dot and Quantum Well Lasers on Silicon

InAs/GaAs quantum dot lasers emitting around 1.3 μm are the best studied semiconductor quantum dot system, and will be the primary focus of this section. Such quantum dot lasers have demonstrated the lowest threshold current densities and highest lasing temperatures of any semiconductor laser emitting in the telecom range [71, 72], making them an attractive candidate to meet low power consumption and athermal performance demands for silicon photonics devices/packages. Here, we review various methods to integrate self-assembled quantum dot lasers with silicon photonic devices, focusing on epitaxial growth of such laser structures directly onto silicon substrates.

The approach that is closest to commercial deployment is integration of quantum dot lasers via flip chip bonding and butt coupling onto ‘silicon optical interposer’ chips consisting of spot size converters, optical modulators, photodetectors, and power splitters. Such transceivers have demonstrated error free operation at 20 Gbit/s from 25 to 125 °C without active adjustment of the quantum dot laser, modulator, or photodiode [73]. Another approach to take advantage of the inherent benefits of quantum dot lasers for silicon photonics is the proposal of using a highly efficient temperature stable quantum dot comb laser as an external dense wavelength-division-multiplexing (DWDM) light source coupled into a silicon photonics chip for modulation and multiplexing [74].

InAs quantum dot lasers have also been integrated with silicon by wafer bonding. Using direct fusion bonding at 300–500 °C, broad area lasers (2.1 mm × 100 μm) with current injection across the bonded GaAs/Si interface show room temperature pulsed lasing thresholds of 205 A/cm^2 [75]. A pulsed lasing temperature up to 110 °C was reported by bonding p-doped quantum dot lasers in a later report [76]. Although the previous two structures were bonded on pure silicon wafers, wafer

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bonded quantum dot lasers on SOI waveguides have also been demonstrated (with the optical mode still confined in the III–V layers), paving the way for future integration with silicon waveguides [77].

Direct growth of quantum dot lasers onto silicon substrates represents another exciting approach for integration onto silicon. Historically, the primary focus of monolithic integration by epitaxy has been to achieve good laser performance by minimizing the number of generated dislocations as much as possible. Despite significant reductions in dislocation density to 10^5–10^6 cm^{-2}, dislocation densities near native substrate levels ($\sim 10^4$ cm^{-2}) appear difficult to achieve. One approach to further reduce the negative effects of residual dislocations on laser performance is to substitute QW active regions by three dimensional quantum dots. Physically, efficient capture and tight spatial confinement of injected carriers by individual quantum dots reduces total carrier migration and subsequent non-radiative recombination at dislocation cores. Because individual quantum dots are essentially independent of each other, the effect of threading dislocations in the active layer is greatly diluted if the quantum dot density is much higher than the dislocation density.

The prospect of using semiconductor quantum dots and their associated three-dimensional potential wells to reduce the effects of dislocations was proposed as early as 1991 [86]. Early explorations of this idea culminated in room temperature pulsed lasing at 1.1 µm or shorter, summarized in Table 15.2. For integra-

Table 15.2 Summary of In(Ga)As self-assembled quantum dot lasers epitaxially grown on silicon

Year	I_{th} (mA)/ J_{th} (A cm^{-2})	Max lasing temp (°C)	Device size (µm^2)	λ (µm)	PL linewidth (meV)	Ref.
1999	788/3850 (Pulsed 80 K)	–	800 × 50	1 (80 K)	49 (17 K)	[78]
2005–2009	500/900 (Pulsed)	95 (Pulsed)	600 × 80 (lowest threshold) 800 × 8 (highest temperature)	1	51	[79–81]
2011	1087.5/725 (Pulsed)	42 (Pulsed)	3000 × 50	1.3	37	[82]
2012	45/64.3 (Pulsed) 114/163 (cw)	84 (Pulsed) 30 (cw)	3500 × 20 (lowest threshold) 3000 × 20 (highest temperature)	1.26	38	[83]
2014	150/200 (Pulsed)	111 (Pulsed)	3000 × 25	1.25	37	[84]
2014	16/430 (cw)	119 (cw), >130 (Pulsed)	(700–1200) × (4–12)	1.25	37	[85]

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tion with silicon waveguides and/or transmission through silica fiber, longer wavelengths are desirable to minimize propagation loss. The first 1.3 μm InAs/GaAs quantum dot laser epitaxially grown on silicon was reported in 2011 [82]. The epitaxial structure comprised a GaAs buffer directly nucleated on a (001) silicon substrate off-cut 4 degrees from the [110] direction, followed by $In_{0.15}Ga_{0.85}As$/GaAs strained layer superlattice dislocation filter layers and another GaAs/$Al_{0.4}Ga_{0.6}As$ short-period superlattice. Following the buffer a conventional GaAs/AlGaAs separate confinement heterostructure (SCH) laser structure was grown with five layers of InAs/GaAs dot-in-a-well layers as the active region. Cleaved facet broad area lasers 3 mm long and 50 μm wide with Ti/Au p-contacts on the III–V epitaxial layer side and Cr/Au n-contact on the bottom silicon substrate showed room temperature pulsed lasing with a threshold current density of 725 A/cm^2. Lasing was limited to ≤42 °C, and a maximum room temperature output power of 26 mW was reported.

By using $In_{0.15}Al_{0.85}As$/GaAs strained layer superlattices in place of $In_{0.15}Ga_{0.85}As$/GaAs strained layer superlattices for improved dislocation filtering, as well as employing a top-top contact geometry to avoid current injection through the dislocated GaAs/Si interface as was done previously, the pulsed lasing threshold for a 3 mm × 25 μm broad area laser was reduced to 200 A/cm^2 [84]. Room temperature output powers above 100 mW have been obtained from a single cleaved facet, and the maximum lasing temperature under pulsed operation was simultaneously increased up to 111 °C [84]. Continuous-wave (cw) performance has not been reported for this device.

Previously, cw lasing of InAs/GaAs quantum dot lasers grown on a germanium substrate was demonstrated with comparable performance to those grown on GaAs substrates [87]. As mentioned above, epitaxial growth of germanium on silicon is a mature CMOS technology, and Ge/Si templates are now widely commercially available. Since Ge is nearly lattice matched to GaAs (0.08% lattice mismatch), growth of GaAs on Ge/Si substrates allows for decoupling of the lattice mismatch and polarity mismatch issues into separate interfaces (i.e. lattice mismatch is treated at the Ge/Si interface while polarity mismatch is treated at the GaAs/Ge interface, as opposed to dealing with both at the same interface which is the case with direct growth of GaAs on Si).

Continuous wave lasing of InAs/GaAs quantum dot lasers epitaxially grown on silicon was first achieved using such an intermediate Ge buffer approach [83]. The same InAs/GaAs quantum dot laser structure grown on Ge/Si substrates with a 2 μm Ge buffer but without strained superlattice dislocation filtering layers exhibits much-improved lasing characteristics compared to direct nucleation of GaAs on Si with very low room temperature pulsed lasing threshold of 64 A/cm^2, as well as room temperature cw lasing thresholds of 163 A/cm^2. Maximum cw output power at room temperature (RT) is 3.7 mW from both facets for a 3.5 mm long cavity with a 20 μm wide ridge. cw operation was sustained up to 30 °C in a 3 mm long device.

Further improvement in cw performance soon followed. InAs/GaAs quantum dot lasers grown on Ge/Si substrates with thresholds of 16 mA and 50 mW output power for small cavities have been demonstrated, while larger cavities have yielded up to

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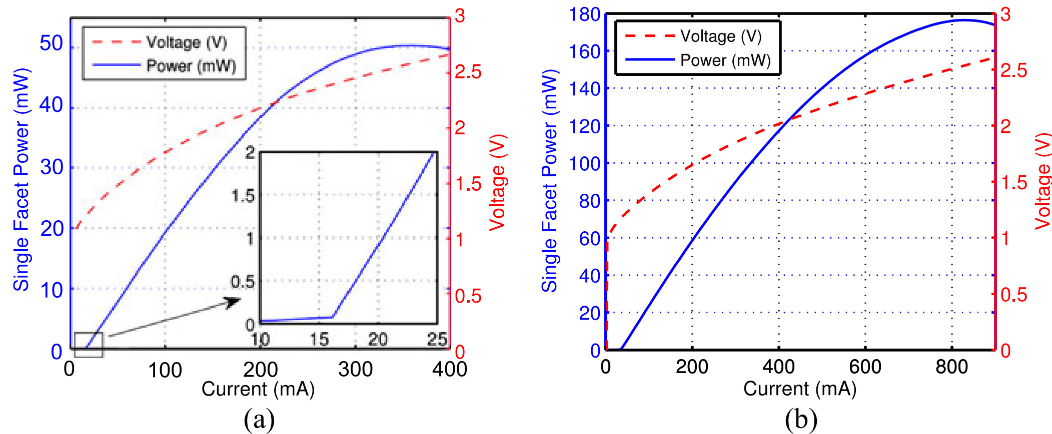

Fig. 15.14 (**a**) Room temperature cw light-current-voltage (LIV) plot of 7-layer quantum dot laser epitaxially grown on Ge/Si substrate with 95% HR coating on one facet, 937 × 4 μm^2 device size, 16 mA threshold current, 50 mW output power. (**b**) Characteristics of larger (1130 × 10 μm^2) but otherwise similar laser; 38 mA threshold current, 176 mW maximum output power [85]

176 mW output power so far with 38 mA threshold current (see Fig. 15.14) [85]. These devices employed seven dot layers for the active region and 95% dielectric high reflection (HR) coating on one facet. Modulation p-doping the GaAs barriers between the quantum dot layers can improve the laser characteristic temperature (T_0) to the 100–200 K range and cw lasing up to 119 °C (see Fig. 15.15). Analysis of >300 devices on two different wafers from separate growth runs exhibited similar characteristics with an average threshold current density of 500 A/cm^2 and minimum values as low as 250 A/cm^2 (see Fig. 15.16). A summary of the progress made with self-assembled quantum dot lasers epitaxially grown on Si or Ge/Si is presented in Table 15.2.

Reliable performance of epitaxially grown III–V lasers on silicon has been a major challenge. This is particularly true for GaAs/AlGaAs based lasers, which are susceptible to recombination enhanced defect reactions [88]. Reported lifetimes for GaAs based QW lasers epitaxially grown on silicon have ranged from a few seconds to 200 hours at room temperature (see Table 15.3). For example, GaAs/AlGaAs QW laser grown on Ge/Ge$_x$Si$_{1-x}$/Si substrates reported a cw lifetime at room temperature of around 4 hours under a constant applied current density of 270 A/cm^2 prior to catastrophic failure [94]. The dislocation density measured at the surface of the SiGe buffer in the aforementioned work was reported to be 2 × 10^6 cm^{-2}. In comparison, GaAs/AlGaAs quantum dot laser diodes epitaxially grown on Ge/Si substrates have surpassed 2100 hours of cw operation at 30 °C under an applied current density of 2 kA/cm^2 before the aging process was stopped for characterization (see Fig. 15.17) [95].

Table 15.3 summarizes some representative lifetime data that have been reported for GaAs based lasers grown on silicon to date. Compared to previous GaAs based QW lasers, InAs/GaAs quantum dot lasers show significantly longer lifetimes at harsher operating conditions, despite having a higher dislocation density compared to some of the QW devices. The improved lifetime is attributed to the same princi-

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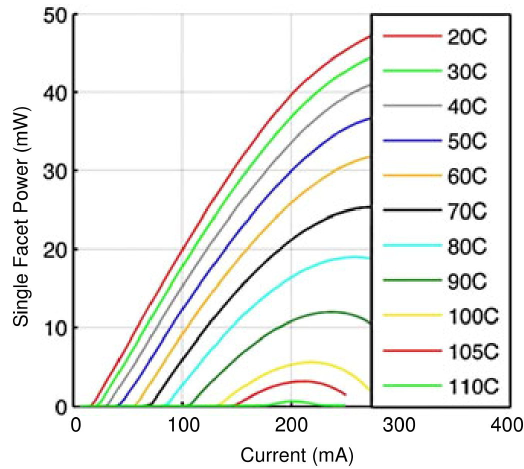

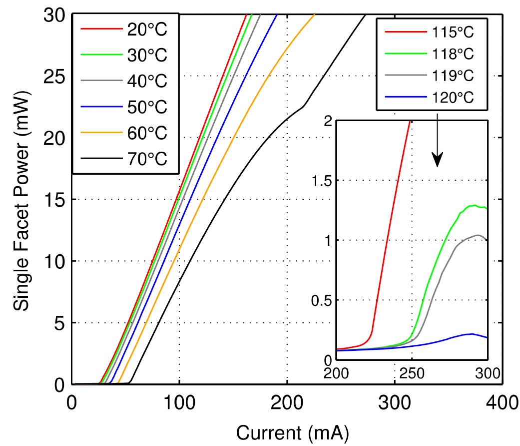

Fig. 15.15 (**a**) Room temperature cw light-current (LI) plots of the device in Fig. 15.14(a) at various stage temperatures showing lasing up to 110 °C. (**b**) LI-plot of a similar sized device (993 × 5 μm^2) but with p-doped active region, demonstrating lasing up to 119 °C [85]

ple that enables the operation of quantum dot lasers despite high defect/dislocation densities, namely that once carriers are captured by a quantum dot they become localized and can no longer diffuse laterally toward dislocations, unlike the QW case. If the dot density significantly exceeds the dislocation density, then the capture cross-section of individual dislocations or defects acting as non-radiative recombination centers is reduced due to competing radiative transitions of the quantum dot ensemble. The net result is a reduction of the non-radiative recombination rate resulting in improved device lifetime. Further, the strain field of the InAs quantum dots presents an additional mechanical barrier for the propagation of growing dislocation loops, and some loops may become pinned by the dots [89]. We expect that future work combining state-of-the-art dislocation reduction techniques, as well as improved uniformity and density of the quantum dot active region, will result in significantly improved laser performance and in particular improved laser reliability.

The following two sections describe more mature technologies, to fabricate high performance transmitters on silicon, which have advanced closer to production and anticipated to appear in the telecom/datacom market in the next few years.

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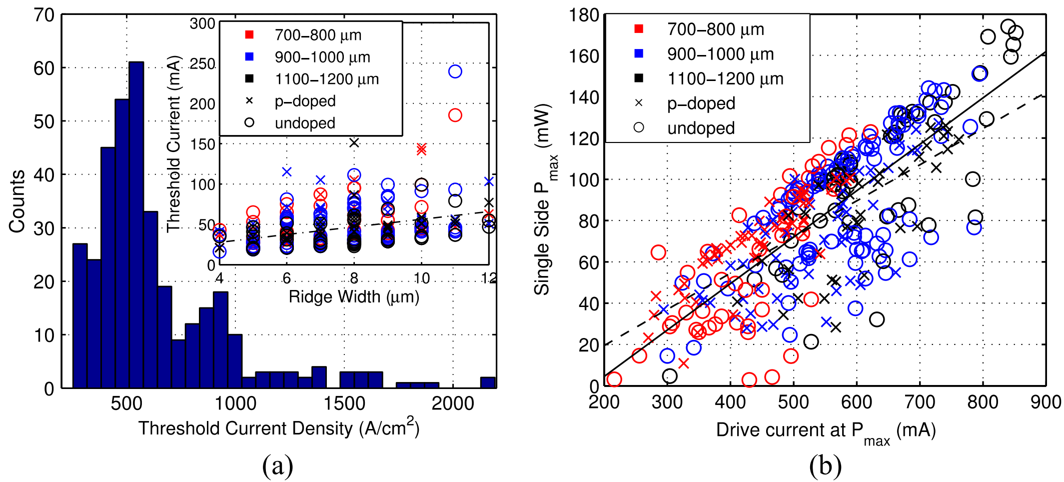

Fig. 15.16 (**a**) Histogram of cw threshold current density at 20 °C for 7-layer quantum dot lasers epitaxially grown on Ge/Si substrates with 95% HR coating on one facet with either intrinsic or p-doped active regions. *Inset*: corresponding threshold currents plotted against ridge width, the *dashed* best fit *line* has a slope of 4.75 mA/μm. (**b**) Maximum cw output power at 20 °C versus corresponding drive current. *Solid* and *dashed lines* are best fits for the undoped and p-doped devices with slopes of 22.52 and 17.52 W/A, respectively [85]

Table 15.3 Summary of representative lifetime data for GaAs based lasers grown on silicon

Year	Description	Aging condition	$J(0)/P(0)$	Dislocation density (method used)	Longest time to failure[a]	Ref.
1987	GaAs/AlGaAs SQW	RT APC	–/2 mW	10^7 cm^{-2} (–)	<10 s	[90]
1991	$In_{0.05}Ga_{0.95}As$/AlGaAs SQW	RT APC	~2000 A/cm^2/2 mW	–	10 hours	[91]
2000	$In_{0.2}Ga_{0.8}As$ “quantum dot like” active region	RT APC	1320 A/cm^2/0.5 mW	–	80 hours[b]	[92]
2001	GaAs/AlGaAs SQW on ELO stripe	RT APC	810 A/cm^2/1 mW	2×10^6 cm^{-2} (etch pits)	200 hours	[93]
2003	GaAs/AlGaAs SQW on Ge_xSi_{1-x}/Si	RT ACC	270 A/cm^2/<1 mW	2×10^6 cm^{-2} (PVTEM + etch pits)	4 hours[b]	[94]
2014	InAs QDs on Ge/Si	30 °C ACC	2000 A/cm^2/16.6 mW	2×10^8 cm^{-2} (PVTEM)	4600 hours (extrapolated).	[95]

[a]Time to failure is defined either by 2× increase in drive current in APC mode, 2× increase in threshold in ACC mode

[b]Actual catastrophic failures [95]

Acronyms: ACC: automatic current control, APC: automatic power control, PVTEM: plain-view TEM

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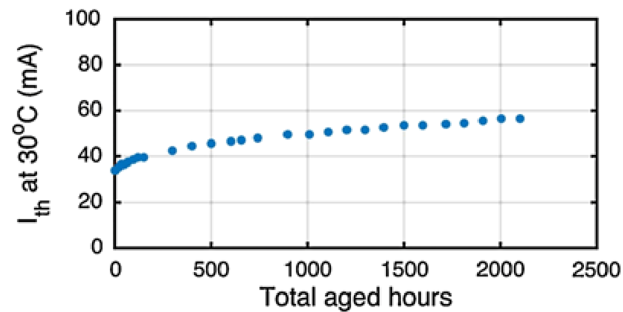

Fig. 15.17 Threshold current (cw) at 30 °C aging temperature of versus aging time for one of the InAs quantum dot lasers epitaxially grown on Ge/Si substrates reported in [85]

15.2.5 Hybrid (Assembly-Level) Integration

In Sects. 15.2.1–15.2.2 we reviewed a few of the major efforts to make silicon lase by manipulating the material properties of silicon or by utilizing other physical mechanisms to obtain optical gain. Recent progress in monolithic integration of direct bandgap materials on Si substrates is also highlighted in Sect. 15.2.3, though the lasing efficiency requires significant improvement. Although much progress has been made in this area and optically pumped Si Raman lasers have been demonstrated, room temperature electrically pumped lasers with useful powers for optical communication applications have not been demonstrated. Hybrid integration is a promising approach where III–V compound semiconductors are used to provide electrically pumped gain and are coupled into passive lightwave circuits on silicon.

The traditional approach to hybrid integration is to take prefabricated III–V lasers and amplifiers and die bond these elements onto a passive planar lightwave circuit (PLC). Since the waveguides on the host substrate, the PLC, and the laser die are already defined, the alignment accuracy during placement needs to be a fraction of the mode width. This is typically within a few hundred nanometers for silicon waveguides, making alignment a challenge for high volume manufacturing and leading to substantial variation in coupling power and back reflections between the two waveguides. Efforts have been made to reduce the sensitivity of this coupling by increasing the mode size through spot size converters [99]. Precision cleaving the III–V active die and creating a perfectly matched trench in the PLC host substrate have been explored in order to create assembly methods that allow for self alignment of the optical modes [100].

Figure 15.18 illustrates a PLC utilizing hybrid integration for switching [101]. In this work, self alignment with ± 1 μm precision is achieved by placing solder-wettable pads on both the host PLC substrate and the III–V chips. During bonding, the surface tension of the Au–Sn solder bumps pulls the two chips into alignment. This demonstration yielded coupling losses of $4 \sim 5$ dB when used with spot size converters. However, the production efficiency and chip yield result in expensive integration cost. Another noteworthy tunable laser demonstration using this technique was published by NEC recently [102]. The laser included individual InP and Si chips assembled to achieve gain and filtering/tuning functionality, respectively. The laser had full C-band tunability with fiber coupled output power in excess of 100 mW. The linewidth across the entire wavelength range was around 15 kHz.

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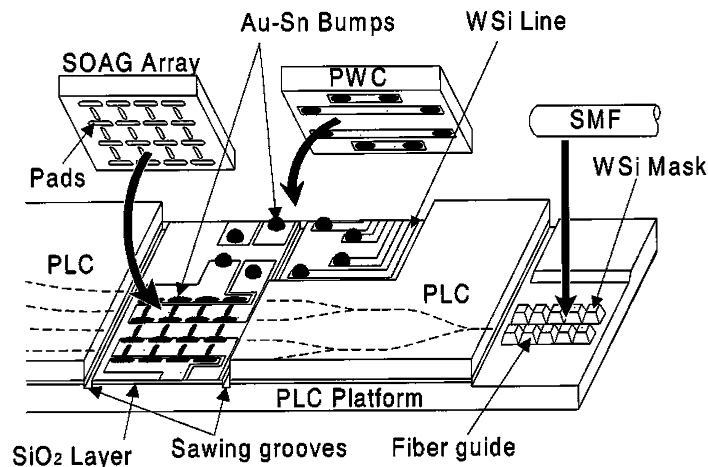

Fig. 15.18 Schematic of proposed hybrid integration scheme for switching [101]. SOAG: semiconductor optical amplifier gate, PWC: printed wiring chips (reproduction under the permission of Institute of Electrical and Electronic Engineers)

The following section includes a wide variety of high performance photonic devices, which were demonstrated by bonding III–V layers onto SOI prior to laser fabrication.

15.2.6 Heterogeneous (Wafer-Scale) Integration

A new heterogeneous integration methodology is the transfer of thin crystalline III–V films onto an SOI host substrate. The silicon is typically patterned prior to the transfer, and the III–V films are processed after transfer allowing for the use of standard lithography-based patterning techniques used to fabricate III–V lasers. The alignment of the optical modes is determined by the lithography, which allows for an extremely repeatable fabrication process and coupling efficiencies near ∼1 dB between the III–V regions and the passive silicon regions as demonstrated by Park et al. [103]. The following section will focus on the new heterogeneous platforms and devices.

Direct wafer bonding is commonly used to mate lattice mismatched semiconductors such as AlGaAs and GaP for high power LEDs, InGaAsP, AlAs and GaAs for improved mirror reflectivity in long wavelength VCSELs, and InGaAsP and AlGaAs for high characteristic temperature T_0 lasers [104]. This process consists of a thorough cleaning of the sample surface to remove all semiconductor particles that were generated during dicing or cleaving as well as all organics on the surface. Next a chemical surface treatment is employed to remove any surface native oxides or other stable surface states. The samples are then placed in physical contact with each other and undergo spontaneous bonding and are held together with Van der Waals forces. This bond is relatively strong, depending on the two material systems being bonded, but is further strengthened through a high temperature anneal (typically 600 °C or higher) while applying pressure on the bonded sample. The high temperature anneal results in the formation of covalent bonds at the bonded interface, while the pressure on the sample compensates for any waviness or surface roughness and ensures greater surface area contact between the two materials.

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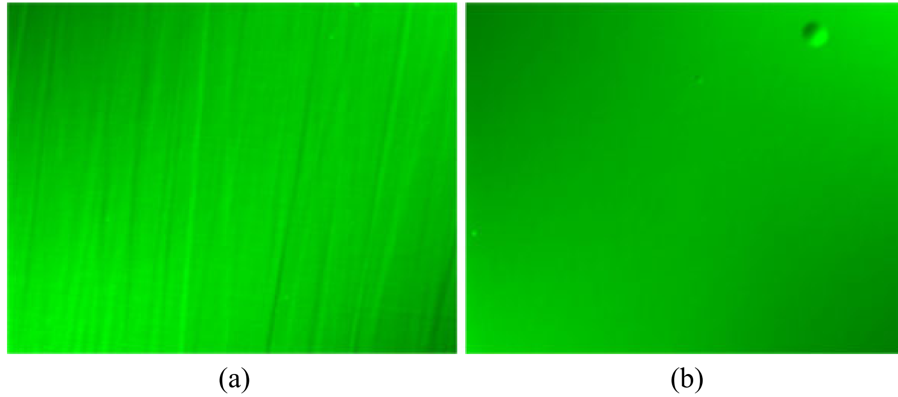

Fig. 15.19 Nomarski microscope images, showing the surface roughness of the transferred III–V surface at bonding temperatures of (**a**) 600 °C and (**b**) 250 °C

The substrate of one of the material systems is then removed by using a wet etch resulting in the transfer of one epitaxial layer structure to another.

The difference in the thermal expansion coefficient of silicon ($\alpha_{Si} = 2.6 \times 10^{-6}$/K) and InP ($\alpha_{InP} = 4.8 \times 10^{-6}$/K, cf. Table 15.1), thermal damage, and doping diffusion pose a large challenge for achieving high quality with active region transfer to silicon through direct wafer bonding. As samples cool down from 600 °C to room temperature, the InP begins to fracture since the thermal stress built up was larger than the fracture energy of the InP. Mild success in preserving the III–V material can be achieved by thinning the substrate of the InP to ∼150 μm between the spontaneous bonding step and high temperature anneal steps. The thinned III–V materials conform more easily to the silicon without accumulating enough stress to fracture the III–V but show cross hatching and material waviness in the transferred III–V materials (Fig. 15.19(a)). Figure 15.19(b) shows a Nomarski mode microscope image of the top surface of an InAlGaAs active region layer structure transferred to silicon after 250 °C anneal. The Nomarski mode of the microscope shows the polarization dependence of the surface reflection and is useful for seeing surface particles and roughness.

The thermal mismatch stress σ of the bonded wafers is given by:

$$\sigma = \frac{E}{1 - \upsilon^2} \left(\frac{\frac{E_{InP}}{1-\upsilon_{InP}^2} \alpha_{InP} h_{InP} + \frac{E_{Si}}{1-\upsilon_{Si}^2} \alpha_{Si} h_{Si}}{\frac{E_{InP}}{1-\upsilon_{InP}^2} h_{InP} + \frac{E_{Si}}{1-\upsilon_{Si}^2} h_{Si}} - \alpha \right) \Delta T \qquad (15.9)$$

where α is the thermal expansion coefficient, h is the thickness of the substrate, E is Young's modulus, ν is Poisson's ratio, and ΔT is the difference between the bonding temperature and room temperature. The critical stress $\tau_{critical}$ required to generate dislocations in InP is empirically formulated by Pasquariello et al. using the theory of stress induced dislocation generation [105] as:

$$\tau_{critical} = 898 \exp\left(\frac{5934}{T} \right) \qquad (15.10)$$

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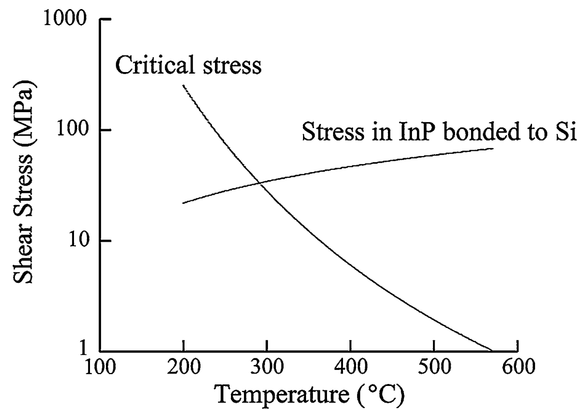

Fig. 15.20 Critical dislocation generation stress in InP and sheer stress between InP bonded to silicon vs. temperature [106] (reproduction under permission of the Institute of Electrical and Electronic Engineers)

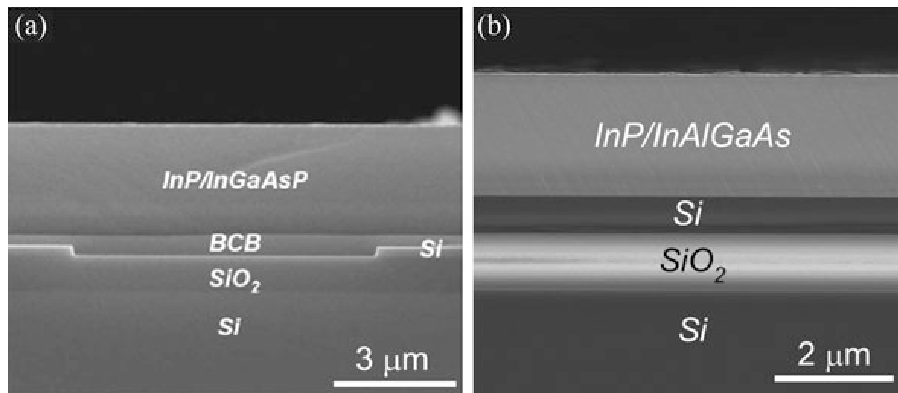

Fig. 15.21 SEM cross-sectional images of (**a**) DVS-BCB [107] and (**b**) LTOPA [108] bonding to integrate InP thin epitaxial films on an SOI substrate

Figure 15.20 shows a plot of the critical stress and the sheer stress as a function of temperature. In order to prevent the generation of dislocations in the InP, the bonding temperature must be kept below 300 °C. Two low-temperature III–V film transfer approaches have been used to yield electrically pumped lasers on silicon. The first uses polymers such as divinyl-tetramethyldisiloxane-benzocyclobutene (DVS-BCB) as a 300 nm thin adhesive layer between the III–V region and the waveguide as shown in Fig. 15.21(a) [107], and the second uses low-temperature oxygen plasma-assisted (LTOPA) wafer bonding where the interfacial oxide with around 15 nm thickness is too thin to be seen in the SEM image of Fig. 15.21(b) [108]. Detailed studies of polymer-based and LTOPA bonding can be found in [109] and [110], respectively. The transferred InP-based epitaxial thin film acts as a gain medium to generate photons when carriers are injected optically or electrically. Then the light can be evanescently coupled into the SOI waveguide underneath as long as the interface material (i.e. polymer or oxide) is sufficiently thin.

Figures 15.22(a) and (b) are the LTOPA wafer bonding-based heterogeneous silicon evanescent platform (HSEP) cross-sectional schematic and SEM image, showing a heterogeneous waveguiding structure formed by bonding III–V epitaxial layers onto the SOI substrate. The typical anneal temperature is kept at 300 °C in all devices made on this platform and discussed in this section. The small index differ-

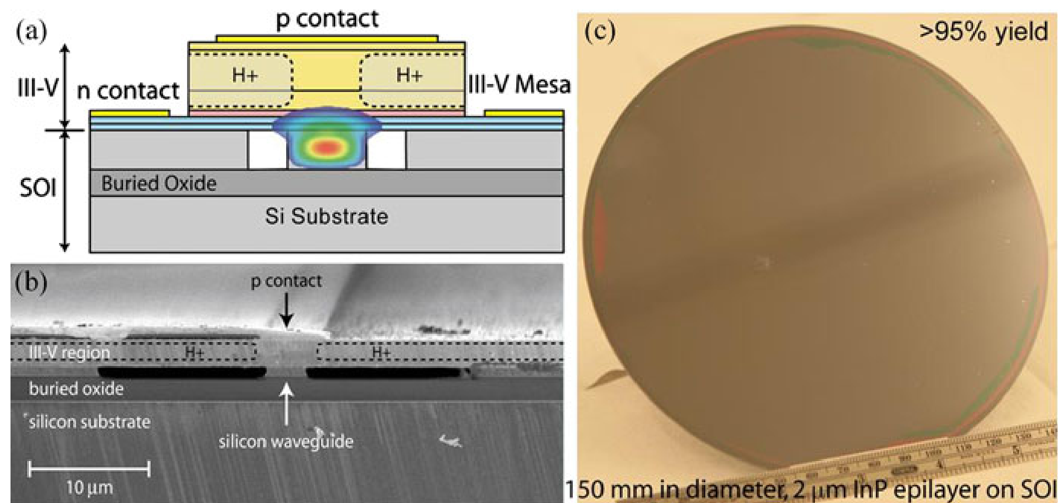

Fig. 15.22 (**a**) Cross-sectional schematic and (**b**) SEM image of heterogeneous Si evanescent platform [108]; (**c**) 150 mm diameter, 2 μm thick InP epitaxial transfer on SOI with >95% yield [112]

ence between Si and III–V materials enables a large freedom in manipulating modal confinement in Si and the III–V semiconductor, which is realized by adjusting the III–V layer thickness, the SOI waveguide dimension [111], and the rib etch depth. The large index contrast for SOI waveguides can tremendously reduce the chip size and power consumption and enhance the integration complexity and yield. Unlike the conventional flip-chip die bond to place discrete active components on passive chips, HSEP eliminates effort and loss in alignment and modal mismatch and literally millions of devices can be made with one bond. Proton implantation in III–Vs creates a current flow channel resulting in good gain and optical mode overlap. Scale-independent integration [110] is demonstrated up to the presently largest InP substrates of 150 mm in diameter in Fig. 15.22(c) [112]. No degradation in bonding quality or increase of processing complexity was observed as the process was scaled up to 150 mm, indicating the possibility for low-cost mass production. Bonding and III–V device back-end processing, both conducted at temperatures less than 350 °C, are completely CMOS-compatible.

Since the first demonstration of epitaxial III–V layer transfer onto SOI, there have been several lasers fabricated with various designs for different applications. Distributed feedback (DFB) lasers [113–115], distributed Bragg reflector (DBR) lasers [116, 117], microring/microdisk lasers [118, 119], arrayed waveguide grating (AWG) multi-wavelength lasers [120, 121], and tunable lasers [122, 123] are some of the prominent laser designs demonstrated in this platform. Figure 15.23 shows an SEM image of an electrically pumped heterogeneous silicon DFB laser along with its optical spectrum. A recent result [124] showed a 200 μm long DFB laser with low threshold current of 8.8 mA and achieved 12.5 Gb/s data transmission using direct modulation. A more compact DFB laser design, using hyperbolic materials, for optical interconnect applications is discussed in [125]. Microring lasers with 50 μm diameter and threshold current <5 mA have also been reported [126], and sub-mA threshold operation has been demonstrated in a DVS-BCB (divinylsiloxane-bis-

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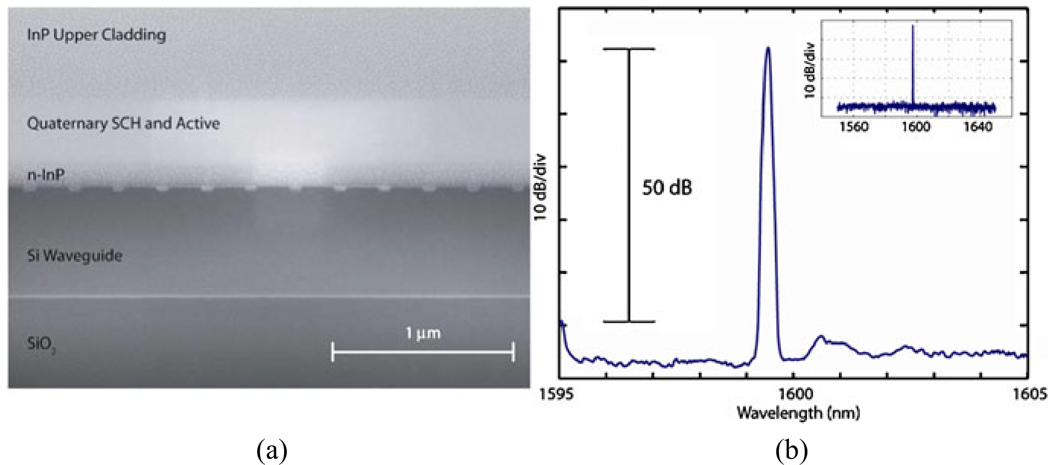

(a) (b)

Fig. 15.23 (**a**) SEM image of longitudinal cross-section of heterogeneous Si DFB laser; (**b**) optical spectrum showing 50 dB of side-mode suppression. *Inset* illustrates single mode lasing over 100 nm span [113]

benzocyclobutene) bonded disk laser with 7.5 μm disk diameter by Van Campenhout et al. [119]. All these results show promise of dense on-chip laser integration for high bandwidth intra-chip communication with low power consumption.

Heterogeneous integration on the one hand helps to reduce the cost of an individual laser due to increased wafer size, and on the other hand can also enable novel laser designs that use more than one photonic element to improve the laser characteristics for a specific application. The photonic circuit techniques described here can evolve in parallel with material advancements and can be optimized separately. We will discuss one example of such a circuit technique to reduce the laser linewidth. The linewidth of a semiconductor laser can be reduced significantly by reducing the loss of the optical cavity and by reducing the confinement factor, which is defined as the ratio of the carrier confined volume to the volume occupied by the photons in the laser cavity. The confinement factor can be further approximated as a product of confinement factors for each of the laser dimensions, viz. lateral, transverse and longitudinal confinement factor.

A narrow linewidth heterogeneous DFB laser on silicon was recently realized by reducing the loss and transverse confinement factor of the optical mode. This was achieved by designing a high-Q hybrid resonator with a grating in silicon to reduce the optical losses so that very little modal overlap with the pumped quantum wells was needed to provide gain. The high-Q silicon resonator is fashioned from a silicon waveguide patterned with a 1D grating (see Fig. 15.24(a)). Coupling to radiation modes is minimized via a bandgap-modulated defect section in the middle, over a spatial width marked as L_d in Fig. 15.24(a), with uniform grating reflectors of length L_m on either side. The defect is designed directly in the frequency domain by parabolically modulating the lower-frequency band edge of the grating as a function of position localizing a resonant mode with a Lorentzian profile in both real and reciprocal space along the resonator (Fig. 15.24(b)). The lowest measured linewidth reported for this laser structure is 18 kHz, as shown in Fig. 15.24(c) [127].

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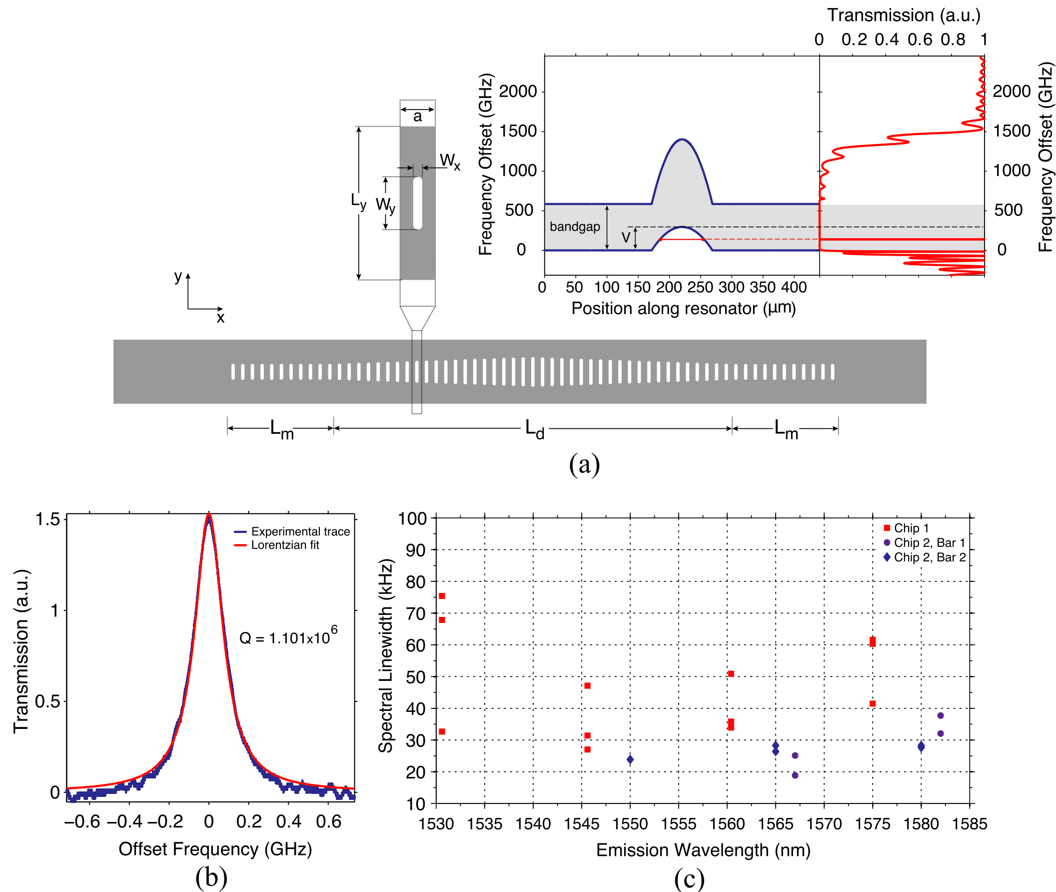

Fig. 15.24 (**a**) Schematic top view of grating in silicon along with spatial band structure of high-Q hybrid resonator plotted against simulated transmission spectrum. (**b**) Experimental trace and Lorentzian fit of transmission resonance of high-Q silicon resonator. (**c**) Distribution of spectral linewidths of high-Q hybrid lasers as a function of emission wavelength [127]

It is expected that this linewidth can be improved even more by further reduction of the transverse confinement factor by lowering the number of quantum wells and/or increasing the spacer oxide thickness between the III–V epitaxial layers and silicon.

Linewidth reduction of tunable lasers can also be achieved by decreasing the longitudinal confinement factor (as detailed in [128]). One corresponding implementation consists of a short active section coupled to a longer passive section by a semitransparent mirror (e.g. 60% reflectance), where wavelength tuning is achieved using two silicon waveguide based cascaded ring resonators with slightly different diameters. This monolithic tunable diode laser showed a linewidth <100 kHz over 54 nm tuning range near the O-band (see Fig. 15.25(b)) [128]. Further optimization of the filter design and the back mirror reflectivity can improve the linewidth even further. Altogether, these heterogeneous integration schemes show great promise with respect to realizing novel photonic integrated circuits which offer superior laser characteristics combined with small size, low weight, low power consumption and attractive cost.

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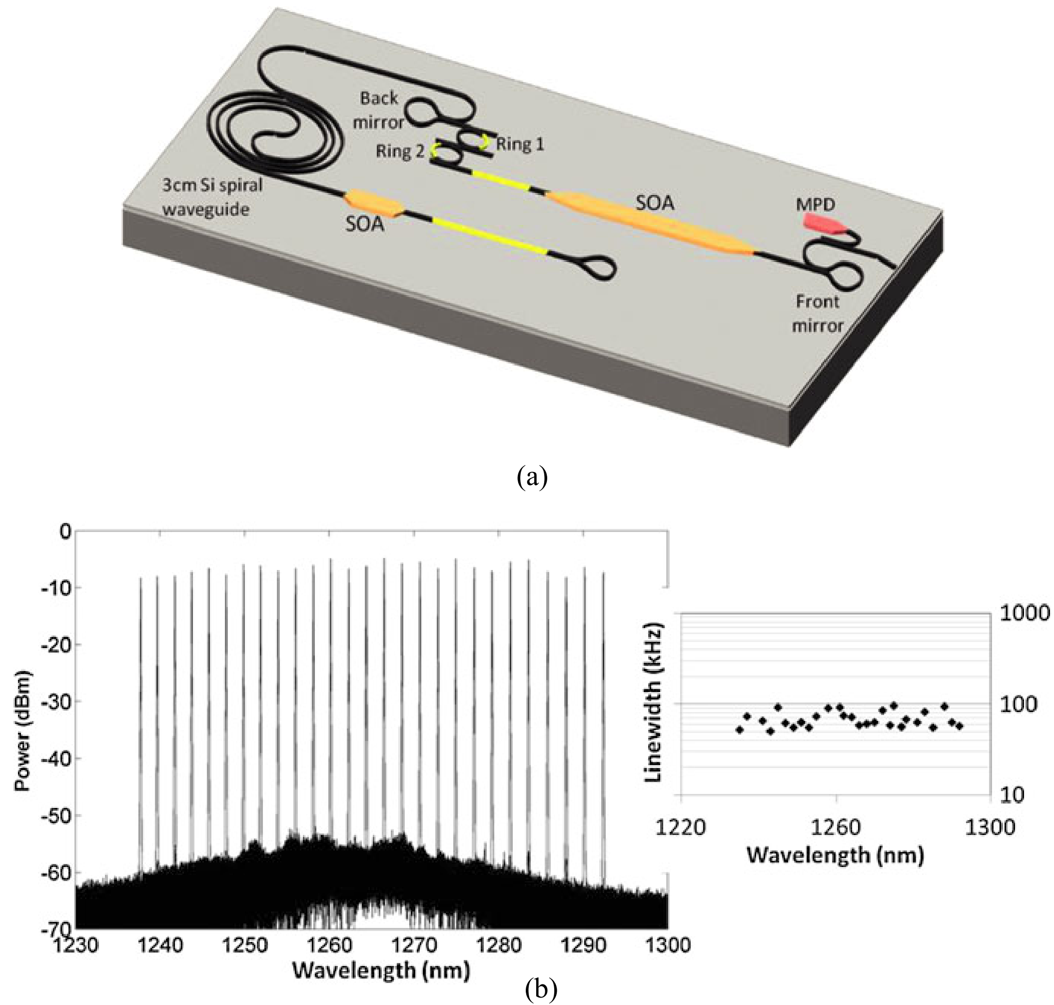

Fig. 15.25 (**a**) Schematic view of tunable laser design with integrated external cavity. Tuners are *yellow* (two phase sections and two rings for wide tuning), and SOAs are *orange* (one is the laser active section, and one is used as an ON/OFF switch or to control the level of feedback). The monitor photodiode (MPD) is used to measure the laser output power for adjustment of laser parameters. (**b**) Overlapping spectra showing >54 nm tuning range with SMSR >45 dB (resolution bandwidth: 0.02 nm ≅ 2.5 GHz) along with the corresponding measured linewidth [128]

15.2.7 Industrial Development and Commercialization

While it has been a research interest to enable a Si-based light source in academia for decades, industry has sped up the pace in R&D and commercialization over the past 15 years, aiming to progress along the lines of Moore's law. In this section, we review the mainstream technology, near-future and long-term trends and highlight some related recent research results to enable an on-chip Si laser for datacom and telecom applications.

The first successful commercialization route was to take prefabricated III–V lasers, either edge-emitters or VCSELs, and amplifiers and die bond these elements onto a passive planar lightwave circuit (PLC), e.g., silica-based PLC initially and

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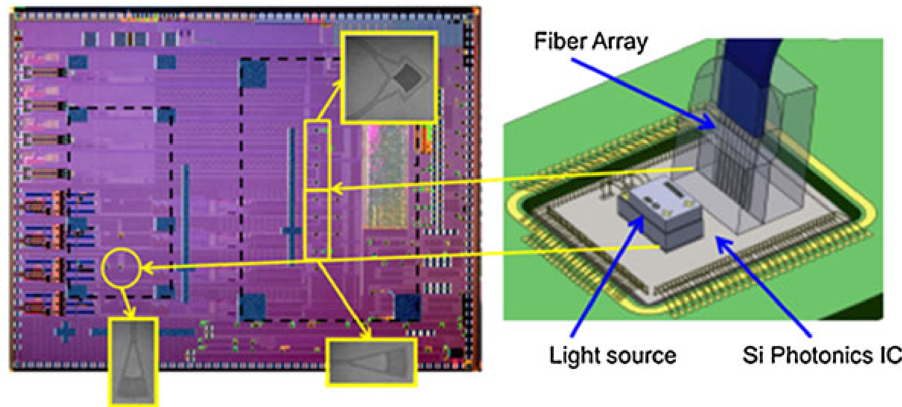

Fig. 15.26 Luxtera Si photonic transceiver chip photograph and packaging cartoon with laser module and optical fiber assembly attached to the top surface of Si CMOS photonics die [129]. Courtesy of Luxtera

shifting to CMOS Si PLCs right now. This solution provides an optical carrier with high power capability and state-of-the-art performance with low threshold current, low relative intensity noise (RIN) and high wall-plug efficiency [130, 131]. It also relies on mature devices and allows the prescreening of the lasers before assembly to ensure good reliability. Therefore, it has been the mainstream approach for photonic interconnect products in the current market. Figure 15.26 are a photograph of a Luxtera's 40 Gbit/s transceiver product chip and packaging cartoon showing a cw DFB laser module flip-chip bonded on a Si CMOS photonic chip [129]. The cw laser output is sent into the CMOS photonic chip through near-vertical couplers based on diffraction gratings, and split into 4 streams to feed 4 independent MZI modulators. The company's newest 4 × 26 Gbit/s transceiver module still employs a similar architecture as the previous 4 × 10 and 4 × 14 Gbit/s products, showing data handling expandability [132].

In addition to grating couplers, edge coupling via a spot size converter is another popular approach. Though it takes more fabrication effort to make a spot size converter than a grating coupler, a spot size converter has the advantage of a much larger optical bandwidth than a grating coupler. Figure 15.27(a) shows the schematic of a III–V diode laser die flip-chip bonded onto the Si substrate of an SOI wafer and output aligned with a spot size converter in the Si waveguide [133]. The 600 μm-long FP laser cavity is defined by two as-cleaved facets. In order to keep the excess loss within 1 dB, the offset in the lateral direction needs to be less than ±0.9 μm. This value can be improved up to ±1.5 μm by tapering the overcladding layer to an input width of 8 μm. In the vertical direction, the offset has to be less than ±0.4 μm, which leads to a tight control of III–V substrate and AuSn thickness. The reported throughput is about 60 chips/hour [133]. Taking account of the alignment accuracy of the flip-chip bonding machine, the coupling efficiency is estimated to be 35% in the worst case and 85% in the best case based upon a theoretical investigation, similar to the efficiency of grating couplers. However, this integration scheme gains an advantage in better thermal management. As reported in the literature and to be

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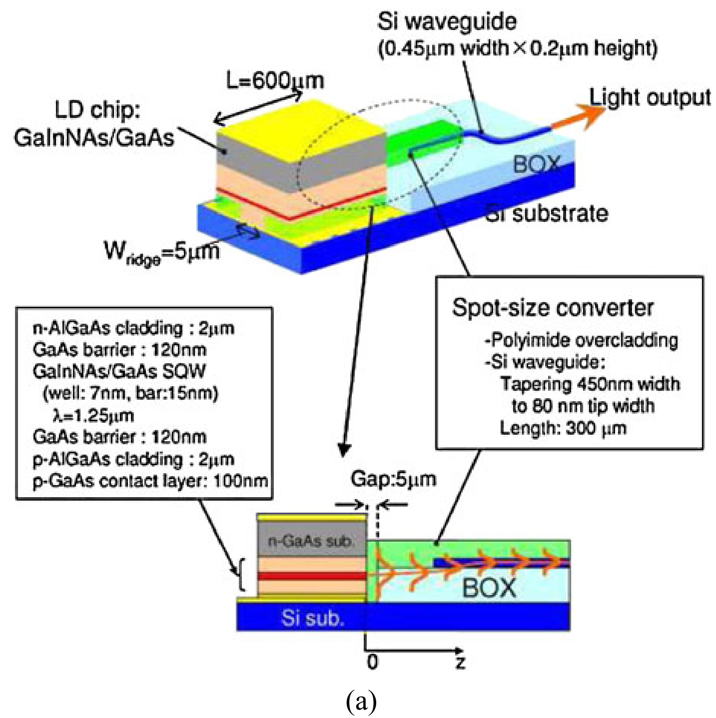
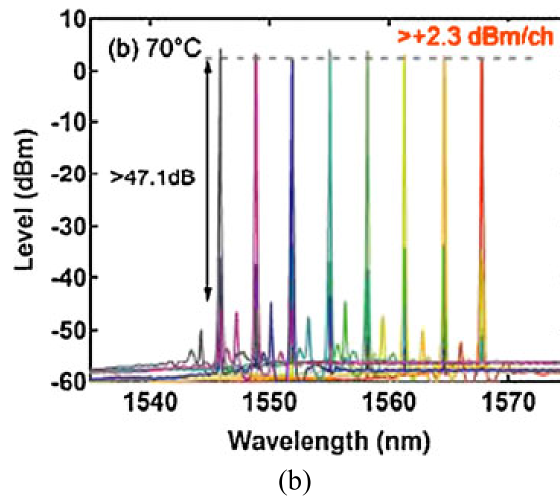


(a)



(b)

Fig. 15.27 (**a**) Schematic illustration of laser diode chip integrated on Si waveguide with spot-size converter [133]. (**b**) 8-λ superimposed spectrum of flip-chip bonded AlGaInAs DFB laser array under 100 mA × 8 channel simultaneous operation at 70 °C [136]

discussed in more detail later in this section [134, 135], heat dissipation in III–V-on-SOI structures is a serious problem for device performance and can pose a reliability issue as well. The thick BOX layer blocks the heat from the III–V junction, so TEC cooling at the Si substrate is of very little use. By partially removing the top Si layer and the BOX layer, the III–V die can get direct contact with the Si substrate through a thin AuSn layer which ensures efficient heat dissipation. An impressive characteristic temperature (T_0) of 132 K was therefore obtained from a GaInNAs-based QW structure with 1250 nm emission wavelength [133]. Very recently an 8-channel multi-wavelength hybrid laser array was also demonstrated based upon the same platform (Fig. 15.27(b)) [136]. Benefiting from high-performance InAlGaAs-based

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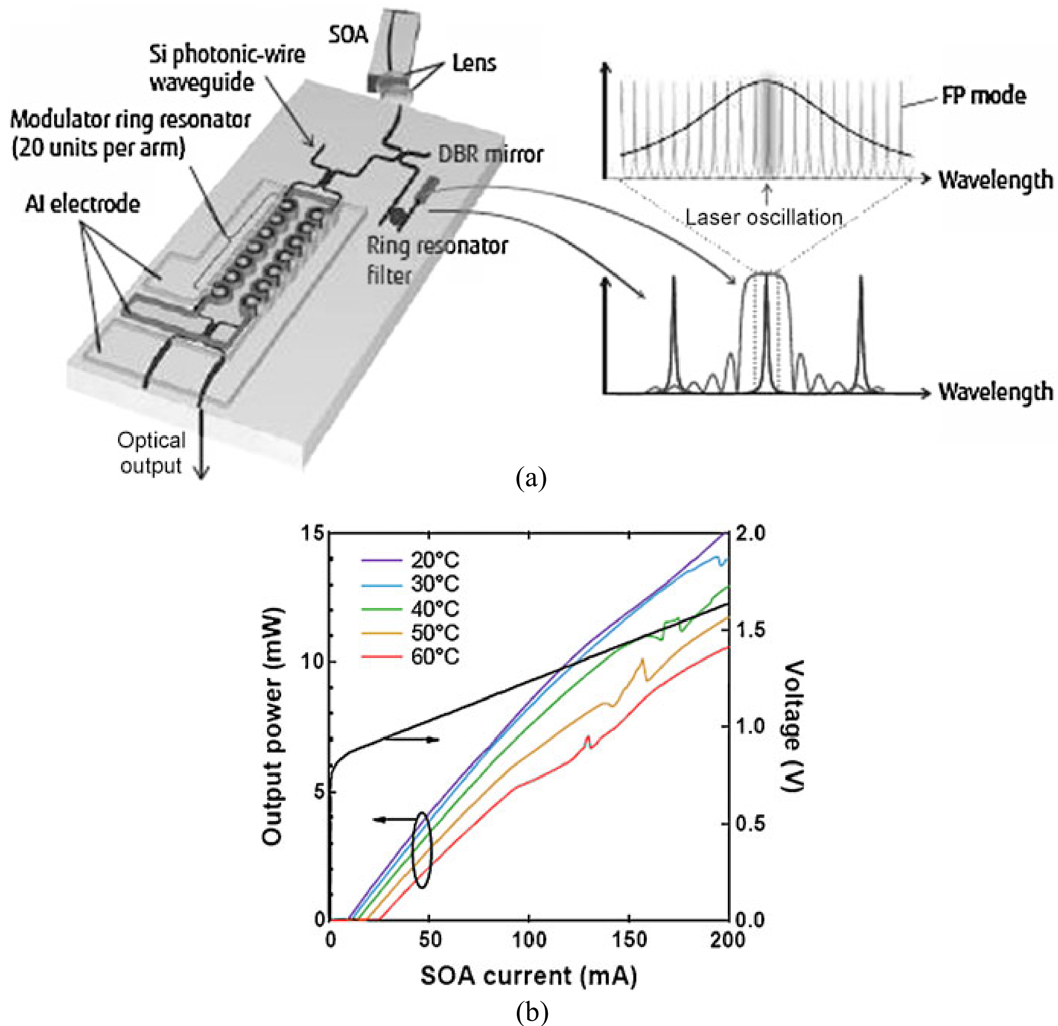

Fig. 15.28 (**a**) Structure of integrated optical transmitter and laser wavelength selection mechanism [137], (**b**) temperature-dependent light-current-voltage (LIV) characteristics of Si hybrid laser [138]

DFB laser arrays, the lasing wavelength is pushed to the 1550 nm window, and the hybrid chip shows excellent spectral characteristics even at 70 °C.

Figure 15.28 illustrates a similar design which takes advantage of the same good heat dissipation principle, however, the III–V part is only an SOA which provides optical gain, and a FP laser cavity is defined by the high-reflection facet of the SOA and a Si DBR mirror in order to achieve single wavelength emission and wavelength tunability [137, 138]. As Fig. 15.28(a) shows, a properly designed DBR limits the reflector bandwidth to less than a FSR of the microring resonator so that single-wavelength emission is assured, and also allows some microring resonance shift due to fabrication imperfection and environment change. Furthermore, since both the DBR and the microring are pure Si components and in close physical proximity, the temperature shift tends to move the DBR reflection band and ring resonance by about the same amount, so that only very little (or even zero) tuning effort is

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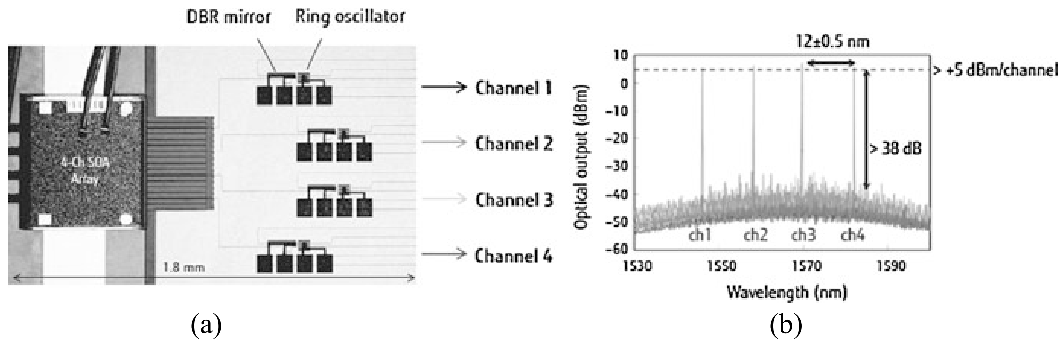

Fig. 15.29 (**a**) Microscopic image of a fabricated 4-ch Si hybrid laser array, (**b**) spectrum of 4-ch Si hybrid laser array [137]

required. The coupling between the SOA die and the Si waveguide does also rely on a spot size converter. Si waveguide components have typically lower loss than III–V counterparts, so they can be fabricated in well-controlled CMOS technology, and as a consequence can lower the laser's cost. Figure 15.28(b) shows the temperature-dependent LIV characteristics of this flip-chip bonded Si hybrid laser [138]. The threshold current is as low as 9.4 mA at 20 °C and 25 mA at 70 °C, and a good wall-plug efficiency (WPE) from 7.6 to 4.5% in this temperature range is also achieved.

A hybrid CWDM laser array was also demonstrated recently based upon a large gain bandwidth SOA chip [137]. Figure 15.29(a) shows the fabricated 4-channel device with an SOA size of 1.8×1.1 mm^2. The same microring resonator is used for each channel and their FSR is designed to be around 12 nm. Each Si DBR is designed differently so that each Bragg wavelength coincides with one of the consecutive microring resonances. Figure 15.29(b) demonstrates the lasing spectra showing four well-defined lasing peaks with over 5 dBm output for each channel and 38 dB side-mode suppression ratio [137].

Besides Luxtera, Acacia Communications is another company employing the external coupling approach for 100G+ metro solutions. Their transceivers consist of a coherent silicon photonic integrated circuit, which is co-packaged with a low power ASIC/DSP chip and an external laser. The laser serves as the input to the modulators and as the local oscillator for the receiver as well [139]. The company has been shipping 100G C form-factor pluggable (CFP) PM-QPSK transceivers with total power consumption of <24 W for the whole package and has recently announced a new 400G transceiver module set to ship later in 2015.

Since CMOS foundries normally do not allow any non-CMOS compatible ("exotic") materials into their fabrication line, packaging III–V dies, either fabricated lasers or optical gain chips, with a Si photonic chip in the backend process is a logical first step to realize a reliable silicon photonics light source. However, inevitable loss and reflection at the coupling interfaces, moderate fabrication efficiency, considerable cost of the chip alignment step, and conflicting demands of small dimensions of the III–V material based devices vs. minimum III–V chip size required for reliable handling during packaging (resulting in inefficient III–V real estate usage) all limit the long-term competitiveness of this approach in the fast

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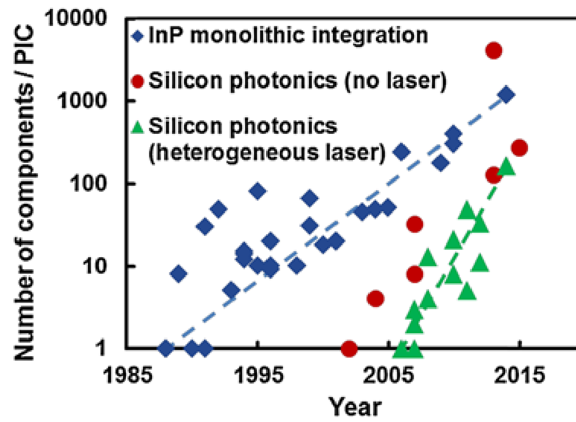

Fig. 15.30 Development of chip complexity measured by the number of components per chip for InP-based photonic integrated circuits (*blue*) and silicon based integration distinguishing PICs with no laser (*red*) or with heterogeneously integrated lasers (*green*), which fit to exponential growth curves (*dashed*) [145]

growing Si photonics market. The new heterogeneous approach discussed earlier in this chapter (see Sect. 15.2.6), which is based upon the transfer of a III–V epitaxial layer onto a Si photonic chip by direct wafer bonding and subsequent definition of the device structure, is a more attractive solution [107, 108, 140, 141]. Among industrial companies Intel had taken a leading position in the execution of early advanced research and later product commercialization. In 2010 Intel demonstrated a 50 Gbit/s heterogeneous transceiver based on 4-transmitter channels with 12.5 Gbit/s Si MZI modulators fed by four heterogeneously integrated DBR lasers, and four Ge-based photodetectors in the receiver [142]. Three years later, Intel announced engineered samples of 100 Gbit/s Si photonics modules with heterogeneously integrated lasers [143]. HP recently launched a program called "The Machine", in which photonic interconnects will eventually replace conventional copper cable and provide low-power consumption, high-speed data transmission between a new generation of computing cores and memories [144]. Heterogeneously integrated Si lasers are likely to serve as the optical engines in this photonic interconnect system.

Since the first demonstration of the heterogeneous device platform in 2005 [146], there has been an extremely fast progression in both advanced research and product engineering [141]. Figure 15.30 indicates that the growth of the number of components/PIC in the heterogeneous Si platform doubles every year compared to 2.6 years for InP PICs [145]. The mature CMOS technology and profound knowledge database accumulated during decades of research on PICs for telecom applications fuel the acceleration in device design and fabrication. Highly improved yield, scaling potential and shorter processing time as demonstrated by recent studies of III–V-to-Si direct wafer bonding have paved the way for efficient mass production [110, 147]. Reliability has remained the last major concern, but fortunately, encouraging results were recently demonstrated from UCSB [148].

In the UCSB study, heterogeneously integrated Si DFB lasers similar to previously demonstrated DFB devices [113] were used. As it is known that superlattices can serve as effective buffer to block the propagation of threading dislocations in III–V-on-Si heteroepitaxy [58, 59, 149], similar superlattice structures were designed in the bonding III–V epitaxial layers. In order to the study whether potential bonding-induced defects at the III–V/Si interface would cause reliability issues,

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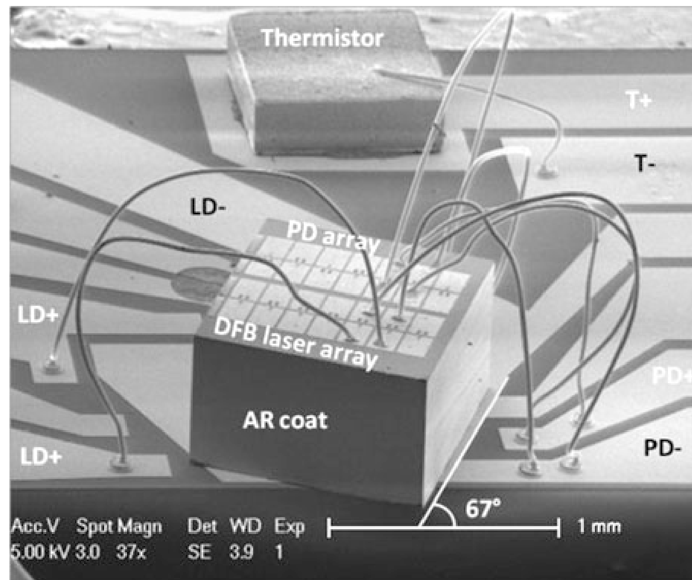

Fig. 15.31 Side-view SEM image of complete carrier used in aging test [148]

three epitaxial structures (A, B or C) with the following key characteristics (full details are given in [148])

- A: unstrained superlattice layers close to the bonding interface
- B: strained (−1% well, 1% barrier) superlattice layers close to the bonding interface
- C: control design with thicker n-InP layer to obtain similar heterogeneous optical mode profile

were transferred to pre-patterned SOI chips, and a total of 3000 laser diodes were characterized. Each laser diode was integrated with an on-chip photodetector to screen out defective lasers. The dimensions of a single die, comprising 300 laser diodes each, were 8 mm × 8 mm. Fourteen typical devices of each epitaxial structure were selected for aging tests. For that purpose the initial dies were further diced into smaller chips, each comprising of two lasers with the same grating design, waveguide facets were polished and AR coated, and a 7° angle for the output Si waveguide was chosen to minimize reflections. The dies were placed on ceramic sub-mounts using silver epoxy for good thermal contact. In order to collect light from a surface normal detector the dies were mounted at a 23° angle from normal using the flip-chip bonder. The devices were wire-bonded to the pads on the submount alongside a thermistor. An SEM image of a complete carrier is shown in Fig. 15.31 [148].

The aging tests were done at five different temperatures, viz. 25 °C, 50 °C, 60 °C, 70 °C and 85 °C while the devices were driven with 80 or 100 mA. Room temperature (25 °C) LI curves were taken at certain intervals during the aging test. The threshold current during the period of aging, at different bias conditions and temperature, is shown in Figs. 15.32(a)–(f). Regardless of design and aging conditions, most devices exhibited no significant degradation in this time period. Only two devices showed increased threshold with time at 70 °C. With 50% increase in threshold

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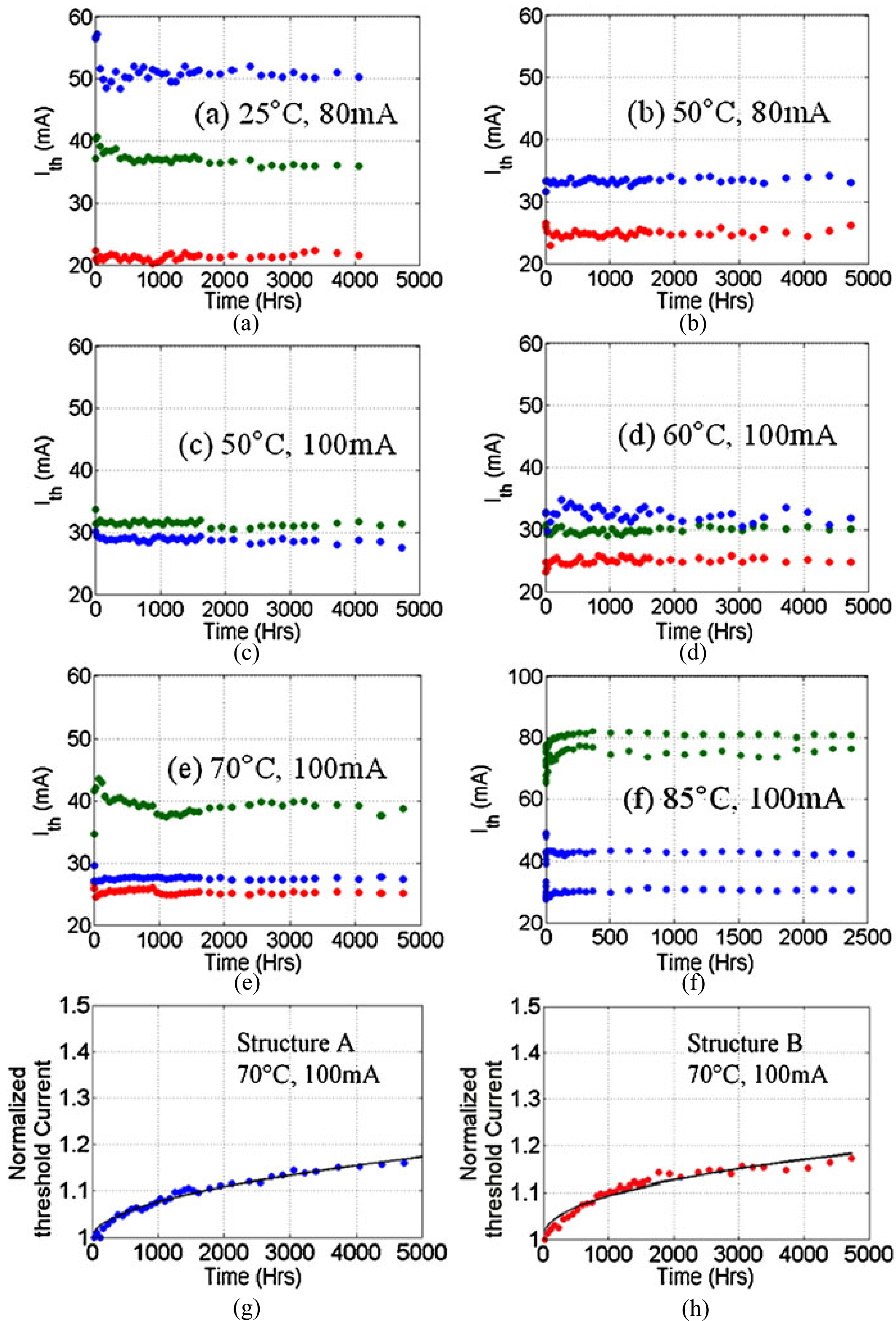

Fig. 15.32 (**a**)–(**f**) Threshold current of devices under various aging conditions – Structure A (*blue*), structure B (*red*) and structure C (*green*). (**g**), (**h**) Degradation data for two structures along with the sub-linear fit (*black*)

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as failure criterion, the two equations below are used for a sub-linear fit to evaluate the mean time to failure (MTTF):

$$I_{th}/I_{th}(0) = 1 + at^m \tag{15.11}$$

$$MTTF = \left(\frac{0.5}{a}\right)^{1/m} \tag{15.12}$$

where I_{th} and t are threshold current and aging time, respectively. The values for the fitting parameters a and m for the data shown in Figs. 15.32(g) and (h) are as follows: Structure A: $a = 0.004678$, $m = 0.43$ and structure B: $a = 0.002215$, $m = 0.51$. This corresponds to MTTF values, at 70 °C, of 49,000 hrs and 40,000 hrs for structures A and B, respectively. Due to insufficient lifetime of devices with structure C corresponding laser lifetimes could not be determined [148].

A subsequent TEM study on one of the failed devices did not reveal any sign of defect propagation towards the MQW active region, indicating that another failure mechanism, e.g., metal-semiconductor contact degradation, dielectric failure, etc. limits the lifetime of the selected device [148]. Additionally, no visible dark line defects were observed in a separate electroluminescence experiment. The reliability study is a necessary requirement en route to commercialization of heterogeneously integrated PICs and we conclude that the technology is suitable for making reliable active optical devices with lifetimes on par with commercially available semiconductor active devices.

High temperature performance of the laser is important, because operation at elevated temperatures cause a shift of the lasing wavelength, lowers the device efficiency, and limits the direct modulation bandwidth. The thermal resistance is strongly influenced by the thick (typically 800 nm or more) buried-oxide layer (BOX) that is required to prevent optical leakage to the Si substrate. While Si with a thermal conductivity of 130 W/mK is one of the semiconductor materials with the best thermally conductivity, SiO_2 is 100× worse in this respect which makes it a thermal bottleneck [134, 135]. Compact device structures, e.g. heterogeneous Si microring lasers, are likely to have higher series resistance and subsequently higher thermal impedance and are more sensitive to thermal issues [150]. Figure 15.33 represents the simulated temperature rise in the heterogeneous microring laser active region at threshold and corresponding thermal impedance values as a function of ring diameter [150]. A finite element method was employed, but simulation is based on experimentally determined device series resistance and threshold current. The predicted temperature increase in the active region is 2.5 °C for $D = 50$ µm device and it grows exponentially to 63 °C for $D = 15$ µm, which prevents cw lasing for smaller ring diameters [150].

A thermal shunt approach was developed to overcome the heat blocking in the BOX layer [151–153]. The idea was to etch a number of trenches through top Si and the BOX layers within or around the III–V mesa, and then fill the trenches with highly thermal conductive materials. Figure 15.34(a) is an SEM cross-sectional image showing a heterogeneously integrated laser with two thermal shunts composed of poly-Si underneath the III–V mesa [151]. The poly-Si shunts are formed before the bonding process by first etching the trenches, and then backfilling the

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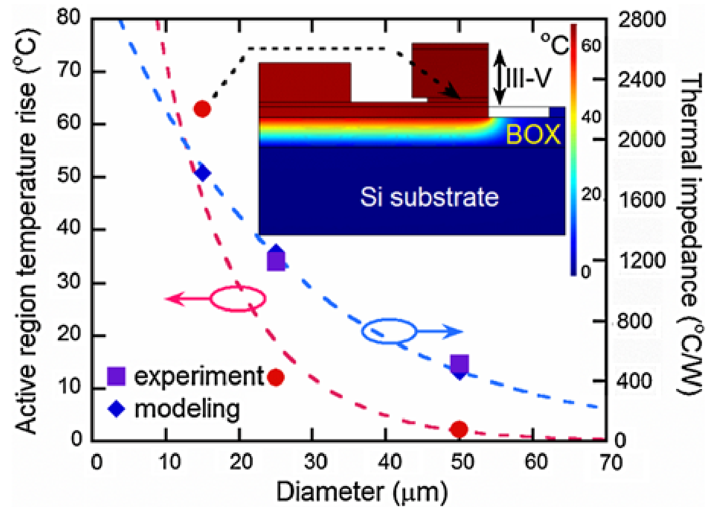

Fig. 15.33 Calculated active region temperature rise at threshold and experimental and modeling data for thermal impedance as a function of ring laser diameter. *Inset*: Temperature profile of ring laser ($D = 15$ μm) at threshold (9.4 mA) obtained by FEM modeling [150]

etched region with amorphous silicon, followed by an anneal at 900 °C for one hour. Figure 15.34(b) is the measured thermal impedance as a function of poly-Si thermal shunt width and offset from the shunt edge to the Si waveguide center. Wider shunts that are close to the silicon waveguide show the largest decrease in thermal impedance Z_t. A 7-μm-wide block of poly-Si that is 5 μm from the center of the Si waveguide reduces the average Z_t of an 800-μm-long FP laser from 41.5 to 33.5 °C/W. Narrower shunts provide less benefit, as they have a smaller cross section through which heat can flow from the upper Si epitaxial layer into the Si substrate [151].

A more effective thermal management by another thermal shunt design has been implemented in heterogeneous microring lasers [152, 153]. Figure 15.35(a) shows the 3D schematic of such a heterogeneously integrated microring laser whose p-type contact and III–V-on-Si mesa are mostly surrounded by a Au layer, and this Au layer extends to and has contact with the Si substrate after the top Si and BOX layers have been locally removed. The n-type contact inside the mesa is also connected to the Si substrate through another Au thermal shunt. This double metal shunt design enables the Joule heat from the III–V mesa to be effectively "grounded" to the Si substrate through the Au shunts [153]. Figures 15.35(b) and (c) are stage temperature-dependent LI curves for $D = 50$ μm ring lasers with and without thermal shunts. The first sudden increase in output power (just above 10 mA) corresponds to the threshold. The kinks in the curves, above threshold, correspond to switching in lasing direction. When the stage temperature was at 20 °C, both devices exhibited the same threshold current around 12.3 mA. The device without thermal shunt had earlier thermal roll-over in the output power (L–I) curves, and its maximum cw lasing temperature was about 70 °C. The device with double thermal shunts, in contrast, was able to lase cw up to 105 °C. The L–I curves show a slower thermal roll-over at the same stage temperature while the output power is 8 to 10 dB higher. With the help of this thermal shunt design, the measured thermal impedance of ring lasers with 50, 30 and 20 μm diameter is reduced from 580, 1031 and 1591 °C/W to 364, 652, and 1105 °C/W, respectively. Clearly, 30% to 40% improvement in thermal

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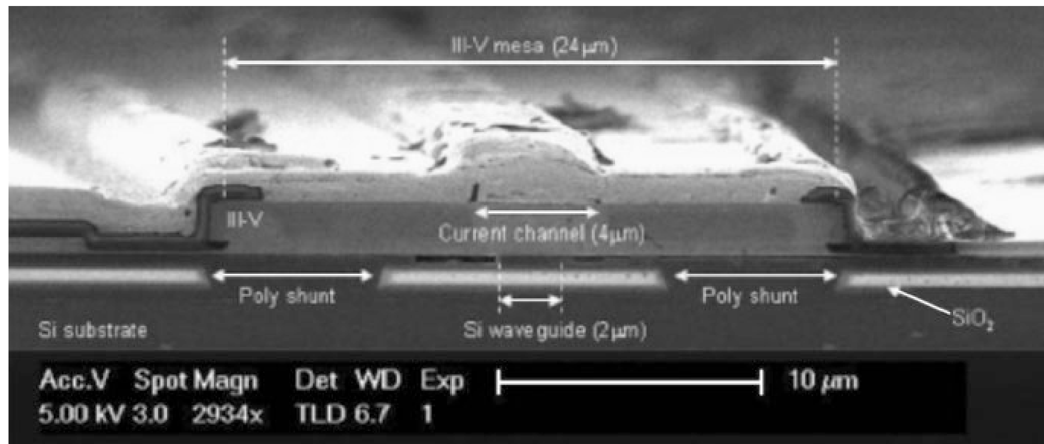
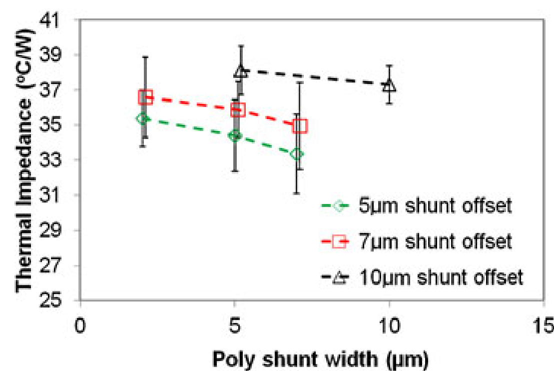


(a)



(b)

Fig. 15.34 (**a**) SEM cross section of heterogeneous silicon FP laser with 5 μm wide poly-Si thermal shunt. The shunts are used to bypass the low thermal conductivity of the SiO_2, and channel heat away from the III–V mesa into the Si substrate, (**b**) thermal impedance of heterogeneous Si lasers including poly-Si thermal shunts between 2 and 5 μm wide and that are between 5 and 10 μm away from the center of the silicon waveguide [151]

impedance was achieved for the devices with thermal shunts, and the maximum cw lasing temperatures could be raised by more than 35 °C [153]. Cu, instead of Au, can also be used and may lead to even better results due to its higher thermal conductivity compared to Au. Furthermore, Cu is preferred in CMOS processing.

In addition to integrating thermal shunts with heterogeneously integrated devices in order to minimize the BOX layer-induced thermal barrier effect, a more advanced approach is to replace the entire BOX layer by another material which can conduct heat much better and has proper optical properties (e.g., refractive index, absorption coefficient, etc.). Diamond is a good candidate because (i) it exhibits the highest bulk thermal conductivity of all materials found in nature, (ii) has excellent optical properties, and (iii) is CMOS compatible. A recent demonstration of Si-on-diamond (SOD) substrate fabrication and low-loss SOD waveguides constitutes a promising start [154]. However, open questions associated with diamond growth, wafer bonding and device fabrication require additional studies.

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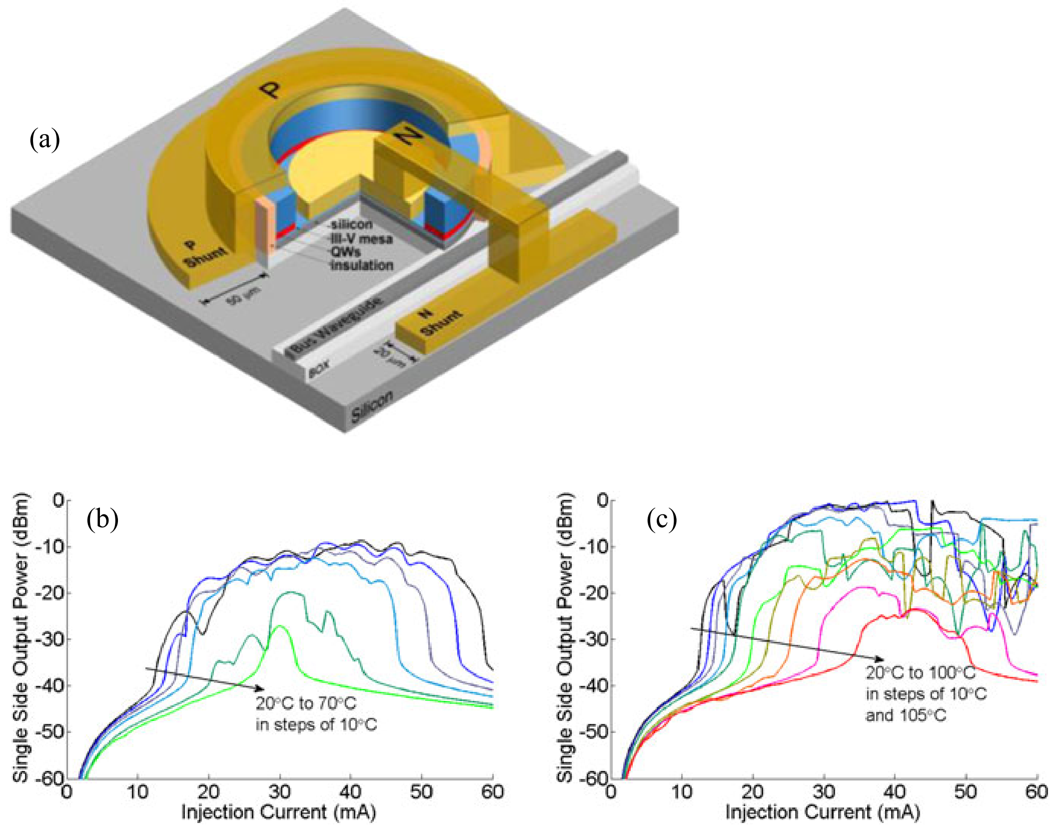

Fig. 15.35 (**a**) Illustration of heterogeneous Si microring laser with thermal shunts, and LI curve of 50 µm in diameter heterogeneous Si microring lasers (**b**) without and (**c**) thermal shunt design

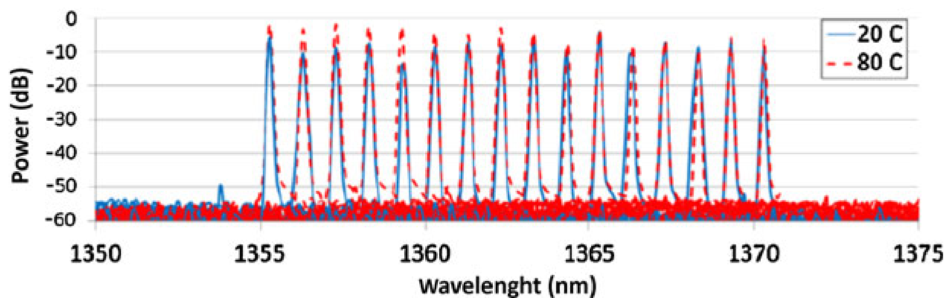

Fig. 15.36 16 wavelength array with 200 GHz spacing, wavelength stabilized at 20 °C and 80 °C [155]

In cases where emission wavelengths have to be locked to a given grid, such as in telecom applications, wavelength tuning and a feedback loop are typically required. Aurrion recently demonstrated an impressive 16-wavelength heterogeneous laser spectra from two adjacent 8-channel, 200 GHz channel spacing arrays [155]. The wavelengths are locked in a range of 20–80 °C (see Fig. 15.36). The output power exceeds 30 mW at RT and exceeds 15 mW at 80 °C, and the SMSR at all

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wavelengths of operation exceeds 40 dB. The corresponding diode efficiencies for 20 °C and 80 °C were 17% and 7%, respectively [155].

Without any doubt, the III–V-on-Si heterogeneous integration technology overcomes the fundamentally poor light emission efficiency in Si, and it offers promising CMOS compatibility and good robustness for a wide range of devices. As discussed in Sect. 15.2.4, the recent breakthrough in high-quality QD heteroepitaxy on Si substrates will make the monolithic approach significantly more competitive. As soon as the defect density can be reduced by factor of 10 the number of hours of operation can be increased to a level acceptable for commercialization, and thereafter will be an attractive long-term solution because of its scalability, lower cost and superior device performance. Regardless of which approach is adopted as the final solution for a Si-based light source, the photonic community is looking forward to the vision of photonics-microelectronics integration becoming a reality in the near future with additional market opportunities for the entire semiconductor industry.

15.3 High-Speed Signal Processing in Silicon

The progress in high-speed silicon modulators has been extraordinary in the past decade. Though conventional electro-optic effects are either unavailable (i.e. the Pockels effect [156]), or weak (i.e. the Kerr and Franz-Keldysh effects) in silicon, the free carrier plasma effect has been successfully employed to provide index changes Δn in the order of 10^{-4}–10^{-3} with reasonable applied voltages. The change of free carrier concentration not only causes the loss variation as according to (15.3), but also determines the index change as given by (15.13) [157].

$$\Delta n = \frac{-q^2\lambda_0^2}{8\pi^2 c^2 n \varepsilon_0}\left(\frac{N_e}{m_{ce}^*} + \frac{N_h}{m_{ch}^*}\right) \tag{15.13}$$

Soref et al. derived the useful empirical equations (15.14)–(15.17) to relate the free carrier plasma effect to the change of index Δn and absorption loss $\Delta\alpha$ in the telecommunication windows at 1.31 and 1.55 μm.

At $\lambda_0 = 1.31$ μm:

$$\Delta n = \Delta n_e + \Delta n_h = -6.2 \times 10^{-22}\Delta N_e - 6.0 \times 10^{-18}(\Delta N_h)^{0.8} \tag{15.14}$$

$$\Delta\alpha = \Delta\alpha_e + \Delta\alpha_h = 6.0 \times 10^{-18}\Delta N_e + 4.0 \times 10^{-18}\Delta N_h \tag{15.15}$$

At $\lambda_0 = 1.55$ μm

$$\Delta n = \Delta n_e + \Delta n_h = -8.8 \times 10^{-22}\Delta N_e - 8.5 \times 10^{-18}(\Delta N_h)^{0.8} \tag{15.16}$$

$$\Delta\alpha = \Delta\alpha_e + \Delta\alpha_h = 8.5 \times 10^{-18}\Delta N_e + 6.0 \times 10^{-18}\Delta N_h \tag{15.17}$$

where ΔN_e and ΔN_h are the respective concentration changes of electrons and holes. Please note the $(\Delta N)^{0.8}$ dependence for holes in the refractive index calculation [157]. An appreciable index change $\Delta n > 1 \times 10^{-3}$ is readily achievable by a moderate doping of about 5×10^{17} cm^{-3}, making the plasma effect the primary phase modulation mechanism in silicon. A more detailed derivation of carrier

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change-induced index and absorption variations from the Kramers-Kronig relations can be found in [158], followed by an excellent review of the history of silicon modulator development. The following sections highlight a few of the most recent innovative high-speed optical modulators on a Si substrate.

15.3.1 Silicon Optical Modulators

The first two silicon modulators passing the 10 Gb/s data transmission benchmark utilized a forward-biased MOS capacitor structure, and a ring-resonator p–i–n diode structure, respectively [159, 160]. Further improvement in bandwidth in the former case is limited by large capacitances in MOS capacitors, while the latter case suffered from slow minority carrier generation and/or recombination [161].

A p–n diode-based Mach-Zehnder interferometer (MZI) design demonstrated 50 Gb/s data transmission and more than 40 GHz bandwidth [162]. The device operates in a carrier depletion mode (i.e. reverse-biased), so the depletion region, whose width is W_D, replaces the MOS capacitor separation, resulting in a reduction of device capacitance [163]. W_D is given by

$$W_D = \sqrt{\frac{2\varepsilon_0\varepsilon_r(V_{Bi}+V)}{qN_A}} \tag{15.18}$$

where ε_r, V_{Bi}, V and N_A are the low-frequency relative permittivity of silicon, the built-in voltage, applied reverse bias voltage, and acceptor concentration respectively. The change of depletion region width leads to a change of free carrier concentration and to a related change of the refractive index as well. This subsequently results in an optical phase change $\Delta\phi$

$$\Delta\phi = \frac{2\pi\,\Delta n_{eff}L}{\lambda_0} \tag{15.19}$$

where Δn_{eff} and L are the effective modal index and the device length, respectively. The MZI geometry converts the phase modulation into an optical intensity modulation.

Figure 15.37(a) is a cross-sectional schematic view of the phase shifter, showing a 0.4 µm-wide p-doped rib waveguide. A special doping profile is designed to place the pn junction in an optimal position for good optical mode overlap and results in the highest depletion in a p-doped rib because the hole density change gives rise to a large index change as described by (15.14) and (15.16). The traveling wave electrode design based on a coplanar waveguide structure is utilized to overcome the RC limitation on modulation bandwidth. The phase modulators were incorporated into an asymmetric MZI structure with an arm length mismatch of 180 µm to convert a phase variation into an intensity modulation. A phase efficiency $V_\pi L_\pi \sim 2.8$ V-cm is obtained in a 1 mm-long phase shifter. Figure 15.37(b) shows the eye diagram of this modulator's optical output at a bit rate of 50 Gb/s. The extinction ratio is

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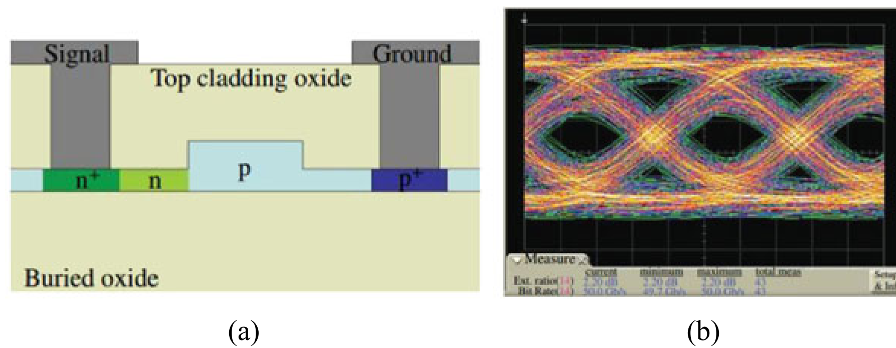

(a) (b)

Fig. 15.37 (**a**) Cross-sectional view of phase modulator (schematic). (**b**) 50 Gb/s optical eye diagram obtained at 1551.75 nm [162]

measured to be 2.2 dB and was limited by the noise from the EDFA. The eye diagram shows that the modulator is capable of transmitting data at 50 Gb/s, which is consistent with a 3 dB bandwidth >40 GHz. A polarization diversity scheme was realized by modifying the doping profile in the rib waveguide enabling modulators that can operate at 40 Gb/s for both TE and TM polarization [164].

The same research group has also demonstrated ring resonator modulators showing open eyes for data rates up to 40 Gb/s [165]. At this high bit rate the extinction ratio was 1.1 dB only, and this has been attributed to the imperfect electrical signal feeding the device which does not completely reach the 1 and 0 levels during switching. This result is particularly interesting for two reasons. First, ring resonators occupy a very small area and hence allow for dense integration, lowering cost. Second, the small size reduces the device capacitance and hence the power consumption for the modulator is <100 fJ/bit. Furthermore, the total power consumption for ring modulators including the driver can be made as low as a few pJ/bit [166].

15.3.2 Hybrid Silicon Modulators

A similar carrier depletion-mode modulator has also been implemented based on the heterogeneous integration platform discussed in Sect. 15.2.6. The III–V MQW epitaxial layer is transferred onto the SOI waveguide and the carrier density is modulated by a reverse bias. Once the MQWs are in a carrier depletion state, several physical effects, such as band-filling-, plasma-, Pockels-, and Kerr effect, all contribute to the index change. Among all of them, the Pockels effect is the only phenomenon which is sensitive to crystal orientation. In other words, this effect can be additive to the other effects if the optical signal propagates along the right direction, or it can reduce the overall index change otherwise (see also Chap. 8, Sect. 8.2.1.4). On the hybrid silicon platform, the direction of patterned silicon waveguides needs to be aligned to the [011] direction of the III–V material so that the phase shift is maximized, or under the correct angle to make it polarization independent. Figure 15.38 shows simulation results with consideration of all these effects [167]. As can be

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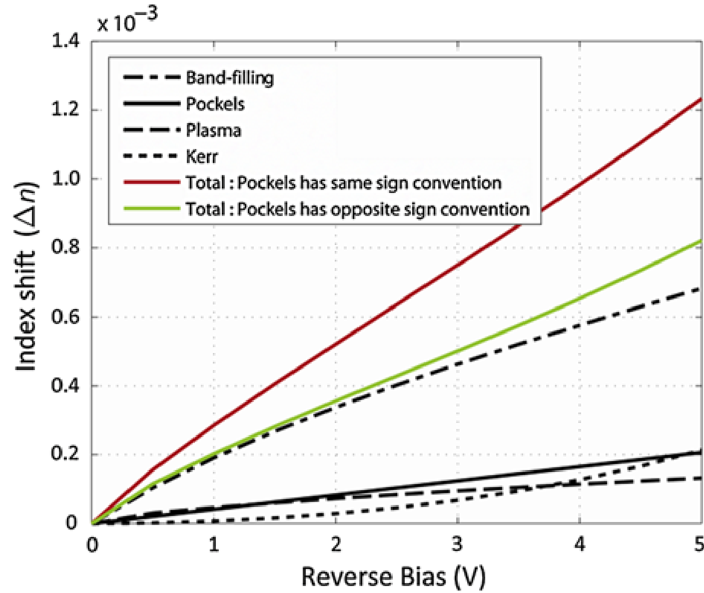

Fig. 15.38 Estimated index shift (TE polarization) of a carrier depletion InAlGaAs MQW phase modulator [167]

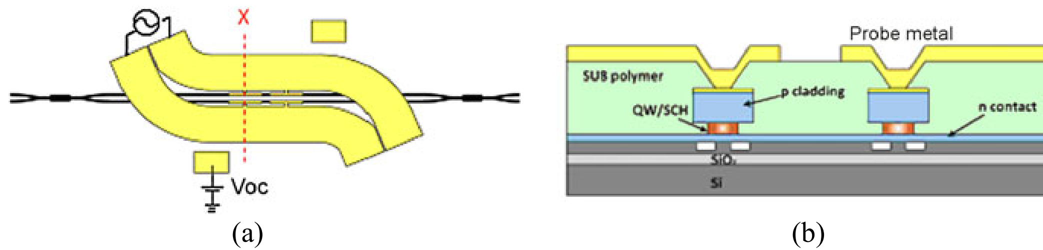

Fig. 15.39 (**a**) Top view of a device with a CL-slotline electrode. (**b**) Cross section (along x) of the hybrid waveguide [169]

seen, the index change is proportional to the magnitude of the reverse bias. Moreover, the introduced index shift in the case of orientation match is approximately 1.5 times larger than in the mismatch case.

Targeting MQWs the same reverse-bias operation, a 16-period MQW active region has been designed with a PL peak at 1.36 μm in order to achieve high optical confinement in the MQWs and low absorption at 1.55 μm [168]. Both, the top SCH layer and the MQWs, are n-type doped in order to introduce free carriers. The thickness and doping of the top SCH layer are carefully designed to result in complete depletion of this layer at zero bias. Thus, all applied bias voltage will be used to deplete the MQW region only. As shown in Fig. 15.39(a), a capacitively loaded (CL) traveling wave electrode (TWE) based on a slotline architecture is adopted to prevent the electrical field from overlapping with the doped semiconductor underneath the metal electrode. This reduces the microwave propagation losses and allows for longer modulators and higher bandwidth. The dimensions on the slotline can also be adjusted for matching the optical group velocity and the microwave phase velocity which also improves the bandwidth.

The device capacitance is reduced by half by using a push-pull scheme because the two diodes on both arms are in series [169]. The cross section of the loaded

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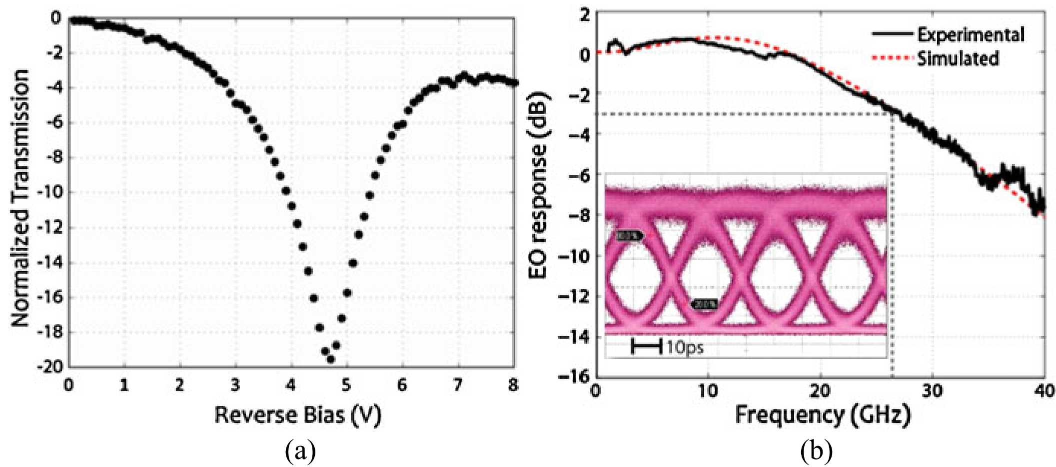

Fig. 15.40 (**a**) Normalized transmission as a function of reverse bias at 1550 nm for a 500 μm long MZM device. (**b**) Modulation bandwidth measured at −3 V with 25 Ω termination. *Inset*: Eye diagram at 40 Gb/s with 11.4 dB extinction ratio [170]

region is depicted in Fig. 15.39(b). The signal and ground of the slotline are on top of each arm, respectively. The two arms have a common ground formed by connecting the n-contact layers together. The cladding mesa is 4 μm wide, and the active region is intentionally under-cut to 2 μm to reduce the device capacitance. The silicon waveguides have a height of 0.47 μm, a slab height of 0.2 μm, and a width of 1 μm. Figure 15.40(a) shows the normalized transmission of a 500 μm long MZM device as a function of reverse bias.

As can be seen, the V_π of a 500 μm long modulator is 4.7 V. This is equivalent to a voltage length product of 2.4 V mm with a static ER of 20 dB. The frequency response of the modulator with −3 V bias across the diode and 25 Ω termination is shown in Fig. 15.40(b). The transmission curve indicates a 3 dB cutoff frequency around 27 GHz. There is good agreement between the measured and expected bandwidth. The inset of Fig. 15.40(b) shows open eyes at 40 Gb/s modulation speed with 11.4 dB extinction ratio [170].

In another approach the PL peak of an InAlGaAs-MQW based electroabsorption modulator (EAM) is shifted closer to the operation wavelength which results in a strong quantum confined Stark effect (QCSE) and consequently a high ER. The MQW section of a realized 1.3 μm EAM contained 12 wells and 13 barriers with a PL peak at 1247 nm. This design assured sufficiently low optical absorption, and making the both, the top and bottom SCH undoped, resulted in a reduced overall device capacitance.

The bias dependent optical waveguide transmission curves of the InAlGaAs-MQW EAM measured at different wavelengths are shown in Fig. 15.41. The active section, which has the same cross-sectional geometry as the MZM described earlier, has a 100 μm long effective absorber length with a three level taper design to transfer the mode into and out of the silicon waveguide with an insertion loss <0.5 dB per taper [172]. The total device insertion loss is 4.9 dB for wavelengths greater

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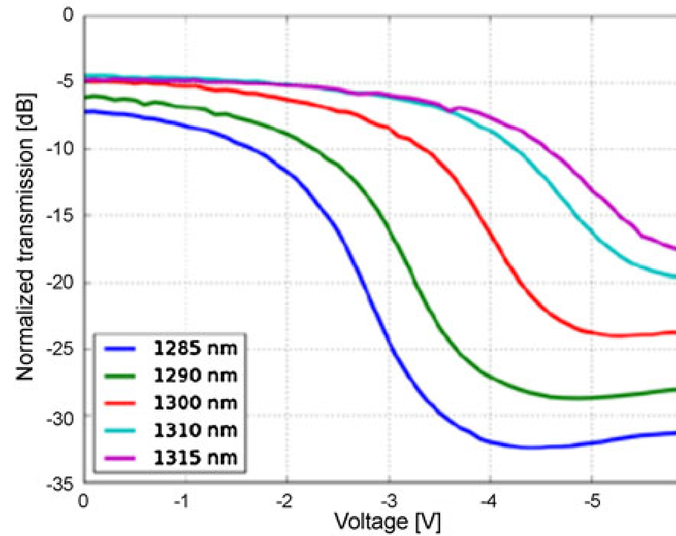

Fig. 15.41 Bias dependent transmission curves of InAlGaAs-MQW based electroabsorption modulator at different input wavelengths [171]

than 1300 nm. The static extinction ratio for a 2 V bias change is between 10 dB and 20 dB.

The electrode design is very important for an electroabsorption modulator. It affects the modulation bandwidth, the microwave reflection and the modulation efficiency. Figures 15.42(a) and (b) show the schematic structure and an SEM image of a modulator which uses a traveling wave segmented electrode design with a low impedance 100 μm active modulation segment and a high impedance 160 μm passive transmission line segment in cascade to improve the overall device modulation bandwidth. An undercut process based on selective wet etching was adopted to narrow the intrinsic layer width down to 2.35 μm while keeping the p-InP mesa width of 4 μm as defined by dry etching. A small silicon ridge width of 1 μm was chosen to keep the main part of the optical mode confined in the intrinsic region, giving a confinement factor of 24% in the MQWs. Figure 15.42(c) shows the measured and calculated electro-optical (E/O) modulation response using a 50 Ω off-chip termination at the electrical output of the device. Only a 2 dB drop was observed up to 67 GHz, which was the upper limit of the lightwave component analyzer used. The extrapolation based on simulation (assuming an intrinsic RC time constant of 1.3 ps) gives a 3 dB bandwidth of ∼74 GHz. With such a large bandwidth, this device is theoretically able to support a non-return-to zero (NRZ) transmission bit rate close to 100 Gb/s [171].

Large signal transmission experiments have been carried out at 50 Gb/s under a bias of −4 V. $2^{31} - 1$ NRZ pseudorandom bit sequence (PRBS) patterns were amplified to a level of around 2.2 V_{pp} and applied to the modulator. The input wavelength was set to 1300 nm and the optical power reaching the modulator was around 4 dBm. Figure 15.43 shows the transmission eye diagrams measured for a back-to-back (B2B) configuration and a 16 km long single mode fiber (SMF) link, respectively. All of these diagrams demonstrate widely opened eyes, and correspond to more than 9 dB dynamic extinction ratio [171].

A similar device with a lumped electrode design showed good temperature stability, with open eyes at 40 Gb/s from 20 °C to 80 °C [172]. The peak-to-peak voltage

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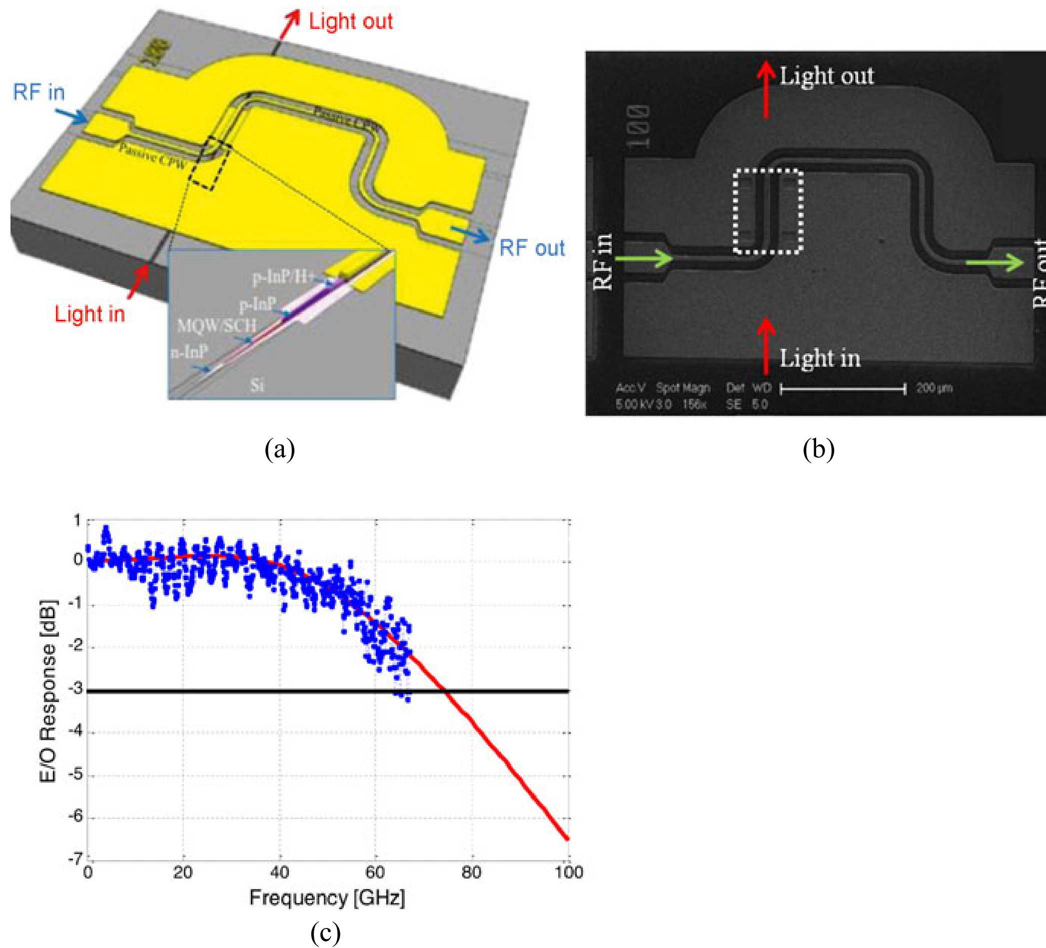

Fig. 15.42 (**a**) Schematic of heterogeneous distributed silicon modulator. *Inset*: enlarged taper part without the probe metal. (**b**) Top-view SEM image of the final device. (**c**) The measured and calculated modulation response for the modulator [171]

applied was only 1 V and the modulator consumed around 112.5 fJ/bit. There have also been recent efforts to incorporate CVD graphene on silicon to potentially fabricate a broadband temperature insensitive modulator. Reference [173] shows the demonstration of a 10 Gb/s graphene-Si electroabsorption modulator operating between 20 °C and 50 °C, in the C band.

The QCSE has also been utilized in strained Ge/SiGe MQW structures monolithically integrated on Si substrates, though the absorption coefficient in SiGe MQWs is still lower than in InP-based materials [174]. Furthermore, it has been reported that strained silicon also exhibits a linear electro-optic refractive index modulation [175]. More recently, there has been an interest in integrating $LiNbO_3$ on silicon to realize highly linear modulators for analog applications. However, the modulation bandwidth achieved needs much improvement before such devices can be incorporated into large scale systems. In summary, we believe that each of these integrated modulator solutions will soon find its appropriate role in a variety of applications.

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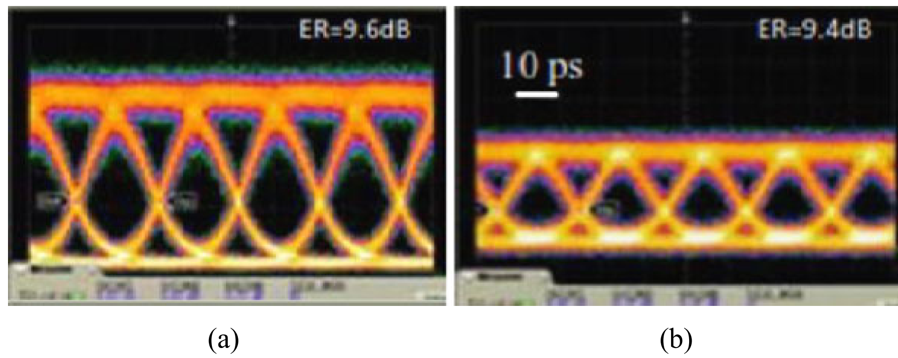

(a) (b)

Fig. 15.43 Measured $2^{31}-1$ PRBS NRZ eye diagrams at 50 Gb/s for (**a**) a back to back configuration and (**b**) after 16 km SMF transmission. The modulator under test was biased at −4 V with the input wavelength set at 1300 nm [171]

15.4 Summary

The roadmap of the microelectronics industry development indicates that Si is unlikely to be replaced by other materials. The urgent need to break the "brick wall" of interconnect bandwidth and power consumption in microprocessors plus emerging markets (e.g. fiber-to-the-home) should be a compelling force to make Si the primary host material for PICs as well. Equipped with the recently developed Si lasers, modulators and photodetectors, plus other necessary components demonstrated already or under development, sophisticated Si PICs should become widespread.

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bowers@ece.ucsb.edu

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bowers@ece.ucsb.edu

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Sudharsanan Srinivasan is a photonics system engineer at Aurrion Inc., Goleta, CA. He received his Bachelors degree with specialization in Engineering Physics from Indian Institute of Technology, Madras, India (July 2009). He received a Ph.D. on heterogeneous integration for silicon photonics at the University of California, Santa Barbara in June 2015. His research interests are in Silicon Photonics. He was President of the Santa Barbara chapter of the IEEE Photonics Society.

Alan Y. Liu received his B.S. in Physics and Mathematics with a minor in Business from Tulane University in 2011, and a Ph.D. in Electronic and Photonic Materials in 2016. He is currently a postdoctoral scholar with Prof. John Bowers' silicon photonics group at the University of California, Santa Barbara. His research interests include quantum dot optoelectronics and silicon photonics.

Di Liang is currently a research scientist at HP Labs (Palo Alto, CA). He received his B.S. degree in Optical Engineering from the Zhejiang University, Hangzhou, China in 2002, and his M.S. and Ph.D. degrees in Electrical Engineering from the University of Notre Dame, Indiana, USA in 2004 and 2006, respectively. His research interests include III–V and silicon photonics, particular in diode lasers, modulators and photodiodes, microring resonators, hybrid integration and nanofabrication technology. He has authored and coauthored over 120 journal and conference papers, three book chapters, and was granted by two US/international patents with another 27 pending. He received American Vacuum Society 35th PCSI-Young Scientist Award and Best Paper Award of The 214th Electrochemical Society Meeting both in 2008, Optical Society of America New Focus/ Bookham Student Award in 2006, and Newport/Spectra-Physics Research Excellence Award in 2005.

John E. Bowers holds the Fred Kavli Chair in Nanotechnology, and is the Director of the Institute for Energy Efficiency and a Professor in the Departments of Materials and Electrical and Computer Engineering at UCSB. He is a cofounder of Aurrion, Aerius Photonics and Calient Networks. Dr. Bowers received his M.S. and Ph.D. degrees from Stanford University and worked for AT&T Bell Laboratories and Honeywell before joining UC Santa Barbara. Dr. Bowers is a member of the National Academy of Engineering, a fellow of the IEEE, OSA and the American Physical Society, and a recipient of the OSA Tyndal Award, the OSA Holonyak Prize, the IEEE LEOS William Streifer Award and the South Coast Business and Technology Entrepreneur of the Year Award. He has published eight book chapters, 600 journal papers, 900 conference papers and has received 54 patents. He and coworkers received the EE Times Annual Creativity in Electronics (ACE) Award for Most Promising Technology for the hybrid silicon laser in 2007.

bowers@ece.ucsb.edu