Trend, Challenges and Applications of Photonic Digital Processing

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Santa Barbara February 1, 2010
Outline

- motivations
- digital signal processing evolution
- our contribution in subsystem development
- applications
- toward photonic integration
- conclusions
The Challenges of electronics

Power limitations...

...also due to the explosion of internet traffic

Internet traffic evolution

Badnwidth Issue at I/O for Tera-scale Servers

Google’s new data centers

Power consumption > 100 MegaW
Advantages

- High bandwidth
- High spectral and spatial coherence
- RF interference free
- Robustness to the cosmic radiations
- Low distortions in signal distribution

Using opportune integration solutions:

- Low power consumption
- Photonic processing cheaper than electro-optical-electro conversion

Applications and related projects

- Ultra-fast interconnection optical networks (MUFINS, LASAGNE, EUROFOS in Europe, NEDO in Japan)
- Network security (Optical firewall – WISDOM in Europe)
- Optical Computing (Lincoln Laboratory-MIT)
- Applications in space capsule (NASA)
- Low phase noise radar transmissions (PHODIR)
- Microwave optics
- Sensors in hostile surroundings
- Grid Computing
- Medical applications
- Biophotonics
- Spectroscopy
- Material characterization
Towards photonic digital processing


1. 2400 BC
2. 1941
3. 1822
4. 1939
5. 1950
6. 1963-67
7. 1969
8. 1971
9. 1978
10. 1992
11. 1995
12. 1996
13. 1998
14. 2000
15. 2003
16. 2008
17. 2010

“AN ULTRAFAST LIGHT GATE, M. A. Duguay and J. W. Hansen, Bell Telephone Laboratories, Murray Hill, N. J.
A device has been built which is capable of gating light on and off on the picosecond time scale. The gate is built in much the same fashion as the optical Kerr cell, the difference being the use of powerful optical pulses rather than electrical pulses to induce a birefringence in various liquids. In the experiment, powerful light pulses from a mode-locked Nd:glass laser, ~5 psec in duration (wavelength 1.06 μm), are used to induce a birefringence in a number of liquids including Cs2, nitrobenzene, chlorobenzene, dichloroetane and others. The transmission of the gate as a function of time is studied by means of a 1033 nsec flashlamp photocell. From the 1.06 μm u.e., the second harmonic generation. With Cs2, the transmission curve has a width of ~8 psec, the peak transmission is 10% and the extinction ratio is 200. With nitrobenzene the curve has an exponentially falling tail on one side. The associated decay time is ~22 μsec. Since 22 μsec is a time characteristic of molecular reorientation times, this observation provides direct support for the long held belief that orientational effects dominate light induced refractive index changes in nitrobenzene.”


Towards photonic digital processing

“All-optical 160Gb/s half-addition half-subtraction and AND/OR function exploiting pump depletion and nonlinearities in a PPLN waveguide” , Bogoni et al. Postdeadline paper ECOC 2008


All-optical logic gate implementations
### Some possible technologies - 1

**Periodically Poled Lithium Niobate (PPLN) waveguide**¹,²

<table>
<thead>
<tr>
<th>Feature</th>
<th>Properties</th>
</tr>
</thead>
<tbody>
<tr>
<td>Complete transparency</td>
<td>Passive (no excess noise)</td>
</tr>
<tr>
<td>Dimensions</td>
<td>Ultrafast response</td>
</tr>
</tbody>
</table>

**Symmetric Self-Electrooptic Device (S-SEED)**³,⁴

<table>
<thead>
<tr>
<th>Feature</th>
<th>Properties</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low switching energy</td>
<td>Speed (?)</td>
</tr>
<tr>
<td>Cascadability</td>
<td>Dimensions</td>
</tr>
</tbody>
</table>

**Ionically Self-Assembled Monolayer (ISAM) films**⁵

<table>
<thead>
<tr>
<th>Feature</th>
<th>Properties</th>
</tr>
</thead>
<tbody>
<tr>
<td>Robustness</td>
<td>Low cost</td>
</tr>
<tr>
<td>Dimensions</td>
<td>Speed (?)</td>
</tr>
<tr>
<td>Efficiency (?)</td>
<td>Early stage</td>
</tr>
</tbody>
</table>

**Vertical Cavity Semiconductor Gates (VCSGs)**⁶

<table>
<thead>
<tr>
<th>Feature</th>
<th>Properties</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low cost</td>
<td>Passive (no excess noise)</td>
</tr>
<tr>
<td>High contrast ratio</td>
<td>Efficiency</td>
</tr>
<tr>
<td>Pol. independent</td>
<td>Temperature dep.</td>
</tr>
</tbody>
</table>

---


⁵ V. Kochergin et al., “Programmable Logic Gates for Optical Processing,” in Proc. ITNG 2008. (Luna, Univ. Alberta)

### Some possible technologies - 2

#### Semiconductor Optical Amplifier (SOA) and Reflective-SOA\(^7,8\)

<table>
<thead>
<tr>
<th>mature technology</th>
<th>hybrid integration</th>
<th>regenerative</th>
<th>dimensions</th>
<th>monolithic integration</th>
<th>speed</th>
<th>power (temperature)</th>
</tr>
</thead>
</table>

#### Quantum Dot Semiconductor Optical Amplifier and Laser (QD-SOA)\(^9\)

<table>
<thead>
<tr>
<th>low power consumption</th>
<th>high speed</th>
<th>selective wavelength</th>
<th>high gain</th>
<th>early stage</th>
<th>cost (process)</th>
<th>dimensions</th>
</tr>
</thead>
</table>

#### Symmetric-Mach-Zehnder (SMZ) in 2-dimensional photonic crystal (2DPC) and QD\(^10\)

<table>
<thead>
<tr>
<th>high speed</th>
<th>hybrid integration</th>
<th>dimensions</th>
<th>monolithic integration</th>
<th>power (temperature)</th>
</tr>
</thead>
</table>

#### Active plasmonics, ultra-fast switch\(^11\)

<table>
<thead>
<tr>
<th>high speed</th>
<th>dimensions</th>
<th>Power consumption efficiency</th>
<th>integration</th>
</tr>
</thead>
</table>

---


Silicon microphotonics\textsuperscript{12,13,14}

<table>
<thead>
<tr>
<th>low power consumption</th>
<th>loss</th>
</tr>
</thead>
<tbody>
<tr>
<td>dimensions</td>
<td>Lacks efficient light emission</td>
</tr>
<tr>
<td>cost</td>
<td></td>
</tr>
<tr>
<td>monolithic integration</td>
<td></td>
</tr>
<tr>
<td>CMOS compatibility</td>
<td></td>
</tr>
</tbody>
</table>


Our approach for photonic digital processing

Step 1: Analysis realization and comparison of all-optical subsystems based on discrete devices,

Step 2: Design of integrated optical circuits

Step 3: Interaction with promising optical technologies for implementing power efficient integrated prototypes

Step 4: Testing of the integrated devices in our sub-systems

Step 5: Investigation of possible applications for photonic digital processing
  ✔ High capacity optical networks
  ✔ Network security
  ✔ Digital radar systems
  ✔ Optical instrumentation
  ✔ Biophotonic

First custom prototype
Developed for CNIT

~7 x 2 cm
## Nonlinear effects in commercially available optical devices

<table>
<thead>
<tr>
<th></th>
<th>Fiber</th>
<th>Waveguide</th>
<th>SOA/EAM</th>
<th>SESAM</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Speed</strong></td>
<td>≈ fs</td>
<td>≈ fs pump depletion ≈ ps SFG &amp; DFG</td>
<td>intraband phenomena ≈10 fs interband phenomena ≈100 ps</td>
<td>few ps</td>
</tr>
<tr>
<td><strong>Stability</strong></td>
<td>low</td>
<td>high</td>
<td>high</td>
<td>high</td>
</tr>
<tr>
<td><strong>Polarization Dependence</strong></td>
<td>yes</td>
<td>yes</td>
<td>no</td>
<td>no</td>
</tr>
<tr>
<td><strong>Cost</strong></td>
<td>Low ≈ 100 €/km</td>
<td>high ≈ 7000€</td>
<td>high ≈ 1000€</td>
<td>Low ≈ hundreds €</td>
</tr>
<tr>
<td><strong>Integrability</strong></td>
<td>no</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td><strong>Walk-off</strong></td>
<td>present</td>
<td></td>
<td></td>
<td>yes</td>
</tr>
<tr>
<td><strong>Pattern Dependence</strong></td>
<td>no</td>
<td>Yes (SFG &amp; DFG)</td>
<td>Yes (SFG &amp; DFG)</td>
<td>yes</td>
</tr>
</tbody>
</table>
Basic functions

- Optical logic gates
- Combinatorial networks
- Optical flip-flop

Highly nonlinear fiber
- Fast dynamics
- High efficiency
- Not integrable
- Polarization dependent

SOA
- Integrable
- High efficiency
- Polarization independent
- Not very fast dynamics

SESAM
- Integrable
- Passive devices
- High efficiency
- Polarization independent
- Slow dynamics

PPLN waveguide
- Integrable
- High efficiency
- Polarization independent
- Not very fast dynamics
Using Semiconductor Optical Amplifier (SOA)

Advantages
- Integrability
- Polarization independence
- Cost
- Stability

Problems
- Speed
- Pattern dependence
Using Periodically Poled Lithium Niobate (PPLN) waveguide

Advantages
- Ultra-fast dynamics
- Integrability
- Passive device
- Stability

Problems
- Polarization dependence
- Temperature control
- Cost
Our digital processors based on SOA

Berrettini et al. "Ultrafast Integrable and Reconfigurable and NOT Photonic Logic Gate", Photonics Technology Letters, 18, 8, 917-919, April, 2006


J. Wang et al., "All-Optical Counter Based on Optical Flip-Flop and Optical AND Gate ", ECOC 2009, P3.21.


J. Wang et al., "All-Optical Clocked D-Type Flip-Flop Exploiting SOA-Based Optical SR Latch and Logic Gates", Photonics is Switching 2009, 10:15 – Th1 1-6.


Our contribution:
Better performance implementations
First implementations

Counter

WC

Demux

ADD/DROP

Counter

λ - converter

SR, D, T, J-K

Flip-Flop

FF
Our digital processors based on PPLN waveguide

Our contribution:
All first implementations

A. Bogoni, et al., "All-op


Using Semiconductor Optical Amplifier (SOA)
Reconfigurable logic gates

10 Gb/s implementation

**Reconfigurable logic gates**

Counter-propagating configuration

10 Gb/s implementation

```
-Log(BER)

Received Mean Power [dBm]
```

- Log(BER) vs. Received Mean Power [dBm]

- B2B
- AND

**Received Mean Power [dBm]**

<table>
<thead>
<tr>
<th>IN</th>
<th>OUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 Gb/s implementation</td>
<td>XGM</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

**IN**

**OUT**
Combinatorial network for OPS networks

- High priority Input: $P_{IH}$
- High priority address: $A_H$
- Low priority address: $A_L$
- Switching Control Generation: SCG
- Contention Resolution Control: CRC

![Diagram]

First combinatorial network for OPS networks

SCG power penalty < 0.2 dB
CRC power penalty < 5 dB

First demonstration in a real 160 Gb/s OPS net testbed

More complex functions

N bit digital comparator

- Higher efficiency packet priority management in OPS net
- All-optical performance monitoring
- Network security

N. Andriolli, et al., "Multistage interconnection network photonic controller exploiting a cascaded SOA-based ultrafast module", in Proc. ECOC'07, P117, 2007
- Full adder

- Optical packet processing
  - Congestion prevention (method of complements)
- Viterbi algorithm in the MLSE
- Optical computing

A/D converter

- High bandwidth optical sampling oscilloscope
- Photonic front-end in fully digital radar systems
- High-definition video,
- Real-time signal monitoring,
- Ultra-fast dispersion compensation

D/A converter

- 2 gates for 2-bit operation (state of the art: 3 gates)
- no assist pulse train required
- wavelength preserving
- low power operation and integrable

D/A converter

- Optical multilevel signals generation for increasing spectral efficiency
- Label/payload encoding
- Pattern recognition
- Arbitrary waveform generation for radar and display applications

Using Periodically Poled Lithium Niobate (PPLN) waveguide
Combining pump depletion and SFG+DFG


Input signals

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>B</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Output signals

<table>
<thead>
<tr>
<th></th>
<th></th>
<th>idle</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>B</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

PPLN waveguide

C-band

SFG

DFG

QPM

CW

Pump depletion
Combining pump depletion and SFG+DFG


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Output signals

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<td>0</td>
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</tr>
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<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

PPLN waveguide
Combining pump depletion and SFG+DFG

160 Gb/s implementation

- BtoB ch A
- BtoB ch B
- demux ch A
- demux ch B
- A AND B
- A AND B
- A XOR B
- A OR B

Received peak power [dBm]

### Flip-flop: SR latch

**Diagram:**

- **Reset**
  - Flip-flop 1
  - NOT logic gate 1
  - Assistant
  - Flip-flop 2

- **Set**
  - Flip-flop 2
  - NOT logic gate 2

**Parameters:**

- **Electronic LSI circuit**
  - Switching time: <10 ns
  - Switching energy: 10 fJ
  - Contrast ratio: <5000

- **Electronic ULSI**
  - Switching time: <100 ps
  - Switching energy: 2-5 fJ
  - Contrast ratio: <0.5

- **Coupled micro-ring lasers (InP/InGaAsP integrated circuit)**
  - Switching time: 20 ps
  - Switching energy: 5.5 fJ

- **Bistable Laser Diodes**
  - Transition time: T_{rel}
  - Switching energy: Few fJ
  - Contrast ratio: 20 dB

- **Semiconductor passive planar micro-resonators (simulated)**
  - Rise time: 10 ps
  - Switching energy: 100-200 fJ
  - Contrast ratio: Few m

- **Er/Yb Doped Fiber (SOA, discrete devices)**
  - Switching time: 10 ns
  - Switching energy: 20 nJ

- **SOA (integrated numerical)**
  - Switching time: 2 ps
  - Switching energy: 120 fJ

- **Nano-photonics**
  - Rise time: 10 ps
  - Switching energy: 100 fJ

**Graphs:**

- **Wavelength (nm):**
  - Laser 1
  - Laser 2

- **OSA traces:**
  - CR > 40 dB
  - CR = 50 dB

- **Power (dBm):**
  - -65
  - -55
  - -45
  - -35
  - -25
  - -15
  - 5

**References:**

Flip-flop: SR latch

Application in 10 Gb/s packet switching

SR latch application in triggered optical flip-flops & counter

Combining one or more SR latch basic blocks and AND logic gates it is possible to realize optical flip-flops & counter with set/reset signals triggered by a reference clock.

- finite state machine in optical computing
- header recognizing, payload processing, buffering and forwarding of optical packets in OPS nets

Applications

High capacity optical networks

Ultra-fast optical instrumentation

Network security

Optical computing

Sensors

Space capsule

Digital radar systems

Microwave optics

biophotonics

spettroscopy

cniiit
Ultra-fast optical systems

- Transmitter (pulsed source, multiwavelength sources, multilevel transmitters)
- Multiplexing (time, wavelength, polarization techniques)
- Inline regeneration (clock recovery, reshaping, reamplifying, and retiming)
- Transmission (CD & PMD dispersion compensation, nonlinear distortion, crosstalk, ...)
- Demultiplexing (time, wavelength, polarization, phase/amplitude modulation format conversion)
- Wavelength conversion

Ultra high capacity transmission systems:

- 640 Gb/s Optical Time Division Multiplexing (OTDM) systems
- Hybrid OTDM/WDM system
- 100 Gbit/s Coherent system
Photonics for WDM-PON: CW multi-l source

Pulse Source e.g., 50GHz
Supercontinuum generation
Channel spacing e.g., 50GHz
Mode-locked laser

Proposed scheme

Electrical eye-diagram
20nm @ -10dB

Commercial instrument

Back-to-Back BER @10Gbps at the APD

Optical equipments: optical pulse sources

WWW.photrix.it

Banchtops

modules

mainframes with interchangeable module
Study, design and realization of a fully digital radar transceiver demonstrator, using photonic technologies for both radar signal generation and received RF signal processing.

**ARCHITECTURE**

**ADVANTAGES**

- Fully digital radar transceiver exploiting photonic technologies based on electro-optic integration
- Transmitter with high phase coherence, and ultra high microwave frequency
- Fully digital receiver based on ultra-fast optical signal processing
- Less requirements in terms of phase coherence
- Flexible solution

### Results of technical tests

<table>
<thead>
<tr>
<th>Item</th>
<th>Parameter Description</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Pulse Rep Rate (PRR)</td>
<td>( f_0 )</td>
<td>500.035 MHz</td>
</tr>
<tr>
<td>2</td>
<td>Pulse source wavelength</td>
<td>( \lambda_0 )</td>
<td>1549.24 nm</td>
</tr>
<tr>
<td>3</td>
<td>Optical Spectrum 10dB BW</td>
<td>( \Delta\lambda )</td>
<td>&gt; 22 nm</td>
</tr>
<tr>
<td>4</td>
<td>Ripple in 10dB BW</td>
<td>( R )</td>
<td>&lt; 2 dB</td>
</tr>
<tr>
<td>5</td>
<td>Autocorrelation pulsewidth (after optical filter with 3 dB BW of 1.9 nm) in the 10 dB BW</td>
<td>( \tau )</td>
<td>&lt; 15 ps</td>
</tr>
<tr>
<td>6</td>
<td>Crosstalk between adjacent pulses (after optical filter with 3 dB BW of 1.9 nm) in the 10 dB BW</td>
<td>( C_t )</td>
<td>&lt; -29</td>
</tr>
<tr>
<td>7</td>
<td>Phase noise (after optical filter with 3 dB BW of 1.9 nm) in the 10 dB BW</td>
<td>( \Phi N )</td>
<td>&lt; 30 fs</td>
</tr>
<tr>
<td>8</td>
<td>Pulse amplitude noise (after optical filter with 3 dB BW of 1.9 nm) in the 10 dB BW</td>
<td>( A N )</td>
<td>&lt; 0.18 %</td>
</tr>
<tr>
<td>9</td>
<td>Side Band Suppression (after optical filter with 3 dB BW of 1.9 nm) in the 10 dB BW</td>
<td>SBS</td>
<td>60 dB</td>
</tr>
<tr>
<td>10</td>
<td>Pulse source average power</td>
<td>( P_H/P_L )</td>
<td>&gt; -2 dBm at high power port; &gt; -12 dBm at low power port</td>
</tr>
</tbody>
</table>
Photonics for biophotonic applications:

- **Optical Topography**
- **Optical Tomography**
- **Diffuse Time-resolved Spectroscopy of cardiac tissue**

**source**

- PicoSource
- ODL
- EDFA
- BPF
- SHG
- PPLN
- BPF

**measures and data processing**

- Variable mechanics
- Tomographic chamber

**design**

- Routing Network
- Detection
- Reconstruction Algorithms

**protocol**

- Earliest light
- Most scattered light

Graphs and charts showing data on wavelengths and optical properties.
Testing of integrated devices in our subsystems and cooperation with technology people to define the potentials of the photonic digital processing.
Toward technological development
1908: 8x2 switch @ 64 kBit/s

≈1000 W
≈ 2 mW/bit
electro-mechanical

2008: 2x2 switch @ 40 GBit/s

≈5 W
≈10 pW/bit
all-optical
From the system to the chip

Photonic processing for the future

Electronic evolution

From the system to the chip

Photonic evolution

The Atanasoff–Berry Computer (ABC) solves systems of linear equations. The arithmetic logic functions were implemented with vacuum tubes. The control logic functions were electromechanical, implemented with relays.
Why photonic integration

- Exploit the economics of wafer scale integration
- Implement complex functions (systems-on-a-chip) in a compact and cost-effective way
- Obtain higher creativity in design with many more functional elements per chip
- Permit interferometric structures
- Improve performance
  - Better power efficiency
  - Minimize optical power loss at interfaces between device elements
  - High reliability
  - Less interfaces
  - Robust
- Align photonic components automatically by lithography
- Obtain simpler packaging and assembly, with standard processes
- Single chip designs with minimal optical interfaces are ideal for demanding environments
Trends in photonic integration

- Towards higher levels of integration
- Towards “nanophotonic” approaches
- Silicon is rapidly gaining importance, next to established PIC-technologies (InP, glass)
- Integration of photonics with electronics
- Apart from many SME-actors, a few larger companies focus on PICs
Approaches to photonic integration

- Cost of entry is very high:
  - photonic integration is available only to a very few companies today
- An alternative approach:
  - “Generic” foundry approach for arbitrary applications on a common qualified process base
  - Design systems that allow user-specified designs to be right first time
  - Very like ASICs in silicon microelectronics

In Europe
System people must contribute to photonic integration

Separate design from process technology
design for the technology
(not design the technology)

- systems
- circuit
- waveguide
- materials

Design rules,
Technology description
Design library
Standard cells
Conclusions

- Photonics can guarantee the evolution of digital processing

- Digital photonic processing based on basic building gates seems to be one of the most practical approach

- Technologies issues are at the moment the main limitation to the photonic digital processing development

- It is mandatory to merge technological development and system design in order to obtain ultra-fast digital processing guaranteeing
  - Low power consumption
  - Monolithic integration
  - High performance
thank you!
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