Simple Epitaxial Lateral Overgrowth Process as a Strategy for Photonic Integration on Silicon

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***Abstract*—In this paper we propose a strategy to achieve monolithic integration of III–Vs on Si for photonic integration through a simple process. By mimicking the SiO_2/Si/SiO_2 waveguide necessary to couple light from the gain medium on its top, we adopt a $\sim$2 μm thick silicon dioxide mask for epitaxial lateral overgrowth (ELOG) of InP on Si. The ELOG InP layer as wells as the subsequently grown quantum wells ($\sim$1. 55 μm) have been analyzed by photoluminescence and transmission electron microscopy and found to have high optical quality and very good interface. The studies are strategically important for a monolithic platform that holds great potential in addressing the future need to have an integrated platform consisting of both III–Vs and Si on same chip.**

***Index Terms*—Monolithic integration of III–Vs on Si, integrated photonics, III–V lasers on Si, ELOG.**

I. Introduction

MONOLITHIC integration of III–Vs on Si is the logical extension of the present day electronic and photonic components. The requirement is to deliver a platform that not only integrates the advantages of both technologies but also reduces the cost and results in smaller footprint than current conventional components. The idea has driven the electronics and photonics researchers around the globe for a couple of decades now and numerous efforts have been made to achieve this integrated platform. InP based alloys that offer favourable wavelengths have attracted interest for integration of InP based compounds on Si, particularly due to their use in long haul communication and also for short-reach high-data rate communications as e.g. relevant for data centers or high-performance computing. To realise this, attempts started with direct growth of thick layers of InP on Si using metal organic chemical vapour deposition [1] and later light sources were demonstrated using direct growth of InGaAsP/InP heterostructures on Si [2]. So far these have not been adopted by the industry due to several issues related to material degradation and early device aging caused by high lattice mismatch. This high lattice mismatch of around 8% and large difference ($\sim$50%) in thermal expansion coefficient of InP and Si motivated researchers to investigate other approaches for integration like hybrid integration using direct bonding [3], [4] and adhesive bonding [5] of InP on Si. This technique has been the most successful method of integration and resulted in demonstration of light sources, amplifiers, modulators and photodetectors on Si [6], [7] with their performance comparable to those realised on planar InP substrates. Even though exemplary results have been reported as this technique integrates the photonic functionality to the CMOS circuitry, truly monolithic approaches are desirable in the long run to reduce the footprint size and manufacturing costs together with enhanced yield.

Recently few successful attempts to monolithically integrate III–Vs on Si have also been reported. Laser operation using III-dilute nitrides based compounds like Ga(NAsP) lattice matched to Si substrates has shown encouraging results at 120 K, although room temperature operation remains to be performed [8]. Room temperature operation of InAs/GaAs quantum dot lasers on Si emitting at 1.3 μm has been realized [9] but so far emission at 1.55 μm has not been realized. Another exciting approach to achieve heterogeneous integration of III-Vs on Si called epitaxial lateral overgrowth (ELOG) has shown promising results [10]–[13] and has the potential to monolithically integrate sources, detectors and modulators for 1.55 μm although to date no such results have been demonstrated. InGaN based light sources on GaN grown using ELOG have been demonstrated a long time ago [14], but to date no InGaAsP/InGaAs based light sources on InP grown on silicon using ELOG have been reported. In this technique a thin film of the desired material is laterally overgrown on a dielectric mask selectively through defined openings from a predeposited seed layer on the host substrate. This dielectric mask hinders the infiltration of defects generated in InP seed layer due to its lattice mismatch with Si. In earlier studies [10]–[13] on ELOG of InP on Si, even though the defects are stopped by the overlying dielectric mask they are still observed above the openings. A hypothesis by Langdo *et al.* [15] emanating from ELOG of Ge conducted on Si suggests the feasibility of defect filtering even above the openings, so called the necking effect when high ratio of mask thickness to opening width (=aspect ratio) is employed. In that work an aspect ratio of greater than 1 is proposed to

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potentially stop all the threading dislocations arising from the seed layer even above the openings. This is also confirmed by our current study, although a recent study by Wang *et al.* [16] has proposed that during selective area growth a mask to opening aspect ratio of greater than 2 is required for extended defect filtering in the openings.

As a strategy for monolithic integration, work done in our laboratory led to the proposal of a monolithic evanescently coupled silicon laser (MECSL) [17] by making use of ELOG InP on Si. In this structure, silicon waveguide is buried in SiO_2, which together with Si act as the mask during ELOG. Thus the gain from InGaAsP based multi-quantum well grown on ELOG InP can be coupled into the Si waveguide beneath, which also acts as the cavity in this design. An alternative design for monolithic integration also uses such a stack for evanescent coupling of light from the adjacent QD lasers on GaAs/Si [18]. Both of these designs demand the "SiO_2/Si/SiO_2 cladding/waveguide/cladding stack" to be on the order of 2 μm. In our MECSEL design, using such a stack as the mask of similar thickness also allows for the opening width of ~1 μm for ELOG for effective defect filtering and is large enough to be able to be processed by optical lithography. An added advantage is that such a relatively large width compared to the nano-sized openings produced by e-beam lithography allows for very low thermal resistivity as these large openings act as effective vias for thermal dissipation in a MECSEL structure [17].

In this study, we demonstrate the feasibility of using such a large mask thickness of 2 μm in ELOG InP on Si by making use of optical lithography with an opening width of 1 μm. By making use of high enough aspect ratio, we demonstrate from transmission electron microscopy (TEM) studies that defect filtering indeed happens even within these wide openings. Besides, a high quality multi quantum well (MQW) with a photoluminescence emission of ~1.5 μm is also demonstrated. The quality of ELOG InP grown by this method is compared with that of the ELOG layers created by unconventional techniques such as e-beam lithography. From a comparative study, we demonstrate the following: (i) low aspect ratio results in defect penetration from the seed layer into the ELOG layer above the opening, (ii) coalescence of adjacent layers also create defects, which however is true only for ELOG InP conducted on the InP seed layer on silicon but not on pure InP substrate suggesting coalescence defects are not inherent to ELOG and (iii) uncoalesced ELOG InP from the patterns generated from optical lithography is of high quality suitable for monolithic integration in a MCSEL design. TEM and μ-PL are used whenever necessary to assess the structural and optical quality of the studied layers.

II. Experiment

In this paper Si (001) wafer 4° off orientated toward $\langle 111 \rangle$ precoated with InP seed layer with an approximate thickness of around 2 μm supplied by SPIRE® corporation USA are used. Defect density in the InP seed layer is as high as 4×10^9 cm^{-2}. The substrate patterning for ELOG consists of crucial steps like polishing of seed layer [19] and etching of high aspect ratio dielectric mask with smooth sidewalls, optimised in this study.

TABLE I
Sample Description

Sample ID	Nominal Opening Size (nm)	Nominal SiO_2 mask thickness (nm)	Aspect ratio	Lithography type
A	1000	40	0.04	E-beam
B	300	700	2.3	E-beam
C	1000	2000	2	Optical

Three samples *A, B, C* are prepared, with varying SiO_2 mask thickness, opening and separation size. E-beam or optical lithography is used for pattern fabrication. Detailed sample description is given in Fig. 1 and Table I. Sample A with aspect ratio $\ll 1$ is used to confirm the ineffective defect filtering. Sample B is considered for demonstrating the potential coalescence defects despite high enough aspect ratio; to study this effect single, double and multiple openings are defined on sample B. Sample C is considered to demonstrate the strategy for monolithic integration by considering a high enough mask thickness as mentioned above which is facilitated by optical lithography. ELOG on sample C is not allowed to coalesce to avoid coalescence defects.

After polishing the InP seed layer on silicon, SiO_2 mask of varying thickness as mentioned in Table I is deposited using plasma enhanced chemical vapour deposition at 300 °C. Deposition time is varied from 100 s to 30 min to achieve specific SiO_2 thickness. Afterwards relevant photoresist is spun to perform e-beam or conventional optical lithography to define the pattern on these InP on Si template coated with SiO_2. Line openings are defined at 30° off [110] to facilitate higher lateral growth rates [20]. Conventional CHF_3 based reactive ion etching is used to etch smooth and vertical sidewalls in SiO_2 using photoresist as an etch mask. These templates are then used in sequential growth runs for ELOG of InP on Si using LP-HVPE. Sulphur doped InP is grown on all the samples with a nominal doping of 2×10^{18} cm^{-3}, which could be used as *n*-type contact layer in the case of device fabrication. We also include a planar reference InP sample in all the runs. Sample A is grown with V/III ratio of 10 for a growth time of 2 minutes and 20 seconds at a growth temperature of 615 °C to achieve a coalesced ELOG layer. Sample B is grown with a V/III ratio of 10 for a growth time of 2 min at growth temperature of 610 °C to achieve a coalesced layer. Sample C is grown with a V/III ratio of 10 for a growth time of 17 min at growth temperature of 605 °C. In the case of sample C these growth parameters are optimized in order not to allow for coalescence of the adjacent growth fronts. After stripping off the SiO_2 mask using 7% buffered HF, MQW designed to emit at 1.55 μm are grown by MOVPE. A reference planar InP substrate is also included in this run. SiO_2 mask is stripped off to avoid loading effect that can change the composition of the MQWs drastically [21]. The MQW layer structure is given in Table II. Optical properties of all the samples are studied using μ-PL at room temperature. TEM analysis is done on the cross-section of the ELOG layers and MQW layers.

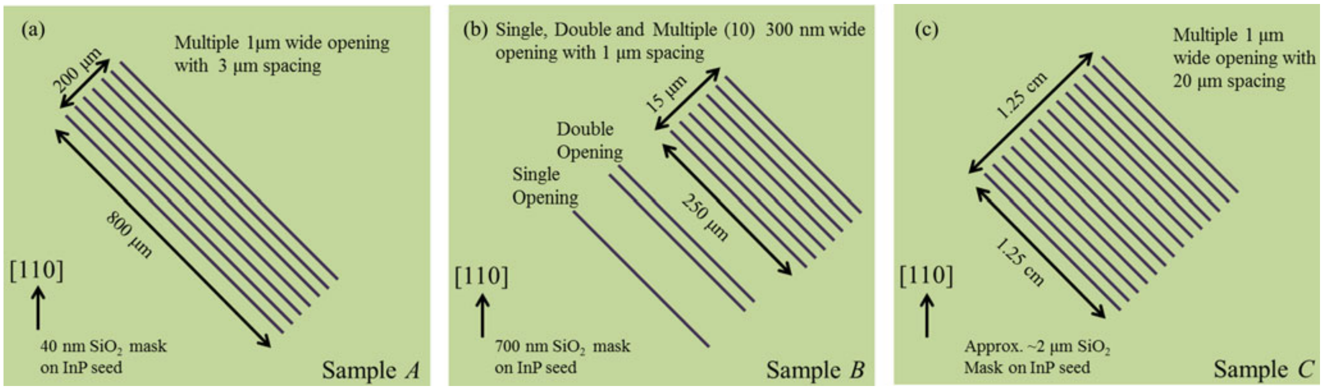

Fig. 1. (a), (b), and (c) show detailed description of mask design and field size for sample A, B, and C respectively.

TABLE II
EPITAXIAL LAYER STRUCTURE OF THE MQWS GROWN ON ELOG INP ON SI USING MOVPE; UID: UNINTENTIONALLY DOPED

Layer Number	Material	Thickness	Doping (cm^{-3})	Details
ELOG InP on Si	n-InP	9 μm	$1x10^{18}$	
1	InP	1.8 μm	UID	Cladding
2, 18	$In_{0.71}GaAs_{0.61}P$	105 nm	UID	SCH
3,5,7, 9,11,13,15,17	$In_{0.73}GaAs_{0.51}P$	8.26 nm	UID	Barrier
4,6,8,10,12,14,16	$In_{0.73}GaAs_{0.84}P$	6.5 nm	UID	QWs
18	InP	1.5 μm	UID	Cladding

III. RESULTS AND DISCUSSION

Fig. 2(a) shows the TEM image of the cross-section of sample A after ELOG InP. It is clearly visible in the TEM image that when the aspect ratio is small, even though defects from the seed layer are blocked by the dielectric mask, a large amount of them are able to infiltrate to the ELOG layer through the openings.

This results in ELOG layers with reduced defects but it is still not suitable for device fabrication. Fig. 2(b) shows the PL spectrum of the ELOG InP on Si along with that of the InP reference sample (planar). It is evident from the intensity of the PL spectra that the defects that have infiltrated to the ELOG layer are working as non-radiative centres thus resulting not only in lower intensity but also a larger full-width half maxima (FWHM).

Fig. 3(a) presents a two-beam diffraction contrast dark-field TEM image with $\{2\,0\,0\}$ family g-vector showing ELOG InP on Si of sample B taken near the $\langle 100\rangle$ direction. Since the aspect ratio is 2.3 ($>$1), we observe that the defects are completely blocked by the SiO_2 mask but also within the opening. Point A in Fig. 3(a) clearly indicates that defects are being blocked by the mask sidewalls in virtue of higher aspect ratio and the operative image force [22]. Nevertheless, the coalescence defects seem to appear, see point B. In addition stacking faults are also found to penetrate from the seed layer. What is particularly interesting is that none of these defects are visible in the TEM cross-section of ELOG InP on InP substrate as shown in our recent studies [23]

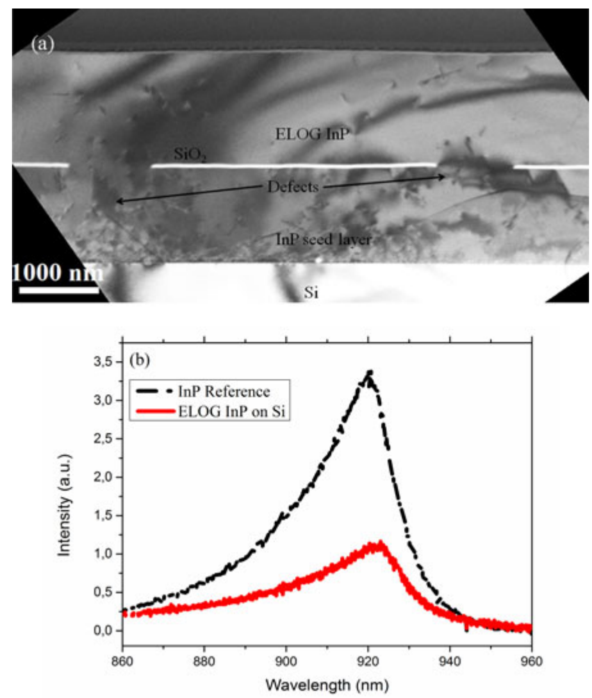

Fig. 2. (a) TEM image of cross-section of sample A, and (b) PL spectra of sample A compared with InP reference.

and those of Julian *et al.* [24]. This leads us to conclude that coalescence defects are not inherent to ELOG but are the results of the seed layer quality. The PL intensity reduction of ELOG InP/Si to $\sim$50% with respect to that of the reference sample, shown in Fig. 3(b), is also a result of these defects. Due to the too large spot size of the PL setup, PL is measured from the ELOG arising from multiple openings (and not on double openings) on sample *B*. Thus we believe that there is room for improvement of the ELOG layer through the improvement of the quality of the seed layer.

Fig. 4 shows the high resolution scanning transmission electron microscope (STEM) high angle annular dark field (HAADF) image of the interface between SiO_2 mask and ELOG InP arising from two openings of sample B. It is also taken along $\langle 100\rangle$ direction. Despite the coalescence defects, the interface formed by ELOG is found to be of high quality. The InP atomic

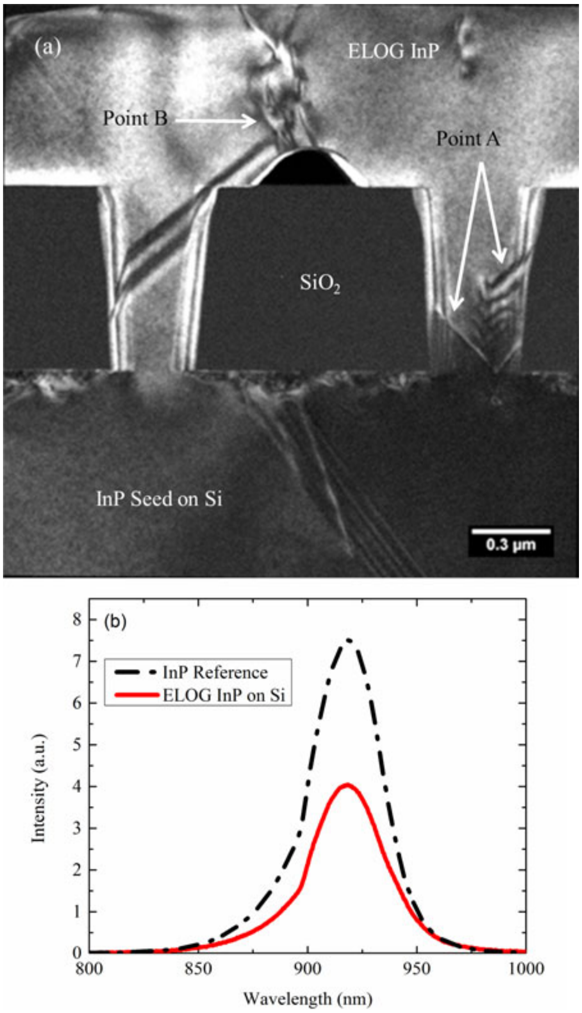

Fig. 3. (a) TEM image of cross-section of sample *B*. Point A indicates the blocked defects within the openings and point B indicates the defects generated due to coalescence of parallel growth fronts. The TEM images are high angular annular dark field (HAADF) images taken along ⟨1 0 0⟩ direction. (b) Room temperature μ-PL measured from multiple openings on sample B.

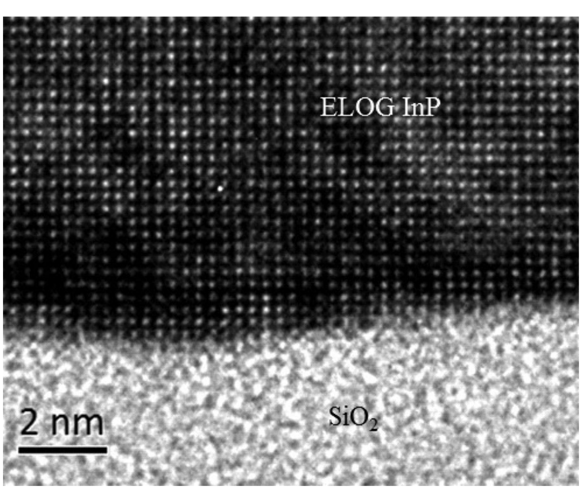

Fig. 4. HAADF STEM image of the clean interface between ELOG InP lattice and amorphous SiO_2.

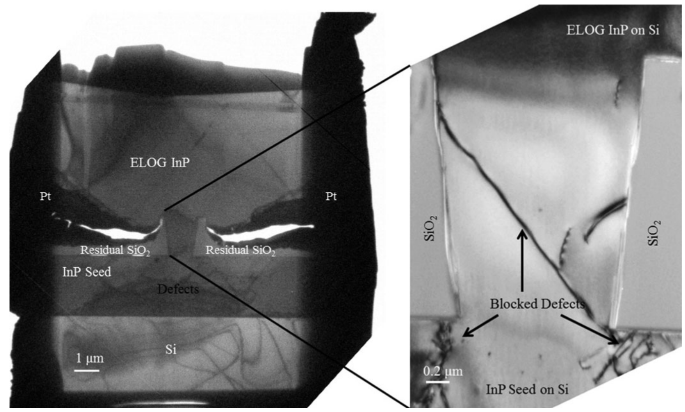

Fig. 5. TEM image of the lamella taken from sample C and magnified view of the opening clearly showing the blocking of defects in such high aspect ratio openings defined using optical lithography.

lattice extends and retracts to conform to the curvature of the SiO_2 surface.

Sample C with the patterns fabricated by optical lithography with an aspect ratio of 2 is particularly interesting since the mask and the opening dimensions are suitable for MCSEL structure enabling evanescent coupling and effective thermal dissipation. Here the ELOG InP was not allowed to coalesce and hence we eliminate the defects due to coalescence. The lateral growth in this sample is approximately 20 μm, which is sufficient to fabricate lasers on. Fig. 5 shows its TEM cross section. The edges of the lamella are also covered with platinum metal to avoid any etching from the focused ion beam employed to create the lamella and hence the width of ELOG is smaller than in reality. Different shades in the ELOG region are caused due to uneven thickness of the lamella which is caused due to such a large sample size and only specific regions could be thinned down to achieve high resolution TEM image. From the TEM image we can observe that SiO_2 mask is not stripped away completely and is providing support to the ELOG InP mesa. In case of real device fabrication the SiO_2 mask needs to be etched away selectively in such a way that it is only removed from the open areas and not beneath the ELOG layer. The SiO_2 layer beneath the ELOG layer is very important in cases where a Si waveguide is buried to achieve evanescent coupling. Fig. 5 demonstrates that in the case of completely straight sidewalls, an aspect ratio greater than 1 is needed to block all the threading segments not only in the mask region but also within the opening thus producing a defect free area even above the openings defined using optical lithography. This has been a major restriction for the ELOG approach when openings are defined using optical lithography to achieve large areas of defect free material since etching of very thick mask resulted in processing difficulties.

Fig. 6 shows the μ-PL spectra taken at room temperature of ELOG InP on Si on sample C. Comparable intensities and FWHM are observed for ELOG InP on Si with planar reference grown along with it. Some redshift can be observed in the μ-PL spectra of ELOG InP on Si of sample C, which has been identified to be due to the fact that the ELOG InP is under tensile strain [25], which was also confirmed by synchrotron x-ray

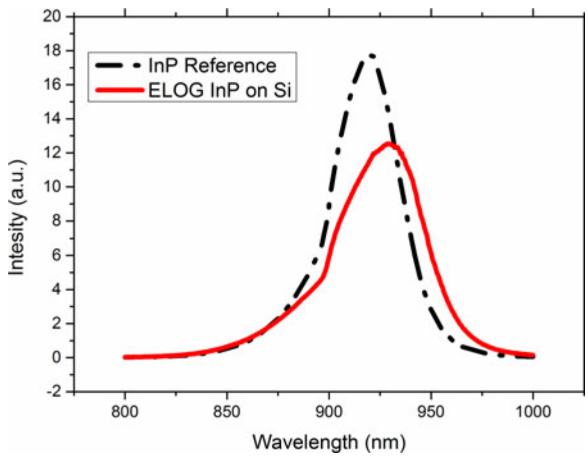

Fig. 6. μ-PL spetra of the sample C, comparable PL intensities and FWHM for ELOG InP on Si and InP reference grown along with it.

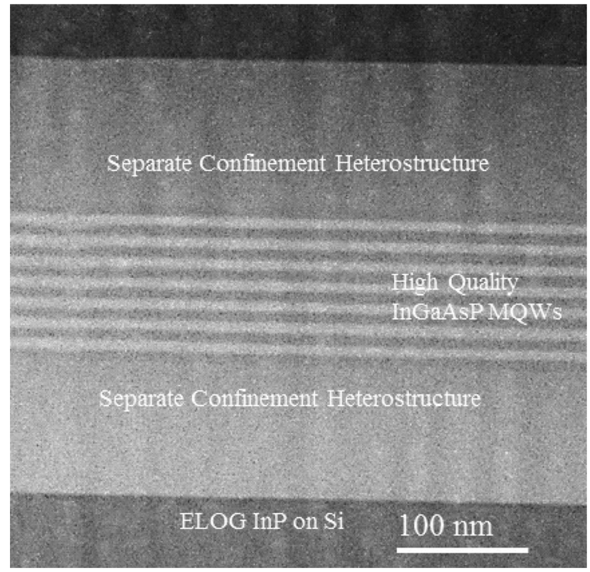

Fig. 7. TEM image of InGaAsP MQWs on uncoalesced ELOG InP on sample C.

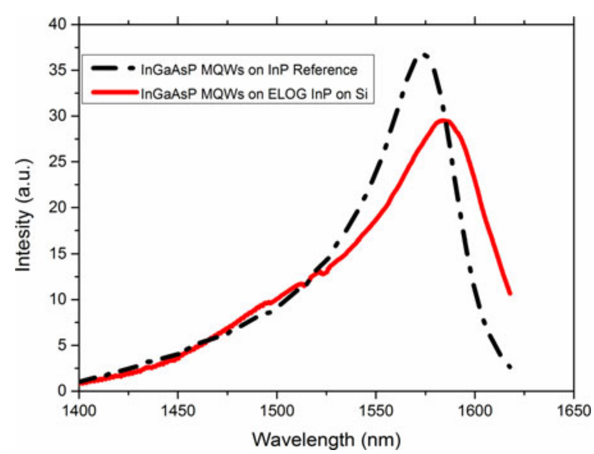

Fig. 8. μ-PL spectra of the MQWs grown on ELOG InP on Si.

topographic studies [26]. Our recent panchromatic cathodoluminescence studies reveal no observable defects in the uncoalesced ELOG InP even at very low ELOG InP thickness of $\sim$ 500 nm [23]. Based on this, the improved optical quality of the ELOG InP arising from sample C with respect to that on sample B is attributed to the uncoalesced form of the layer on the former, and the effect of growth temperature difference should be negligible. An increased thickness of the ELOG layer can also be a reason for the PL intensity enhancement in sample C, however, this effect is more tangible for coalesced layers as our previous studies indicate [27].Thus the best quality of ELOG layer can be obtained in the uncoalesced form resulting from high aspect ratio. Exact defect density of ELOG InP on sample C was not measured but the good optical quality of MQWs grown on it is supportive of its low defect density. Additional studies such as Raman spectroscopy and time resolved photoluminescence can throw more light on these layers which however were not conducted during this investigation.

After the growth of MQWs using MOVPE as described in the experimental section, TEM and μ-PL is done to check the uniformity of the MQWs across the ELOG layer. Fig. 7 shows the TEM image of MQWs grown on sample C. Highly uniform MQWs with very good interface are achieved on large areas of ELOG InP on Si.

Room temperature μ-PL measurements on the sample C show almost comparable intensities (within 85%) for MQWs grown on reference InP and ELOG InP on Si as shown in Fig. 8. Some red shift is visible in the PL spectra of MQWs on ELOG InP on Si; this is due to the same residual strain mentioned previously for the ELOG InP on Si layer.

IV. Summary and Conclusion

In line with our previously proposed strategy for realising a MCSEL [17], we have demonstrated ELOG InP on Si with a 2 μm thick mask layer that mimics the waveguide structure in the MCSEL. The opening width was 1 μm which leads to the aspect ratio (mask thickness/opening width) of 2, which is largely sufficient to filter the defects from the seed layer. In addition, the ELOG layers were not allowed to coalesce thereby additional defects that may form due to coalescence are hindered. TEM analysis shows that the defects are filtered not only by the mask but also by the opening due to the high aspect ratio. Besides, a high quality MQW with a photoluminescence emission of $\sim$1.5 μm is also demonstrated with very good interface. Interface investigation of ELOG InP on SiO_2 by STEM reveals that it is of high quality and the InP atomic lattice extends and retracts to conform to the curvature of the SiO2 surface. Although the STEM study was done on e-beam patterned sample, the results should be applicable even for the growth associated with optical lithography as conducted in this investigation.

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