WAFER-FUSED THIN FILM COOLER SEMICONDUCTOR LASER STRUCTURES

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Abstract

We examine the cooling requirements and temperature stabilization needs of semiconductor lasers with emphasis on vertical cavity surface emitting laser (VCSEL) arrays. Semiconductor lasers in both in-plane and vertical cavity geometries are capable of generating large heat power densities on the order of kW/cm^2 over areas as small as 100 μm^2. When cooling of the laser is needed, the cooler should be able to provide similar amounts of heat pumping. For these large amounts of heat pumping a thin-film cooler structure is needed, especially if individual devices of an array must have precise temperature stabilization. Integration of the laser and thin film cooler by Au-Au wafer fusion is proposed. The fusion of the two interfaces is accomplished by mass transport in the deposited Au-films, which can be achieved under pressure at elevated temperatures. The quality of the fused interface is studied and preliminary experimental results are presented.

Introduction

Temperature stabilization for laser sources in high speed and wavelength division multiplexed (WDM) optical telecommunication systems is typically accomplished with thermoelectric coolers (TECs). While the TECs have been successfully used in commercial components, there are many incompatibilities between these devices and semiconductor lasers. Whereas the lasers use integrated circuit technology for batch fabrication, TECs are individually fabricated by hand or by automated machines. The result is an increased cost and reduced reliability [1-2]. In addition, the lasers are of small size and generate large heating densities while the TECs are of large size and are capable of providing only small cooling power densities. Since the cooler is placed beneath the laser substrate in various kinds of packages, the generated heat has a chance to spread out before reaching the top of the cooler. While this relaxes the requirement for large cooling power density from the cooler, it also introduces a substantial thermal resistance between the heat source (laser active region) and sink (cooler). This allows the operating temperature of the laser to be significantly higher than the cooler itself.

The approach taken in this work was to remove the substrate, and instead integrate the laser directly with a thin-film cooler structure. Thin-film SiGe/Si superlattice coolers were chosen for this integration. In the process used, wafers were bonded together using an Au-Au fusion process.

VCSEL Thermal Issues

The specific laser source chosen for investigation in this work was a long wavelength VCSEL [3]. Due to their low cost and high-speed direct-modulation capabilities, they are attractive sources for short and medium range optical fiber networks, optical interconnects, and parallel optical data processing [3-4]. However, before these devices can be deployed in such systems, the performance-limiting effects due to Joule heating must be solved. Unfavorably, the active region typically operates at a substantially higher temperature than that of the heat sink, owing to the considerable thermal resistance between the heat source and sink. The elevated temperature increases loss mechanisms in the laser such as carrier leakage and enhanced Auger processes in the active region. Figure 1 shows the measured output power versus current and ambient temperature for a typical device. The initial increase in threshold current and reduction in differential efficiency are related to the steadily increasing heat sink temperatures while the roll off at higher currents is due to the additional rise in temperature from Joule heating. Figure 2 plots the experimental internal active-region temperature of a VCSEL versus current for a heat sink temperature of 20 °C. For moderate output

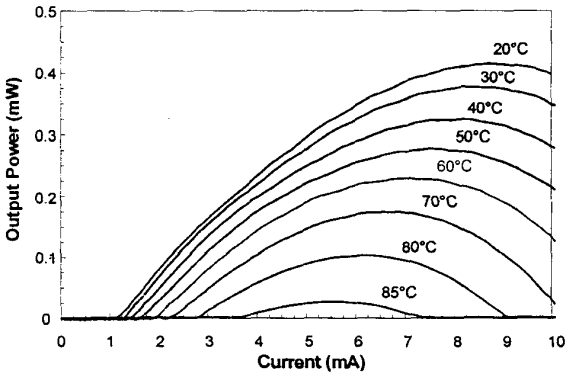

Fig. 1 Output power versus current and temperature for a typical VCSEL.

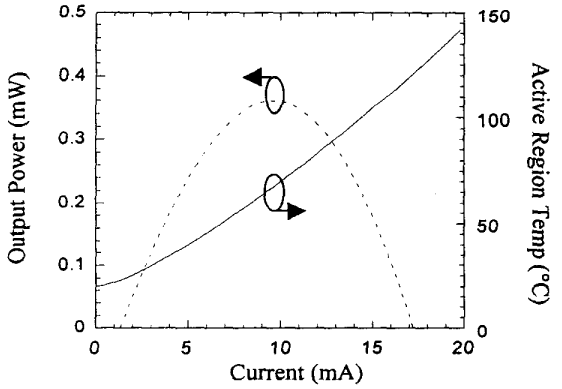

Fig. 2 Active region temperature versus current plotted alongside output power for a heat sink temperature of 20 °C.

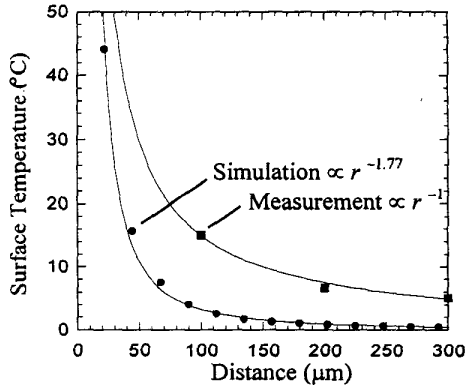

Fig. 3 Comparison of simulated and measured surface temperature versus distance from the VCSEL heat source.

powers, the active region can be more than 30 °C above the heat sink temperature. Therefore, even with a thermoelectric cooler beneath the substrate, the device temperature can be significantly higher. This can be even greater for structures that include bottom distributed Bragg reflector (DBR) mirrors which have a larger thermal resistance.

The heat generated by a single VCSEL can also impact the operation of other devices in an array through thermal crosstalk. To evaluate the crosstalk theoretically, a 3-D ANSYS thermal simulation [5] was used to solve the surface temperature surrounding a VCSEL under operation. The simulation assumed a 10-μm pillar diameter sitting on a 7.7-μm-thick GaAs/AlAs DBR and 300-μm-thick GaAs substrate. A worse case condition of a 100 °C operating temperature was assumed. An approximate analytical formula for the surface-temperature distribution can be expressed as:

$$T(r) = \frac{P}{2\pi\beta_{lat} r} \qquad (1)$$

where P is the power of the heat source, β_{lat} is the effective lateral thermal-conductivity, and r is the distance from the source [6,7]. Figure 2 compares the simulation result to experimentally measured surface temperatures. The temperature can be seen to drop off very quickly within 20 to 30 microns. While the experimental values fit well to equation 1, the simulation values dropped off more steeply showing a stronger inverse dependence on distance. This can be explained partly by the presence of a boundary thermal resistance at the bottom of the heat sink which was not included in the simulation. Evidently, the thermal floor in figure 2 depends on the mounting of the sample to the heat sink. The experimental values show about 5% of the VCSEL's peak temperature is present 300-μm away from the sample. If another device in the array was also operating, the elevated temperature would affect the output power and emission wavelength. As an example, if a single VCSEL in a WDM array with 300-μm-pitch employing a wavelength spacing of 0.2 nm requires a temperature stabilization of ± 0.5 °C, the nearest operating device could not heat up beyond 5 °C unless some other active tuning mechanism is used. Thermal crosstalk may be even more of an issue for structures that employ lateral heat spreading layers such as in all-epitaxial long wavelength VCSELs [8]. Reduction in crosstalk is possible by short-circuiting the lateral heat spreading with flip-chip bonding to a good heat sink, but there would still be no control over emission wavelength. Flip chipping to Si-based micro-coolers would allow for integration with both cooling elements and drive electronics.

Heterogeneous Integration

Heterogeneous integration offers more flexibility in design compared to monolithic integration as each device is seperately optimized. Since this allows for the use of dissimilar materials, the best available thin-film micro-cooler should be used. Recent work on $Si_{1-x}Ge_x$/Si [9] and SiGeC/Si [10] superlattice structures have shown impressive cooling performance. Fan *et. al.* have demonstrated maximum cooling values of 4 to 12 K with SiGe/Si superlattices and cooling power densities exceeding 500 W/cm^2 for SiGeC/Si superlattices. These devices are currently being investigated for integration with Si-based microelectronics, and work is underway to further improve performance with thermionic emission in heterostructures [11].

To achieve the heterogeneous integration, several different bonding methods were evaluated, including the use of conductor loaded adhesives and solders. While these types of joining materials allow for bonding of non-uniform surfaces, they suffer from very poor thermal conductivities. Instead, the method chosen was to transfer the InP laser epi-layer onto a Si substrate by Au-Au fusion. This process was attractive since bonding parameters had already been optimized in previous work [12]. Characterization samples were used to determine the feasibility of the process for thermionic cooler fabrication. Figure 3 shows the steps used in the Au-Au bonding. After sample cleaning, metal layers of Ti/Pt/Au 500/1000/15000Å were deposited by e-beam evaporation. The Ti acted as an adhesion layer while the Pt prevented Au-spiking into the semiconductor during the bonding process. A thickness of 1000Å was experimentally determined to be the minimum for processes using temperatures below 400 °C. The thick Au-layer was chosen for enhanced heat spreading and to accommodate any non-planarities in either surface. The samples were then brought into contact and held under pressure (~ 70 kPa) using a

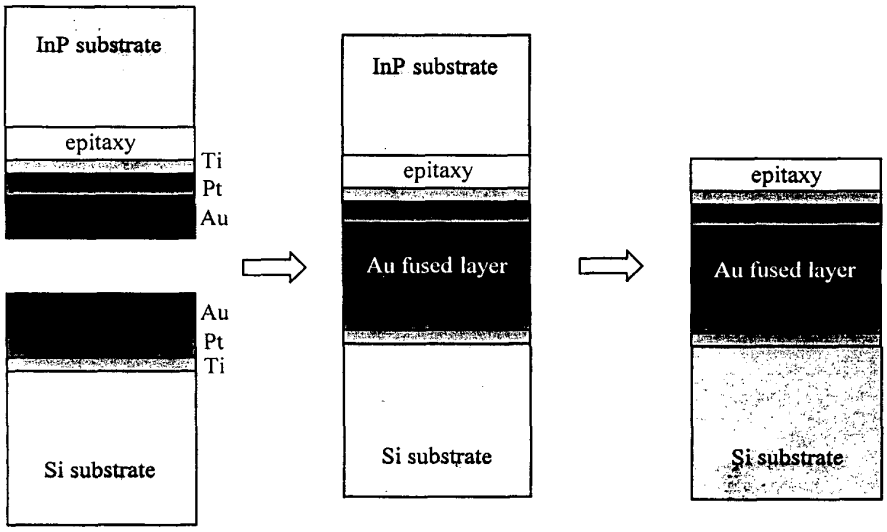

Fig. 4 Au-Au fusion process for transferring epitaxial layers from the InP growth substrate to a Si substrate. The steps are (a) E-beam evaporation of Ti/Pt/Au metallization, (b) Au-Au fusion under pressure and at high temperatures, and (c) InP substrate removal. The process can be generalized to any surrogate substrate.

graphite fixture placed in a vacuum furnace with nitrogen overpressure. The temperature was ramped up at 2°C/min to a temperature of 350 °C, held for five minutes, and then ramped down at the same rate. The slow ramping was to reduce stress caused by the coefficient of thermal expansion (CTE) mismatch between the wafer and metal. After the fusion, the InP substrate was etched off, and the remaining epi layers were examined under an optical microscope. Test structures indicated that roughly 50% of the devices bonded. While the quality of the bond is difficult to evaluate visually, the mesas that did remain attached survived violent agitation with solvents. Further electrical and thermal evaluation of the test structures and of integrated devices should indicate the quality and uniformity of the Au-Au bond. Evaporating a thin layer of Sn after the Au evaporation is expected to help with the reliability of this process since the solder can actually reach its melting temperature and re-flow to fill in any voids. Any addition of Sn would increase the thermal resistance, and must be considered when deciding how thick a layer to use.

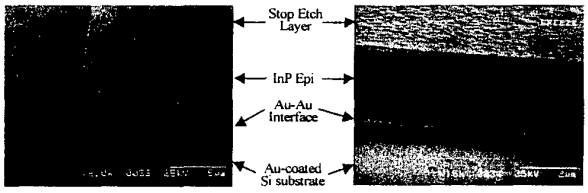

Fig. 5 SEM of a Au-Au bonded test structure indicating the various regions and interface.

Conclusions

There are many issues to consider for integration of cooling devices with laser sources. While conventional thermoelectric coolers currently provide larger temperature differences, they can only loosely control the temperature of the substrate and are limited in their cooling power density. Thin-film coolers can be integrated with optoelectronic devices to provide active temperature stabilization, wavelength tuning, and large cooling power densities far beyond bulk Peltier coolers. Heterogeneous integration allows for separate optimization of the cooler and laser structures. The use of Au-Au fusion should provide an ideal interface both electrically and thermally, however further work is needed to improve the bonding uniformity and yield.

Acknowledgments

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