

## Cooling Power Density of SiGe/Si Superlattice Micro Refrigerators

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### ABSTRACT

Experiments were carried out to determine the cooling power density of SiGe/Si superlattice microcoolers by integrating thin film metal resistor heaters on the cooling surface. By evaluating the maximum cooling of the device under different heat load conditions, the cooling power density was directly measured. Both micro thermocouple probes and the resistance of thin film heaters were used to get an accurate measurement of temperature on top of the device. Superlattice structures were used to enhance the device performance by reducing the thermal conductivity, and by providing selective emission of hot carriers through thermionic emission. Various device sizes were characterized. The maximum cooling and the cooling power density had different dependences on the micro refrigerator size. Net cooling over 4.1 K below ambient and cooling power density of 598 W/cm<sup>2</sup> for 40 × 40 μm<sup>2</sup> devices were measured at room temperature.

### INTRODUCTION

With the rapid development of VLSI technology, heat generation and thermal management are becoming barriers, preventing increased clock speeds and decreased feature sizes. Thermoelectric (TE) coolers based on bulk Bi<sub>2</sub>Te<sub>3</sub> are commonly used for electronic and optoelectronic device cooling, but they cannot be directly integrated with the IC fabrication process. There has been an increasing demand for localized cooling and temperature stabilization of microelectronic and optoelectronic devices. Recently p-type BiTe/SbTe thin film coolers have been utilized demonstrating a high thermoelectric figure-of-merit and cooling power density [1]. Si-based microcoolers are attractive because they have the potential for monolithic integration with Si microelectronics. SiGe is a good thermoelectric material especially for high temperature applications [2,3], and superlattice structures can further enhance the cooler performance by reducing the thermal conductivity between the hot and the cold junctions, and by selective emission of hot carriers above the barrier layers in the thermionic emission process [4-21]. Thin film resistors were integrated with cooler devices and they were used to characterize the cooling performance with a heat load.

### MATERIAL GROWTH

The structure of the microcooler sample consisted of a 3 μm thick 200 × (5nm Si<sub>0.7</sub>Ge<sub>0.3</sub> /

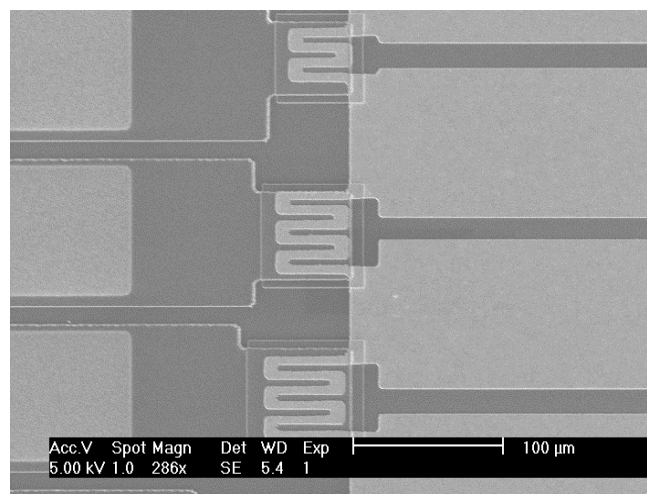
10nm Si) superlattice grown symmetrically strained on a buffer layer designed so that the in-plane lattice constant was approximately that of relaxed  $\text{Si}_{0.8}\text{Ge}_{0.2}$ . The doping level is  $5 \times 10^{19} \text{ cm}^{-3}$  for both the superlattice and the buffer layer. A  $0.5 \mu\text{m}$   $\text{Si}_{0.9}\text{Ge}_{0.1}$  cap layer was grown on the superlattice with the top  $0.25 \mu\text{m}$  doped to  $2 \times 10^{20} \text{ cm}^{-3}$  to reduce the ohmic contact resistance. This  $\text{Si}_{0.7}\text{Ge}_{0.3}/\text{Si}$  superlattice has a valance band offset of about 0.2 eV. Thermionic emission of hot holes over this barrier can produce cooling. In addition, a superlattice structure has many interfaces that increase phonon scattering, and therefore lower thermal conductivity. The samples were grown with a molecular beam epitaxy (MBE) machine on five inch diameter (001)-oriented Si substrates, doped to  $0.001 \sim 0.006 \Omega\text{-cm}$  with Boron.

## DEVICE FABRICATION AND MEASUREMENTS

Mesas  $0.6 \mu\text{m}$  high were formed using reactive ion etching down to the SiGe/Si superlattice layer. A 100 nm titanium layer was deposited to both form a titanium silicide layer on the Silicon surface and to act as a metal barrier to separate SiGe and Al. Subsequently a  $1 \mu\text{m}$  thick aluminum layer was deposited. To facilitate wire bonding, additional metal layers of titanium and gold were used. The device was annealed at  $450 \text{ }^\circ\text{C}$  for 5 seconds.

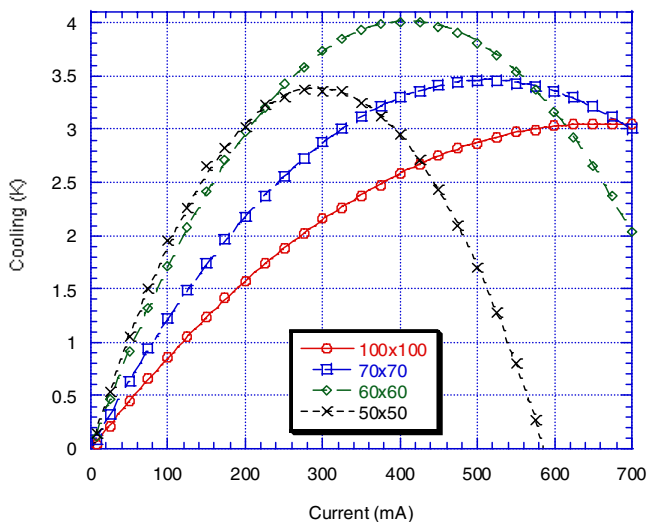
In order to facilitate the integration of a thin film resistor on top of the device, the top metal contact was extended to the side with a  $0.3 \mu\text{m}$  thick  $\text{SiN}_x$  insulating layer underneath. Heat flow from the side contact to the top of the device was taken into account, and a side electrode pad was optimized to get a balance between resistive Joule heating and heat conduction. A thin film metal resistor was integrated into the device and used as a heat load for the cooling power density measurement. A scanning electron micrograph (SEM) image of the processed devices is shown in Fig. 1.

Micro refrigerators were tested at room temperature. Device cooling was measured using two micro thermocouples; one thermocouple with  $\sim 50 \mu\text{m}$  bead size was placed on top of the cooler and another one on the substrate far away from the device. Fig. 2 shows the test results for coolers (processed without heater on top) ranging in size from  $40 \times 40$  up to  $100 \times 100 \mu\text{m}^2$ . The



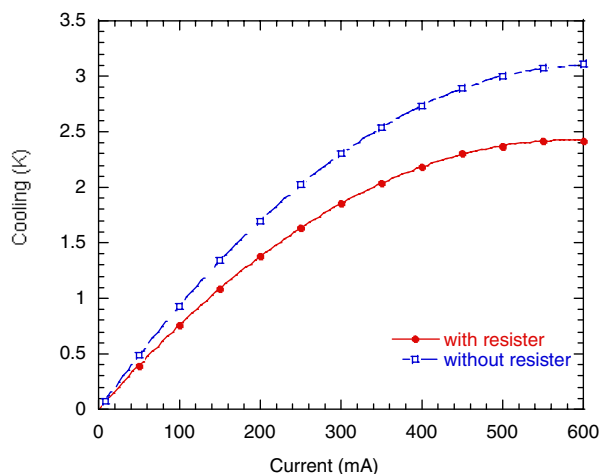
**Figure 1.** Processed SiGe/Si coolers with integrated thin film metal wire resistors.

maximum cooling of 4.1 K was measured for the  $60 \times 60 \mu\text{m}^2$  device. The cooling power of the device was measured using the integrated thin film resistor, which applied a heat load to the cooler.



**Figure 2.** Cooling measured for  $50 \times 50 \mu\text{m}^2$ ,  $60 \times 60 \mu\text{m}^2$ ,  $70 \times 70 \mu\text{m}^2$  and  $100 \times 100 \mu\text{m}^2$  SiGe/Si coolers.

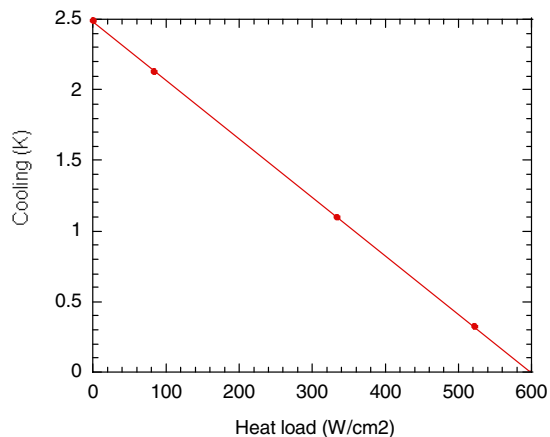
Figure 3 shows the cooling measured on a  $100 \times 100 \mu\text{m}^2$  device that incorporated a thin film heater. Due to the extra thermal conduction paths from the top side of the cooler to the substrate, the absolute cooling is reduced from 3.2 K to 2.4 K. A constant electric current was



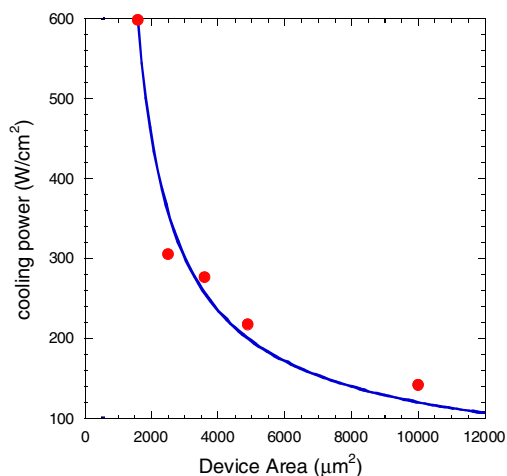
**Figure 3.** Cooling comparison of  $100 \times 100 \mu\text{m}^2$  coolers with and without thin film resistor on the top.

applied through the metal wire to provide a constant thermal load to the cooler while the cooling was measured. The maximum cooling power is defined as the heat load power that makes the device's maximum cooling temperature equal to zero.

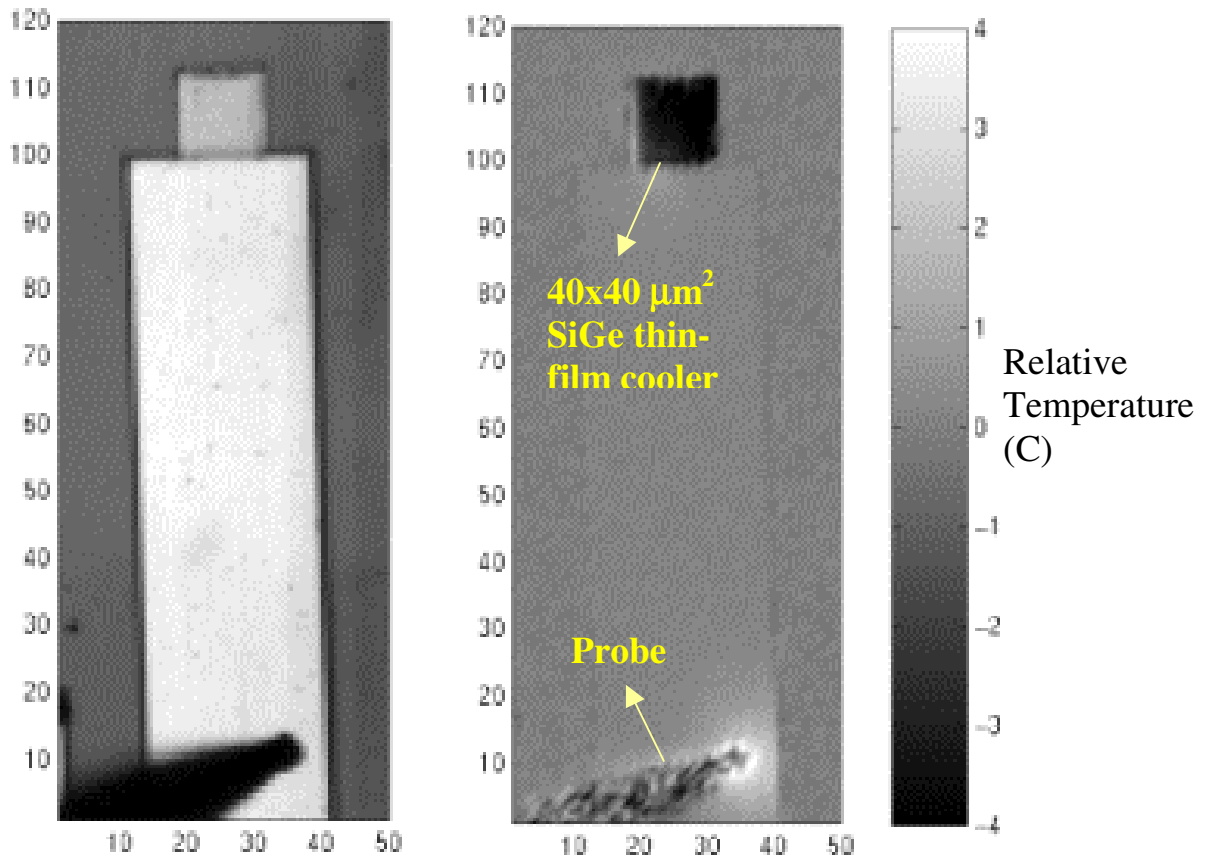
The measured cooling power density for the  $40 \times 40 \mu\text{m}^2$  device is shown in Fig. 4. The maximum cooling power density for various device sizes is shown in Fig. 5. The largest cooling measured,  $598 \text{ W/cm}^2$ , was obtained for the smallest device ( $40 \times 40 \mu\text{m}^2$ ).



**Figure 4.** Measured cooling power density for  $40 \times 40 \mu\text{m}^2$  SiGe/Si cooler at room temperature.



**Figure 5.** Cooling power density for various cooler sizes and the fitting with  $1/(aA^{1/2} + b)$ , where  $A$  is the device area and  $a$  and  $b$  are constants.



**Figure 6.** Temperature distribution on top of a 40x40 micron square thin film cooler measured using thermoreflectance imaging. The stage temperature is 25C. The applied current is 250mA.

In addition to the micro thermocouple measurements, a thermoreflectance imaging method<sup>22</sup> was used to study the device's thermal distribution. Fig. 6 shows the temperature distribution for a  $40 \times 40 \mu\text{m}^2$  device. One can see uniform cooling on top of the micro refrigerator as well as localized heating near the current probe. The top metal contact layer was extended far away to the side in order to eliminate the effect of the current probe heating on the cooler's performance. Fig. 6 also shows how the localized temperature at any specific location on the chip surface can be controlled accurately.

## DISCUSSION

According to conventional bulk thermoelectric cooler models, maximum cooling is determined by the TE figure-of-merit and is independent of the cooler size. However, with device minimization, the cooler's thermal and electrical resistances become very small and non-ideal effects, such as metal-semiconductor contact resistance and heat sink thermal resistance,

must be considered in the device modeling. These non-ideal effects not only reduce the maximum cooling but also make the cooling performance device size dependent. For example, the cooler's thermal resistance is inversely proportional to the cooler's area, while the thermal resistance of the silicon substrate beneath the device is inversely proportional to the square root of the cooler's area. The relationship of the substrate's thermal resistance and the device's area can be expressed as:

$$R_{\text{sub}} = \alpha\pi^{1/2}/4\beta A^{1/2} \quad (1)$$

where  $R_{\text{sub}}$ ,  $\beta$ , and  $A$  are substrate thermal resistance, thermal conductivity of the half space substrate, and device area, respectively. The  $\alpha$  is a coefficient, and a value of about 0.761 was obtained in our cooler simulation and ANSYS model curve fitting [23,24]. The ratio of the cooler's thermal resistance to the substrate's (heat sink) thermal resistance is inversely proportional to the device size. Therefore as the device gets smaller, the substrate becomes closer to an ideal heat sink and the overall micro refrigerator's cooling performance improves. Another difference from conventional bulk TE coolers is that the thin film micro coolers described here are single element devices instead of the p- and n-type array structures. One should consider the heat conduction from the side contact to the cold junction of the device. Since in these structures the side contact scales with the linear dimension of the cooler, larger devices tend to be less affected by the heat conduction from the side. Because of the interplay of the above two non-ideal effects, there is an optimal device size for the maximum cooling temperature. This is shown in the measurements in Fig. 2 where  $60 \mu\text{m} \times 60 \mu\text{m}$  devices show the largest cooling.

For the cooling power density measurements, the main limiting factor is the total thermal resistance between the topside of the cooler and the heat sink. Detailed modeling [25] has shown that in the range of our device sizes (2000-10,000 micron square), the cooling power density may be described by the expression  $1/(a A^{1/2} + b)$ , where  $A$  is the device area and  $a$  and  $b$  are constants. The fitting in Fig. 6 matches very well the measurement results for various device sizes and it confirms the better cooling power performance of the smaller refrigerators.

## CONCLUSION

In summary, with standard IC processing technology, thin film metal wire resistors were integrated with the cooler devices and they were used as controllable electrical thermal loads. Cooling power density of  $598 \text{ W/cm}^2$  for  $40 \times 40 \mu\text{m}^2$  coolers and cooling up to 4.1 K for  $60 \times 60 \mu\text{m}^2$  devices were measured at room temperature. This shows the possibility for integrated and localized cooling of high power electronic and optoelectronic devices with micro thin film refrigerators.

This work was supported by the DARPA HERETIC and the Packard Foundation.

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