Design and Implementation of an Integrated Reconfigurable Silicon Photonics Switch Matrix in IRIS Project

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***Abstract*—This paper aims to present the design and the achieved results on a CMOS electronic and photonic integrated device for low cost, low power, transparent, mass-manufacturable optical switching. An unprecedented number of integrated photonic components (more than 1000), each individually electronically controlled, allows for the realization of a transponder aggregator device which interconnects up to eight transponders to a four direction colorless-directionless-contentionless ROADM. Each direction supports 12 200-GHz spaced wavelengths, which can be independently added or dropped from the network. An electronic ASIC, 3-D integrated on top of the photonic chip, controls the switch fabrics to allow a complete and microsecond fast reconfigurability.**

***Index Terms*—3-D photonic integration, colorless, directionless and contentionless (CDC) reconfigurable add and drop multiplexers (ROADM), integrated optical circuits, micro-ring resonator switch element, optical switches, photonic system-on-chip, silicon photonics, transponder aggregator, optical switching matrix.**

Manuscript received January 29, 2016; accepted March 20, 2016. This work was supported by the European Union's Seventh Framework Program FP7/2007–2013 under Grant 619194. *(Corresponding author: Francesco Testa.)*

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Digital Object Identifier 10.1109/JSTQE.2016.2547322

I. Introduction

NEXT generation reconfigurable add and drop multiplexers (ROADM) architectures will be more flexible with respect to the currently deployed optical nodes.

New ROADMs will operate in colorless, directionless and contentionless (CDC) mode [1]. This will extend the flexibility and automation to the optical node end points where the transponders are ordinarily interconnected to the node, avoiding any manual intervention in case of their reconfiguration. The CDC add/drop access will enable the operator to optimize resource utilization, and support re-routing functions in the event of faults in a cost effective manner. To add such flexibility to the conventional ROADMs that uses free space optics based 1xN wavelength selective switches (WSS) for optical line switching, new architectures have been proposed [2] based on the use of an additional block denoted as transponder aggregator (TPA) replacing the fixed WDM multiplexer and demultiplexer. An example of a four directional CDC ROADM is depicted in Fig. 1.

The TPA is a switching sub-system used to distribute selected combs of wavelengths received from WSS device to transponders without any limitation in term of wavelengths or directions. In the opposite direction, the TPA is used to combine any wavelengths from transponders to any WSS. TPA devices commercially available are based on mature PLC technologies [2], [3]. Very recently new silicon photonic integrated TPA devices have been described where a matrix of Mach–Zehnder interferometer based 2×2 switch elements and a cyclic 8×8 AWG are integrated on a same chip [4], [5]. Silicon Photonic integration is a very interesting technology due to its potential of implementing photonic switching devices with unprecedented low cost, fast response time (microsecond range) and small footprint characteristics. In FP7 IRIS project (Integrated Reconfigurable silicon photonic based optical Switch [6]) a completely new concept of integrated TPA device has been introduced and developed.

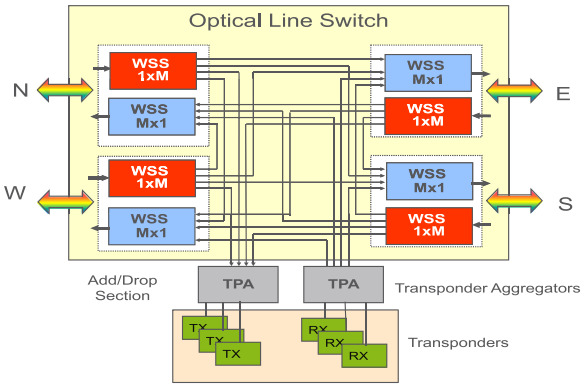

Fig. 1. Colorless-directionless and contentionless ROADM.

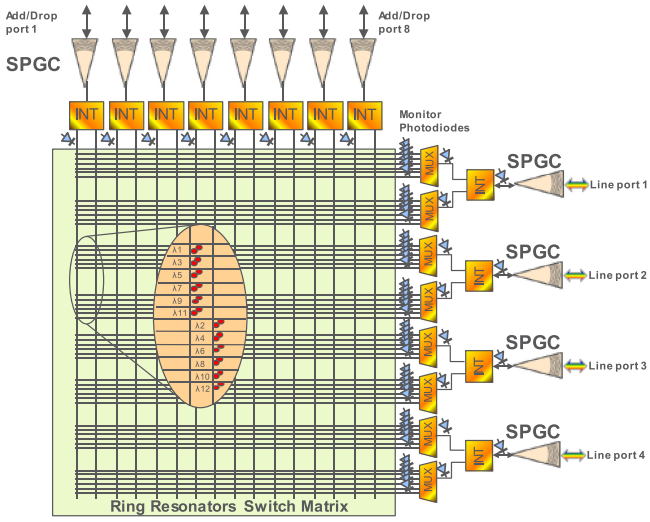

Fig. 2. Architecture of IRIS TPA.

II. Device Architecture

The architecture of the integrated TPA is shown in Fig. 2. It is worth noting that the same device can be used for two functions: dropping WDM channels from the input line ports to local drop ports and adding WDM channels from local add ports to the output line ports: this can be achieved by simply inverting the direction of the optical flows thanks to the definition of a common architecture.

In the Drop switch, four sets of up to 12 WDM channels, 200 GHz spaced, arrive at each of the four input line ports and are coupled to the chip by single polarization grating couplers (SPGC). Interleavers blocks separates the input channels into odd and even channels to increase the wavelength spacing in the switching matrix and to relax the channel isolation requirements. Then, two types of demux blocks, one working with odd wavelengths and one with even wavelengths, demultiplex the odd/even separated channels. At the demux output, the signals are sent to the switching matrix constituted by an optical crossbar of micro-ring resonators (MRR) switch elements for which a detailed design analysis has been presented in Ref. [7]. The matrix has 4×12 rows, each one of which is able to switch a certain wavelength, and 8×2 columns, which number the drop ports connected to optical receivers. In the switching matrix, the demultiplexed signal travels on a row until it gets to the column connected to the drop output. At this crossing point, there is one or two MRRs, which are thermally tuned (activated) in resonance with the signal wavelength. Therefore, the signal couples to the resonators and is transferred to the corresponding drop column. Note that, two waveguides connect to each drop port where one handles the odd wavelengths while the other the even wavelengths. An interleaver recombines the odd and even wavelengths to the drop port where a SPGC allows coupling to an optical fiber.

In the Add switch (see Fig. 2), eight tunable transmitters add a WDM signal to the chip by the SPGC. Interleavers at each add input direct the odd and even wavelengths to the proper columns in the matrix switch. All the ring resonator resonances in the matrix are off with respect to the signal wavelength. Only those ring resonators at the cross with the proper direction to which the signal has to be added are activated. Therefore, the signal is deviated horizontally toward the output multiplexer. After the multiplexer the signals reach an interleaver which combines odd and even wavelengths to the same output fiber.

Monitor photodetectors are placed at strategic input and output location to allow monitoring the different blocks.

III. Crosstalk Analysis

Achieving a low level of crosstalk is one of the most challenging aspects of the silicon photonics TPA architecture presented here. Crosstalk is a system effects coming from the finite isolation of the various component blocks cascaded in the switch. Two types of optical crosstalk are defined according to Ref. [8]: interferometric crosstalk (C_I), arising from disturbing channels at the same wavelength of the wanted channel and inter-channel crosstalk (C_C), arising from the disturbing channels at wavelengths different from that of wanted channel.

Since the aim of this paper is the definition of the switch architecture, only the most detrimental crosstalk sources will be reported here. In fact, they mostly dictate the requirements of the transfer function for the MRR switch element, the mux/demux and the interleaver. A complete crosstalk analysis of our TPA is going to be reported in a future paper.

A. Add Switch Crosstalk

In the Add switch, unwanted signals at the same wavelength of the wanted signals cause the crosstalk. Hence, for the add matrix only interferometric crosstalk is considered.

The most detrimental interferometric crosstalk arises from the MRRs set in the OFF condition. In the worst case, in our four line ports TPA, up to three disturbing channels at the same wavelengths could be present and they are attenuated with respect to the wanted channel by an amount equal to the unidirectional isolation I (dB) of MRR: for that reason $-I_{x-y}$ is denoted as the ratio of the power (expressed in dB) of the disturbing channel at wavelength x coming from the add input y, relative to the power of the wanted channel. A sketch indicating how crosstalk is generated in MRR set in OFF is depicted in Fig. 4(a).

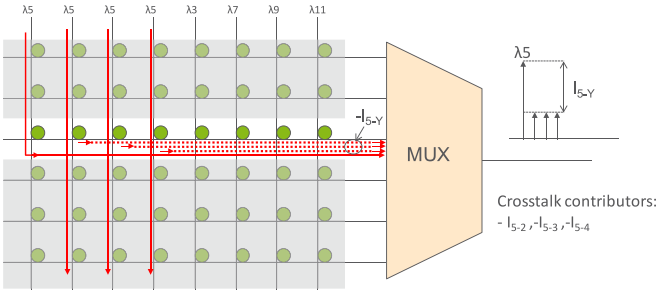

Fig. 3. Interferometric crosstalk components in the add TPA.

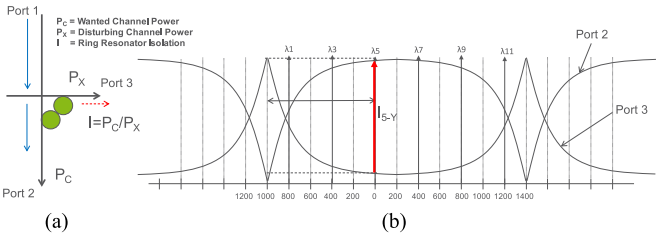

Fig. 4. (a) Crosstalk in MRR set in OFF. (b) Position of MRR in OFF for both add and drop TPA.

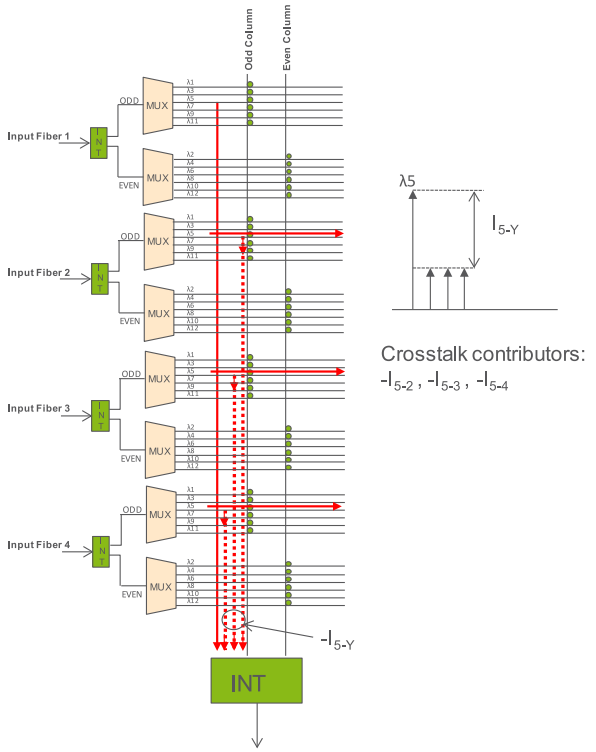

Fig. 5. Interferometric crosstalk components in the drop TPA.

For our worst case crosstalk analysis wavelength λ_5 has been selected as wanted channel to be switched toward one of the multiplexer because it is, together with the wavelength λ_7 the most central wavelengths with highest crosstalk (see Fig. 3). The most detrimental crosstalk contributions are due to disturbing channels at the same wavelength which, during their vertical travel along the column, leaks power in correspondence to the crossing of the MRR in row 3 of the matrix where the wanted λ_5 channels is also guided.

Due to non-ideal isolation of the MRR, together with the wanted channels at λ_5 other three disturbing signals (to be added on other fiber lines) at the same wavelength can be present whose relative power (expressed in dB) is denoted as $-I_{5-x}$ (see Fig. 3).

To keep this type of crosstalk contributions as low as possible, the resonance of the MRRs in each row are kept reasonably far from the channel wavelengths when the micro-ring is in OFF. In Fig. 4(b) they are kept 1000 GHz far from the wavelength channel to benefit from the high isolation achieved in this condition.

Additional interferometric crosstalk contributions are given by the non-ideal isolation of the waveguide crossing and interleaver but they are not reported here because their power level is guaranteed by design to be negligible by setting the isolation sufficiently high (>45 dB for waveguide crossing and >20 dB for interleavers).

B. Drop Switch Crosstalk

In the Drop switch the crosstalk is constituted by the presence, together with the wanted signals to be dropped to the optical receiver in one column, of unwanted power at the same wavelength (interferometric crosstalk) and at different wavelengths (inter-channel crosstalk) generated inside the optical switching matrix. In the following only interferometric crosstalk will be reported due to its most detrimental effect while inter-channel crosstalk will be dealt in a future paper dedicated to the crosstalk analysis.

The interferometric crosstalk contributions are shown in Fig. 5. $-I_{x-y(dB)}$ is the power (relative to the wanted signal) leaked by the disturbing channels at wavelength λ_x (the same of the signal), coming from the input line y.

In this case, for simplicity, we have set the same reference channel λ_5, although now all the wavelengths have the same behavior.

The interferometric crosstalk components are originated by the non-ideal isolation of the MRRs set in OFF along the drop column that are traversed horizontally by the three disturbing channels at the same wavelength of the wanted channel but travelling toward other drop columns. In fact while the wanted channel is intentionally dropped vertically along the column toward the receiver, from input line 1 (see Fig. 5), up to three disturbing channels coming from other input line (2, 3 and 4) are leaked and they are also guided together with the wanted signal along the same column.

As in the add matrix, in order to keep this type of crosstalk contributions as low as possible, the resonance of the MRR is kept reasonably far from the channel wavelengths when the MRR is in OFF. It is also kept 1000 GHz far from the wavelength channel to benefit from the high isolation achieved in this condition (see Fig. 4(b)).

Other additional interferometric crosstalk contributions are caused by the non-ideal isolation of the waveguide crossing and interleavers but they are not reported here because their power

level is negligible as guaranteed by design by setting sufficiently low the relative isolation.

In the drop matrix inter-channel crosstalk is also present but it will not be discussed in this paper as it is much less detrimental with respect to interferometric crosstalk that is the one dictating the requirements of the optical elements.

IV. Requirements and Specifications

The requirements and specifications of the different integrated optical components have been defined on the basis of the maximum crosstalk level accepted by the system and on the maximum allowed insertion loss. The maximum accepted crosstalk level has been specified to be the one for which the power penalty is not exceeding 1 dB for both add and drop switching sub-systems. For this calculation the equation and graphs reported in [8] have been taken as reference.

The strategy to fulfill these requirements has been the following: the dominant crosstalk source must be the interferometric crosstalk to which the 1 dB penalty is assigned.

Among the various crosstalk sources the non-ideal isolation of the MRRs must be the dominant one.

According to the ITU-T recommendations for optical system design [8] the following equation and criteria have been adopted to calculate the wanted isolation of the MRR, I_{X-Y}:

$C_{I(dB)} = +\,d - I_{X-Y} + 10\log10(k-1)$

Where:

$C_{I(dB)=}$ Ratio of the disturbing power (not including ASE) to the wanted power within a single wavelength

d(dB) = max power difference between channels at the same wavelength

k = max number of channels at the same wavelength

I_{X-Y} (dB) = minimum isolation required for MRR

In our case k = 3, d = 2 dB for the add matrix and 4 dB for the drop matrix. The maximum crosstalk level for 1 dB power penalty is $C_I = -27$ dB [8, Fig. 9.19].

This gives a minimum isolation required $I_{X-Y} = 34$ dB for the add matrix and $I_{X-Y} = 36$ dB for the drop matrix.

Regarding the maximum accepted on-chip loss it has been set to <13 dB, which is the same level of a commercial TPA [3]. However for a final version of this type of switches a hybrid integration of InP based gain blocks should be considered in order to compensate for both the on-chip loss and the coupling loss avoiding the use external erbium doped fiber amplifiers at the TPA line ports.

Concerning the signal pass-band the requirement was based on the support of both direct detection transmission at 10 and 25 Gb/s and coherent QPSK transmission at 100 Gb/s.

In Table I the main design specifications are presented and they have been taken as input by the optical circuit designers.

TABLE I

Property	Value	Unit
System Wavelength range	1542–1562	nm
WDM channel spacing	200	GHz
Interleaver Insertion Loss	< 1.5	dB
Inter-leaver 1-dB Pass-band width	> 120	GHz
Interleaver Channel Isolation at 200 GHz	> 20	dB
Mux 1-dB Pass-band width	> 100	GHz
Mux channel isolation at 200 GHz offset	> 10	dB
Mux adjacent channel isolation at 400 GHz offset	> 20	dB
Mux channel isolation at 600 GHz offset	> 25	dB
Mux channel isolation at 800 GHz offset and higher	> 30	dB
Mux insertion loss	< 3	dB
MRR free spectral range	> 2.4	THz
MRR 1-dB Pass-band width	> 50	GHz
MRR channel isolation at 200 GHz offset	> 20	dB
MRR channel isolation at 400 GHz offset	> 25	dB
MRR channel isolation at 600 GHz offset	> 30	dB
MRR channel isolation at 1000 GHz offset	> 35	dB
MRR insertion loss in OFF	< 0.1	dB
MRR insertion loss in ON	< 1	dB
MRR minimum tuning range	8	nm
Waveguide crossing loss	< 0.03	dB
Waveguide crossing Isolation	> 45	dB

V. Circuit Design

The proposed integrated TPA consists of two CMOS chips, one including all the photonic integrated circuit (PIC) and the other with the electronic integrated circuit (EIC) for the device control. These two circuits will be in contact to each other through hundreds of micro-pillar based interconnections, therefore different aspects must be considered in the device functioning including electrical, electromagnetic and thermal effects which could influence the system behavior.

A. PIC Design

The PIC requires many different photonic building blocks with specific requirements. In this section, an overview of them will be given, showing also experimental results when available.

1) Waveguides: The waveguide cross section has dimensions 220 × 480 nm^2 to ensure single-mode conditions at 1.55 μm for the transverse-electric polarization. Widening of the waveguides is implemented in straight sections in order to reduce loss and back-scattering.

2) Grating Couplers: A SPGC with a shallow-etch depth of 70 nm and a buried oxide of 2 μm has been implemented. The grating consists of 33 trenches arranged with a period of 625 nm, targeting a transmission spectrum centered at 1550 nm with a fiber angle of 8° using index matching liquid. The nominal filling factor of 50% was chosen to provide the optimum modal overlap between the exponentially decreasing optical field at the grating output and the Gaussian mode of a SMF28 optical fiber [9]. The grating uses elliptical grating trenches and a short, 22 μm lateral taper between the single mode waveguide and a grating region whose geometry is optimized to provide efficient coupling in the lateral direction to the single mode fiber [10]. The total fiber-to-fiber loss peak at 1548 nm is 6.4 dB (see Fig. 6), which means 3.2 dB loss per grating. This value agrees with finite different time domain simulations. The measured 1 dB-bandwidth is 33 nm.

3) Crossings: As the device has hundreds of interconnected elements, it is important to have very low loss at each crossing. The crossings have been designed as linearly tapered 1 × 1

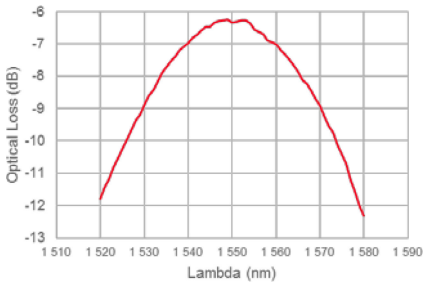

Fig. 6. Fiber-to-fiber optical transmission loss through two grating couplers.

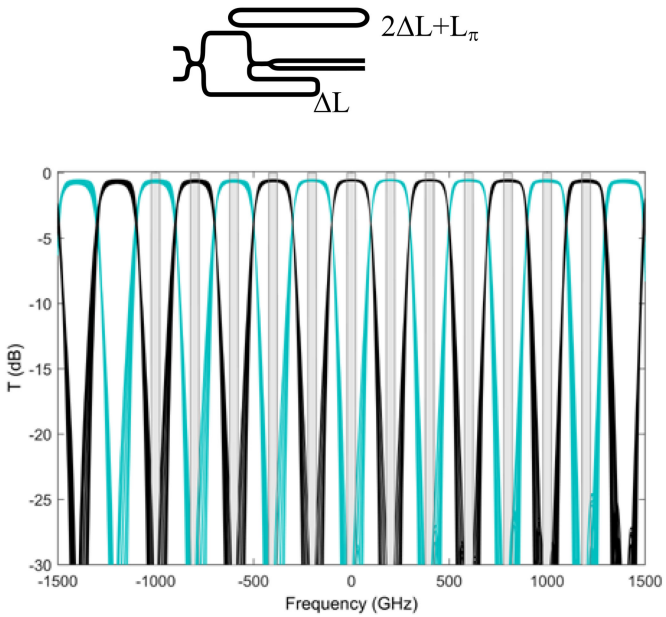

Fig. 7. Schematic of the interleaver design and simulated yield analysis with fabrication deviations (considering both heaters in optimum conditions for each case). Bar and cross spectra are shown in black and blue respectively. Channel positions are indicated with gray rectangles, channel spacing is 200 GHz and central frequency is set to 193.1 THz (1552 nm).

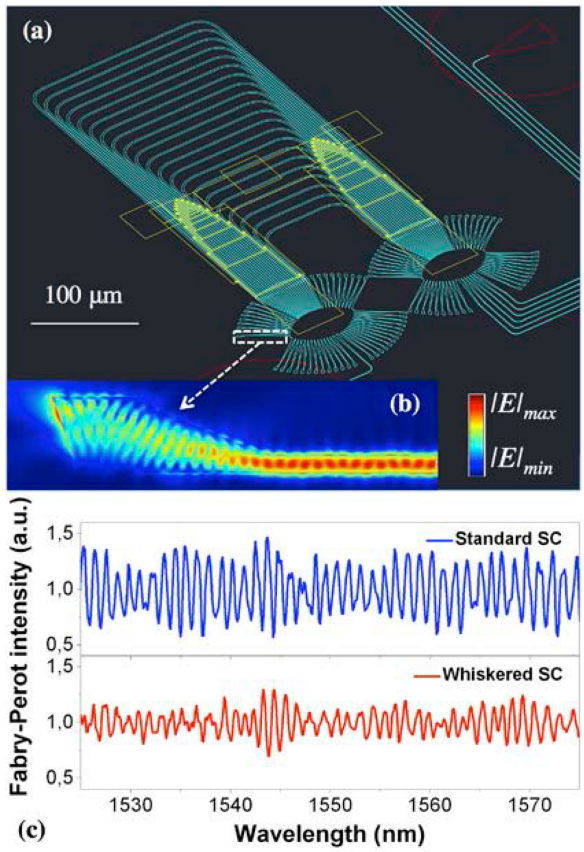

Fig. 8. (a) AWG layout realized for the IRIS full matrix. Different colors represent different design layers: in cyan the silicon waveguides, in yellow the Ti/TiN heaters, the micro-pillars and the electrical pads, in red the grating couplers. (b) FEM simulation of the electric field profile propagating through a reflection killer. Back-reflections are about 18 dB. (c) Fabry-Perot oscillations that rise in a AWG with a standard SC, upper plot, and with a whiskered SC, lower plot.

MMI elements, obtaining simulated loss values <0.04 dB per crossing for the whole band and an isolation above 45 dB.

4) Interleavers: Channel interleavers are needed in order to relax the requirements of the demultiplexer. The design has been based on infinite impulse response (IIR-type) interleavers consisting of a Mach–Zehnder interferometer with a racetrack-resonator in one branch [11]. This type of interleaver, shown in Fig. 7, can be adjusted and tuned using only two heaters. Simulations showed isolation values >20 dB even considering fabrication deviations of ± 10 nm in SOI thickness and in waveguide width.

5) Arrayed Waveguide Gratings (AWGs): After the channels are interleaved, the signals need to be demultiplexed to switch every channel independently [12]–[14]. The AWG has been designed with 400 GHz channel separation for this purpose. The most critical aspect in the AWG design is the control of the phase errors in the grating. In addition, also unwanted reflectance in the star coupler (SC) could affect the AWG performances. Therefore we designed a new SC which reduces the background noise due to whiskers placed at the SOI slab/silica interface to keep down the signal back-scattering. The whiskers consist in a series of tapered waveguides placed perpendicularly to the focal lines and ending in a particular geometry which acts as "reflection killer" (see Fig. 8(a)-(b)). This allows reducing the Fabry–Perot interference that arises within the SC [15], [16]. The analysis of the output signal shows a reduction in the SC reflectance of more than one order of magnitude for the whiskered SC with respect to a standard one (see Fig. 8(c)).

The temperature-dependent wavelength shift of the waveguides when a temperature variation is experienced by the AWG has also been studied [17], [18]. Simulations and experimental measurements confirm that the thermal shift is dramatically reduced for a design with a TiO2 cladding, because of its negative thermo-optic coefficient [19]. Finally, a heating circuit that allows the fine-tuning of the AWG channel-output minimizing the power consumption has been also implemented.

6) Optical Monitors: As the system requires adjustments of the heaters, optical monitors are needed in many positions along the circuit. The monitors also need to work in both directions due to the fact that the device has to operate in direct and reverse

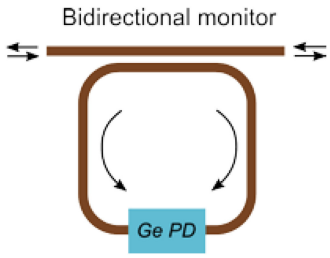

Fig. 9. Bidirectional monitor.

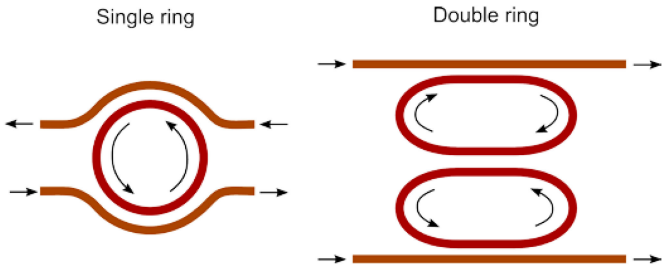

Fig. 10. Single and double micro-ring geometries.

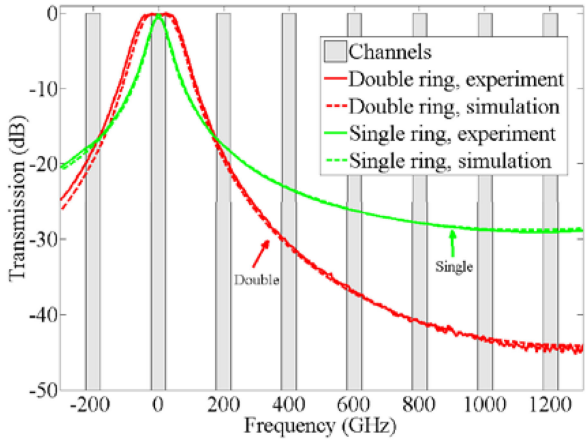

Fig. 11. Transmission response of single (red) and double micro-rings (green). Solid lines represent the experiment, and dashed lines, the simulation. The 200 GHz-spaced channel positions are indicated with grey rectangles. Zero frequency corresponds to approximately 1552 nm.

mode as drop-TPA and add-TPA respectively. Integrated Ge photodiodes have been implemented with dual ports to achieve this functionality (see Fig. 9). These can be designed with any coupling factor (10% or 5% depending on target power) and require an extinction between both photodiode ports higher than 30 dB to avoid any ripples in the output.

7) Micro-Ring-Resonator Switch: This is the most important element of the matrix, as it is responsible for the switching functionality. It also requires very high channel isolation (>35 dB) and low insertion loss. The use MRRs have been proposed for this function due to their compactness and energy efficiency [20]. One could either use a single micro-ring, or a higher-order filter cascading several micro-rings. The main advantage of the single micro-ring, apart from its simplicity, is its lower power consumption, as only one micro-ring needs to be heated for tuning. However, the specified minimum channel isolation (35 dB) requires a high quality factor, hence yields a very narrow channel width, which equals 14 GHz at 1 dB. This is an intrinsic limitation of filters of order 1. On the other hand, filters made with two micro-rings can achieve high isolation without compromising the channel width. Nevertheless, the main disadvantage is the fact that it requires tuning two elements, thus power consumption is approximately double. In addition, an order-two filter requires both optical paths to be identical, which sometimes can be problematic if fabrication deviations introduce asymmetries either in the waveguide or the heater geometry. If that is the case, independent heating of both micro-rings would be necessary.

In order to study all possibilities, single and double micro-rings with different geometries have been designed and fabricated. Two examples of these geometries are shown in Fig. 10. The single-micro-ring shown is a fully-etched circular ring with 5 μm radius, 480 nm width and curved couplers, as with straight couplers it is not possible to reach such high coupling coefficient [21]. The gap between micro-ring and bus was set to two different values, 175 and 200 nm, and the full angle of the curved coupler was varied between 8° and 32°. It has been selected a specific case with a balanced trade-off between isolation and channel width, which corresponds to a gap of 175 nm and a coupler angle of 8°, and Fig. 11 shows the result together with the simulation, showing a good agreement with a single resonator response with 7% coupling factor.

On the other hand, the double micro-ring shown in Fig. 10 is composed of two fully-etched racetrack resonators with straight couplers and coupling length of 2.2 μm. The tight bends required for maintaining the same free spectral range (FSR) (2.4 THz) have been generated with Bezier curves to reduce loss. Details of these structures will be published elsewhere. Coupling coefficients have been designed to be 20% between bus and micro-ring and 1.23% between micro-rings. These coupling values have been attained with 410 nm waveguide and bus width and gaps of 208 and 386 nm respectively. Experimental result and simulations are shown in Fig. 11, where it is clear that both isolation and channel flatness are greatly improved with respect to the single micro-ring case.

The micro-rings can be tuned by heating them individually. Integrated silicon heaters as well as metal heaters have been designed. Each alternative has its own advantages and disadvantages. Metal heaters require specific fabrication processes, but being located on top, they do not occupy useful circuit area. On the other hand, integrated heaters are compatible with the processes needed for modulators, but they require dedicated area of the circuit. In terms of efficiency, there is no clear winner [22], as the main factors related to efficiency are related to the thermal isolation of the elements themselves.

To design the micro-ring heaters, thermal simulations have been performed using the COMSOL Multiphysics software [23]. Simulations of both metal heaters and integrated heaters have been implemented with different geometries. In particular, in Fig. 12 an example is shown of an integrated heater in which the current is injected through a conductive path close to the

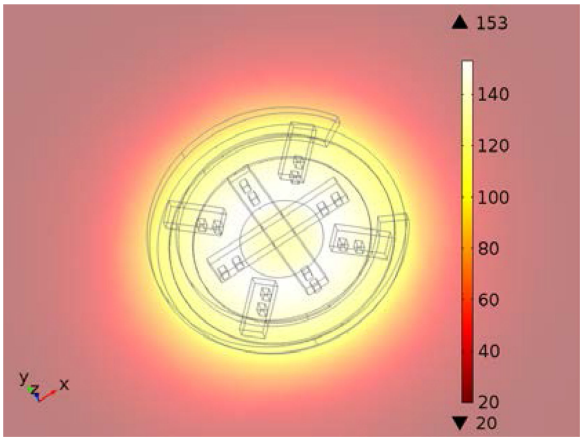

Fig. 12. Simulation of a single micro-ring integrated heater. Temperature variation (°C) for V = 0.9 V.

micro-ring that is obtained by doping a silicon concentric internal micro-ring. For the doping concentration a p+ doping of 1×10^{19} cm^{-3} has been considered which yields a sheet resistance equal to 488 Ω/sq. for a silicon thickness $h = 220$ nm. This particular case corresponds to a heater distance of 1.5 μm and also includes a 60-nm-thick silicon slab to connect the micro-ring and the heater in order to enhance the heat transfer. The maximum supplied voltage is fixed by the electronics used for the control, which is equal to 1.8 V. To keep the heater resistance low, the electrodes are set with an interdigitated shape. The average temperature change in the micro-ring is about 100 °C for an applied voltage of 0.9 V, as shown in Fig. 12. Combining the previous results with the mode analysis [24], [25] a resonance shift of about 8nm is expected for that temperature. The response time of these heaters is expected to be between 3 and 4 μs.

B. EIC Design

The main task of the EIC is to control the heater power of the more than 800 heating elements integrated in the PIC.

This is necessary (i) to tune the optical elements to compensate for production tolerances and (ii) to control the state of the switching elements. Fig. 13 shows the combination of the EIC and the PIC. Furthermore, the main parts of the EIC, the heater control cells, the parallel addressing interface, and the analog interface are depicted.

In [26] a pulse width modulation (PWM) heater control approach is presented, which is very energy efficient but suffers from thermal ripple. Contrary to this, the thermal ripple in the analog approach presented in this paper can be reduced to negligible values.

Fig. 14 shows the circuit diagram of one heater control cell. It consists of a sample-and-hold (S&H) element, a rail-to-rail operational amplifier with low power consumption of only 36 μW, the driving metal–oxide semiconductor field effect transistor (MOSFET) M, and a voltage divider.

The operational amplifier regulates the voltage at the gate of the MOSFET M to set the voltage V_M across the transistor's drain

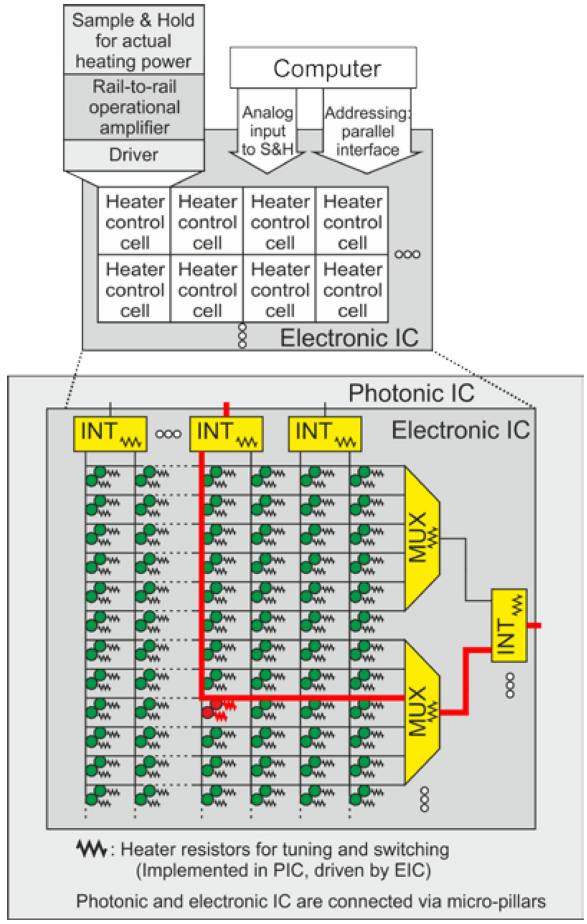

Fig. 13. Control of the heater resistors in the PIC by the EIC.

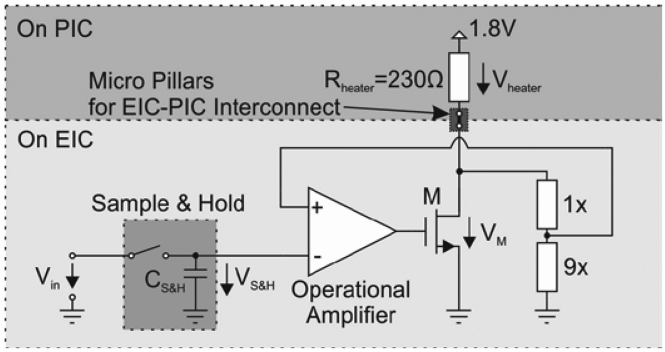

Fig. 14. Block diagram of one heater control circuit

and source to 111.11% of the value stored in the S&H element. This means, by setting the voltage V_{in} at the S&H element, the voltage V_{heater} across the heater element, and therefore its heating power P_{heater} can be controlled. The voltage divider is necessary to be able to fully turn off the heating power even if the operational amplifier has non-negligible input offset voltage.

A test chip with a 4 × 4 heater control matrix including all the interfacing electronics was designed and fabricated in 160 nm BCD8sP to evaluate the heater control circuit. For the design only the CMOS part of this technology was used. Fig. 15

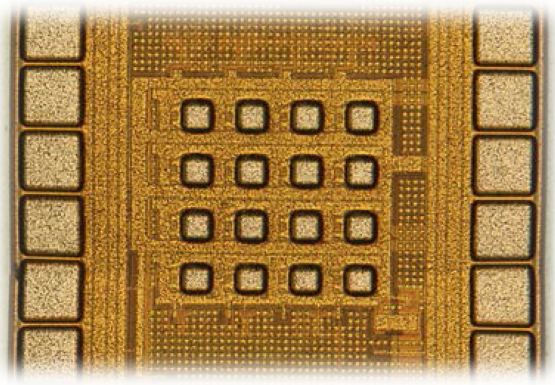

Fig. 15. Chip micrograph of EIC test chip.

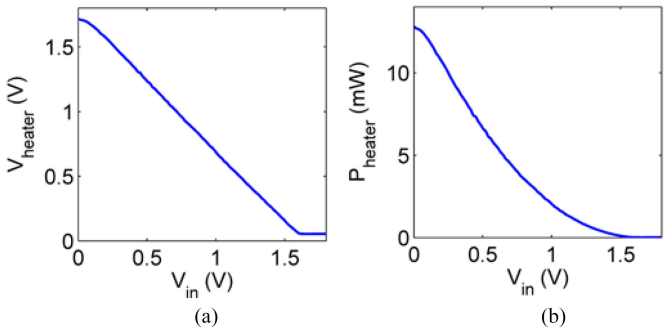

Fig. 16. Heater voltage (a) and heater power (b) depending on the input voltage of the S&H element.

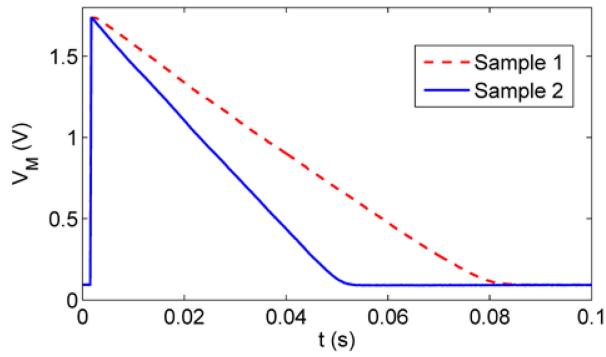

Fig. 17. S&H voltage drop for two different S&H elements over time caused by leakage.

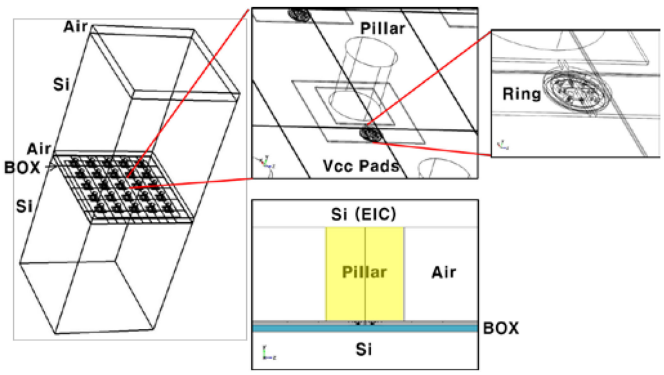

Fig. 18. Layout of thermal simulation including 5 × 5 ring switches connected to EIC for thermal control through Cu pillars.

shows a chip micrograph of the test chip containing the control circuit and the micro-pillar pads for a 4 × 4 heater matrix. Line and column addressing lines have been used to select a specific heater element and to update its heating power by loading its S&H.

Sweeping the input voltage V_{in} of the S&H shows a very linear relationship between V_{in} and the heater voltage V_{heater} applied on the heating element (see Fig. 16(a)). This means there is a quadratic relationship between V_{in} and the heating power P_{heater} (see Fig. 16(b)). The steepest section of this graph defines the necessary resolution for the digital-to-analog converter (DAC) that feeds the S&H element. For example for a resolution of the heating power of 100 μW a DAC with a resolution of 8 bit is necessary.

Every S&H element suffers some leakage. Due to this leakage, the voltage stored inside the S&H element changes, which also changes the actual heating power. In order to keep this effect below critical limits, the S&H elements must be refreshed from time to time. To specify the maximum time between two refresh cycles, the leakage of the S&H elements has been investigated. Fig. 17 shows a relatively linear drop of the S&H voltage over time with a drop rate in the range of ∼ 20 to 35 V/s. This drop rate results in a minimum refresh rate in the range of 4000 refresh cycles per second which is a feasible rate. With this refresh rate and an increase of the sampling capacitance by a factor of 10, the thermal ripple can be about an order of magnitude smaller than with the PWM heater control approach.

VI. Switch Matrix Thermal Simulation

Accurate thermal management of the switching matrix is necessary for the multiple, closely spaced thermo-optic switch elements. The temperature distribution of the multiple switches has been simulated to predict the temperature rise and the amount of thermal cross-talk among the individual switch elements. The simulation layout included interdigitated-contact micro-ring heaters as in Fig. 18. A set of 5 × 5 micro-ring switches have been included for the thermal simulation to see the mutual influence among them. The distance between the neighboring micro-ring heaters was 100 μm in the simulation. The interdigitated heater of the micro-ring switch has been connected to the EIC for resonance control through micro-pillars, and 1.25 V was applied to the micro-pillar to raise the temperature of the micro-ring from the initial temperature enough for an effective switching operation. The temperature of the bottom surface of the silicon substrate was kept at a constant temperature assuming it to be cooled by a thermo-electric cooler (TEC). An additional heat generation is expected in operating the EIC, in addition to the heat generated by the interdigitated heater. The additional heat of 2 mW from EIC was reasonably assumed to flow through the micro-pillar toward the bottom silicon substrate.

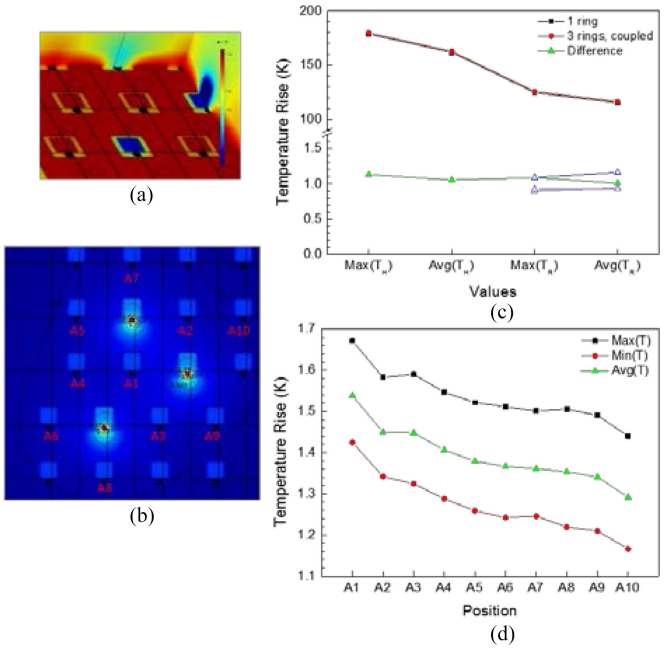

Fig. 19. Results of thermal simulation: (a) voltage distribution, (b) temperature distribution, (c) temperature rise of three heated micro-rings, and (d) temperature rise of neighboring micro-rings.

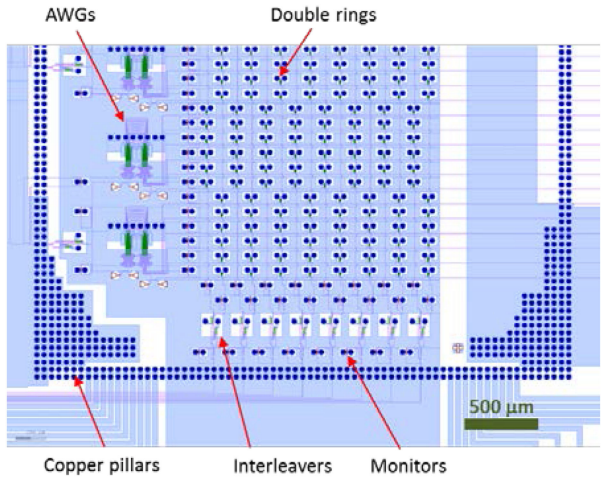

Fig. 20. Mask layout showing the bottom part of the matrix with double-ring switches.

Fig. 19 shows the voltage (a) and temperature distribution (b) by the simulation when three micro-rings are operated by 1.25 V. Fig. 19 also shows the temperature rise for the three heated micro-rings (c) and the other neighboring micro-rings (d). Maximum temperature rise for the heater ($\mathrm{Max}(T_H)$) is about 180 °C, and the average temperature rise for the micro-ring ($\mathrm{Avg}(T_R)$) is about 115 °C. Thermal cross talk to the neighboring micro-rings are less than 1.6 °C and the thermal cross talk between the heated micro-rings are less than 1.2 °C. Considering that the resonance shift is measured to be ∼10 GHz per degree, this means that turning on adjacent rings can detune a ring in the off state by up to 16 GHz and a ring in the on state by up to 12 GHz. For a ring in the off state, this shift has no impact, as the filter is located much further from resonance.

However, when the ring is in the on state, the impact of 12 GHz shift would depend on the filter shape. The double ring has a very broad channel, almost 80 GHz, therefore in this case the effect will not have an impact on the performance. For the single ring filter, which has a narrow filter shape, this effect may have an impact. However, even for that case, a correction could be applied through the control software in order to compensate for these effects.

VII. PIC Mask Implementation

The total PIC size is 8.4×7.8 mm^2, although a considerable amount of this area is dedicated to the electrical pads and the fiber array. Most of the elements are concentrated in the EIC interconnect area, which is 3.7×5.7 mm^2. A section of the mask layout is shown in Fig. 20. The PIC also has 16 grating couplers for the fiber array, and more than 60 electrical pads for the EIC power supply, thermal sensing and communication.

The generation of the PIC layout was based on the building blocks shown in Section V-A. There is a total of 12 interleavers (with two heaters each), 8 AWGs (with 4 heaters each), and $8 \times 4 \times 12 = 384$ switch elements. Each switch element has either one heater for the single-ring version or two for the double-ring version. This means a total of 824 heaters for the double-ring matrix. Each heater is independently controlled by the EIC through micro-pillars. On the other hand, the circuit has 84 power monitors. The integration level is very high, as the number of optical functions per mm^2 is 200 (including waveguides crossings) in the switch matrix area.

Every micro-ring is designed to be in the off state, i.e., with its resonance shifted a constant amount with respect to the wavelength channel it has to switch. Therefore each row is tuned to a different frequency. This was implemented by varying the perimeter of the micro-rings a small amount with respect to the previous one in order to center them appropriately. In our case, the perimeter variation was approximately 57 nm between consecutive channels.

When many elements are interconnected in series, one must be careful with periodicity-induced effects. This means that combined reflections from different elements may add up coherently, thus yielding a much higher reflection than a simple sum of intensities. For this reason, the exact optical distance between consecutive elements in the matrix has been randomized in order to average out the phase differences and therefore remove coherent effects.

The metal heater version requires a total number of 10 mask layers: two etch levels, the metal heater, the via, the metal layer, the passivation overlay, the micro-pillar, plus the three layers needed by the Ge photodiodes. On the other hand, the integrated heater version needs 11 layers, as the metal heater layer is not needed, but one layer is needed for Si doping (which can be either p+ or n+) and the silicide layer to improve the contact between the via and the doped silicon.

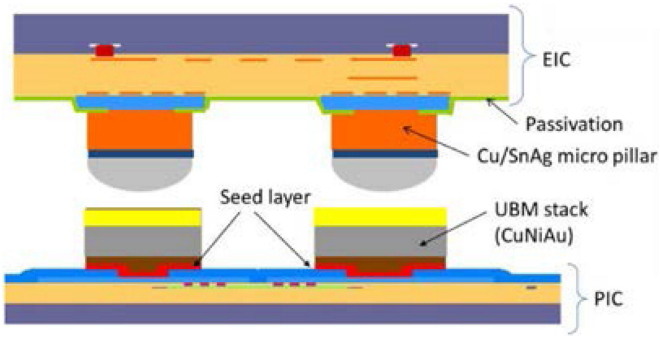

Fig. 21. Cross section of PIC and EIC dies with UBM stack and micro pillars.

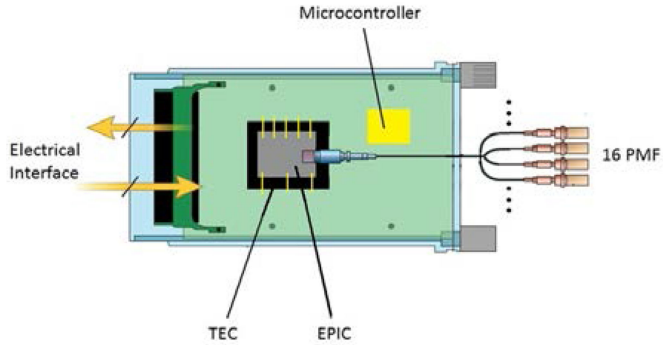

Fig. 22. Artist vision of the package design.

VIII. PIC-EIC Integration and Packaging

The presented device architecture has been designed in order to get a very high integration level on a silicon photonic platform thanks to highly confined optical modes in silicon waveguides. Indeed, the final system on a chip demonstrator will exhibit more than 1000 functions of different types with many electrical connections between the PIC and the driving electronic integrated circuit (EIC). Moreover, the PIC must also be interfaced with more than ten fibers [27]. Lastly, such a high integration level raises also thermal management issues.

The EIC-to-PIC interconnect is made using micro-pillar array. Electronic wafers (comprising the EIC) are post-processed with micro pillars using electroplating semi-additive process of a Ti/Ni/Cu metallic stack through a thick resist mask [28]. An additional layer of eutectic solder (e.g., SnAg) is deposited on the top of the micro pillar. The photonic wafers (comprising the PIC) are processed with an under bump metallization (UBM) pads defined by a Cu/Ni/Au stack. The resulting flip-chip assembly is depicted in Fig. 21. This 3-D hybrid integration technology suits well the targeted integration level with 50 μm pitch interconnection array and less than 1 Ω serial resistance by contact. Moreover, as the silicon photonic technology ensures the system on chip scalability, this integration technology is also scalable in term of interconnection density with a current minimal pitch of 30 μm.

Once the EIC-to-PIC interconnection is made the packaging process goes on with the soldering of all the components into the package, which should guarantee solderability and a good thermal conductivity and heat flow between parts, allowing to dissipate the chip heat power. The scheme of the envisaged package is shown in Fig. 22. The first element to be soldered is the TEC used to dissipate the heat power generated by the chip. To guarantee a good thermal dissipation the TEC's top and bottom AlN ceramic surfaces are gold plated. The employed TEC, which allows to dissipate up to 8.2 W within a temperature span of 25 K, is soldered inside the package with Sn (63%)-Pb(37%) solder bumps melted at 195 °C. Then the chip is glued on the TEC with a thermosetting resin. Both the TEC and the chip are pick-and-placed by means of a die-attach Finetech machine.

Then the following step is the wire bonding of all the TEC and chip's pads to the PCB, which includes a microcontroller for controlling the photonic/electronic chip and readout of the monitor photodiodes, as well as the TEC and all the necessary power electronics. The process used in this specific case is the ball-wedge, where applying heat, pressure and ultrasonic energy, a "ball" is made on one end of the pad and the wedge is realized on the other end of the connection. Gold wire 20 μm thick is used utilizing the wire bonder TPT equipment. Gold has been chosen as the material for making the wire because it provides a flexible and reliable interconnect solution with a low electrical resistivity and an attendant increase in thermal conductivity.

The last step is the fiber arrays' optical vertical alignment and fixing to the chip's waveguides gratings. The fiber arrays comprises 16 polarization maintaining fibers, with a pitch of 127 μm, bending insensitive, and polished with an 8° angle to match with the grating couplers acceptance field and FC/APC connectors at the other end. The pigtailing is achieved by the use of a six-axis alignment bench produced by PI-Micos. The equipment maximizes the optical power by controlling all the axes of freedom. The fibers are stuck to the chip in the position of maximum optical power using an UV epoxy resin.

To complete the device production, the package is protected with a frame and lid encapsulation.

IX. Conclusion

In this paper the design and the achieved results of the integrated reconfigurable silicon photonics optical switch in IRIS Project have been presented. Next stage is the fabrication of the complete PIC and EIC circuits and the device demonstration at system level. The results of this work will prove the feasibility of CMOS photonic system on chip with a very high optical integration scale and the high density interconnect techniques to electronic chip for the device control.

Further breakthroughs are needed for such type of devices to further scale the integration level and to become commercially mature: the management of the polarization and the reduction of crosstalk and losses.

For the first aspect polarization diversity architectures are to be implemented to provide polarization insensitive operations while for the reduction of crosstalk a careful block design could be a viable solution. Finally for the loss issue the use of InP based semiconductor optical amplifier chips hybrid integrated

with the PIC to compensate for the total device losses is the most promising technique to ideally realize lossless devices.

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He is currently the Director of the Technology Development in the R&D of the Networking Products Division of ST Microelectronics, Milan, where he introduced Silicon Photonics from 2004 and today leads several R&D projects in this field and in consumer market. He joined ST with his R&D group in 2000 bringing the Planar Lightwave Circuit (PLC) technology to develop optical matrix switch. From 1980 to 2000, he was the Head of Photonic Unit in the Central R&D of Italtel, where he jointly developed PLC technology with AT&T Bell Labs in early 1990s to realize integrated optical transmission modules. In those years, he was also active in R&D of Optical fiber Communication, he initiated the development of double cladding high power optical amplifier, free-space communication, plastic optical fiber links for medical and automotive applications, and designing many microoptic or discrete, active or passive, optical devices. From 1977 to early 1980s, he was an R&D Designer of semiconductor LED and laser sources operating in first, second, and third window of optical fibers at CSELT, Turin, Italy.

Dr. Chiaretti is a Member of BOG of the IEEE Photonics Society Italy Chapter. He is the author and/or coauthor of more than 40 journals and international conference papers and holds more than 20 granted patents.

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Paolo Pintus (S'10–M'11) was born in Cagliari, Italy, in 1983. He received the Bachelor's degree (with Hons.) and the Master's degree (with Hons.) in electronic engineering from the University of Cagliari, Cagliari, in 2005 and 2007, respectively, and the Ph.D. degree in innovative technologies of ICT and robotics from the Scuola Superiore Sant'Anna, Pisa, Italy, in 2012.

In 2007, he was a Visiting Student (Leonardo da Vinci program) with the Department of Biological Sciences, Imperial College of London, London, U.K. He was a Visiting Researcher during 2010–2011 and a Visiting Assistant Project Scientist in 2015 with the Optoelectronics Research Group of the University of California Santa Barbara, Santa Barbara, CA, USA. He is currently a Research Fellow at Scuola Superiore Sant'Anna, Pisa, and a Member of the National Inter-University Consortium for Telecommunications. His research interests are in the field of integrated optics, silicon photonics, and numerical method for electromagnetism.

Min-Su Kim received the B.S., M.S., and Ph.D. degrees in physics from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 1993, 1995, and 2002, respectively. In KAIST, he carried out theoretical and experimental researches related to various second- and third-order nonlinear optical processes. He joined the Electronics and Telecommunications Research Institute, Daejeon, in 2002, where he has been involved mainly in the research on functional optical devices related with nonlinear optical processes and planar waveguide structures. He is recently involved in thermal analyses of dielectric and silicon photonic waveguide devices.

Daivid Fowler received the Degree (Ist class Hons.) in physics from the University of Hull, Hull, U.K., in 2001, and the Ph.D. degree in nonlinear electron dynamics in novel III–V superlattices from the Semiconductor Quantum Physics Group, University of Nottingham, Nottingham, U.K., in 2005. Since then, he has been a Research Engineer, first investigating III–V-based terahertz sources/detectors at the University of Nottingham before moving on to quantum cascade lasers at the Institut d'Électronique Fondamentale at the Université de Paris 11, Paris, France. In late 2010, he joined the CEA Grenoble, Grenoble, France, as a Research Engineer initially in the field of optics and plasmonics for cooled infrared detectors, and since 2012 in the domain of silicon photonics. He is the author/coauthor of around 30 scientific articles and 4 patents.

José Ángel Ayúcar has been working at the Nanophotonics Technology Centre of Valencia, Valencia, Spain, since September 2004. He started working on the support to From End. He is actually working as Technical of Laboratory, Packaging and Assembly area, in the development of front-end technologies and back-end necessary for integrating photonic components. He has 14 years of experience working on microelectronic, in AT&T and Lucent Technologies, Madrid, Spain, as a Technical Specialist in the analysis failure of chips and packages, in the final product and manufacturing process, improving the yield of the wafers. He is mainly specialized in wire bonder, FineTech, shear, cutting processes, etc.

Michael Hofbauer received the Dipl. Ing. degree from the Vienna University of Technology, Vienna, Austria, in 2011. Since 2005, he has been with the Institute of Electrodynamics, Microwave and Circuit Engineering, Vienna University of Technology, where since 2011, he has been working toward the Ph.D. degree. His research interests include single event effects, semiconductor simulations, 3-D cameras, distance measurement, optoelectronics, and electronic-photonic integration. He is the author and coauthor of more than 30 scientific publications.

Mattia Mancinelli received the B.S. degree in physics from the University of Perugia, Perugia, Italy, in 2008, and the M.S. degree in experimental physics the Ph.D. degree in physics from the University of Trento, Trento, Italy, in 2010 and 2013, respectively.

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Maryse Fournier received the Graduate degree from the Conservatoire National des Arts et Métiers of Grenoble, Grenoble, in 1993. She has been working for ten years at Sofradir Company, Châtenay-Malabry, France, where she was in charge of the flip-chip assembly of infrared focal planes. In 2000, she joined CEA-LETI, Grenoble, to develop processes and electrooptical characterizations of advanced infrared detectors. Since 2010, she has been working in the 200-mm CMOS foundry to develop devices for Silicon Photonics applications. She is currently a Process Integration Engineer at CEA-LETI, Grenoble. She is in charge of the Multi Project Wafer operations within LETI, under FP7-PHOTONFAB and FP7-ESSenTIAL projects for the European ePIXfab platform. She is also involved in various European funded FP projects (FAON, FABULOUS, IRIS) and industrial collaborations. She is the coauthor of more than 30 papers in journals and conference proceedings in its field of expertise.

Giovan Battista Preve was born in Milan, Italy, in 1962. He received the Degree in physics from the University of Milan, Milan, in 1986. He has 20 years of experience working on packaging-related industrial R&D and production in Italy, including two years in Telettra (now Alcatel) on high-RF components, six years in Italtel on optoelectronic components, including a couple of years at AT&T Bell Labs in Murray Hill, NY, USA, during a technology transfer between such companies, three years at Gefran Sensors on MEMS activities, and finally seven years in Pirelli Labs again on optoelectronic components, as a Supervisor of the Back End Laboratories. In June 2008, he joined Valencia Nanophotonics Technology Center, Valencia, Spain, as an Assembly and Packaging Area Manager mainly working on silicon photonic-related applications.

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From May 2014 to December 2014, she was a Visiting Student at Fondazione Bruno Kessler, Trento, where she was involved in collaboration on optical properties of strained silicon for photonic applications. Since 2012, she has been working on radiative recombination and optical gain in tensile-strained Germanium in collaboration with the University of Pisa and on modeling of strain-induced second-order nonlinearities in silicon at Scuola Superiore Sant'Anna.

Ms. Manganelli is the author of several publications on optical properties of strained Germanium and strained silicon for photonics applications and presented her research activity at the IEEE Group IV Photonics Conference in Paris in 2014.

Claudio Castellan received the B.S. and M.S. degrees in physics from the University of Trento, Trento, Italy, in 2013 and 2015, respectively. He is currently working toward the Ph.D. degree in physics at the Nanoscience Laboratory, University of Trento.

His research interest includes the modeling and the experimental test of integrated structures for the wavelength-division multiplexing and nonlinear optics in silicon waveguides.

Gabriel Parès received the Engineer degree in material science from l'Institut National des Sciences Appliquées de Lyon, Lyon, France, and the Postgraduate degree in semiconductor material sciences from the University of Lyon, Lyon. He has been working for 24 years in semiconductors and MEMS industry in industrial and R&D fields, formerly for STMicro and MEMScap, then he joined CEA-LETI, Grenoble, France, in 2004. He is currently a Project Leader at CEA-LETI in the Laboratory of Packaging and Integration, working on 2.5-D/3-D chip stacking, Silicon interposer, TSV integration, as well as rebuilt wafer technologies and advanced packaging solutions. Additionally, he is in charge of the Open3D platform providing access to 3-D technologies for LETI's customers. He is an active Member of the IMAPS Society as the Technical Chair of the IMAPS conference. He holds five patents in 3-D integration fields.

Olivier Lemonnier received the Graduate degree from the Instrumental Engineering Department, Paris XI Institute of Technology, Orsay, France. In 1986, he joined the Aerospatiale Group (now EADS) were he was involved in electronic hardening studies. In 1991, he was recruited by a start-up company designing electrooptic polymers for optical data transmission purposes. In 2003, he joined CEA-LETI, MINATEC Institute, Grenoble, France, where he develops automated test equipments.

Fabrizio Gambini (M'15) was born in Piacenza, Italy, in 1987. He received the B.S. and M.S. degrees in telecommunication engineering from the Politecnico of Milan, Milan, Italy, in 2010 and 2012, respectively, defending the thesis: "Modeling and characterization of first-order optical integrated filters in Indium Phosphide." Since November 2013, he has been working toward the Ph.D. degree at the Scuola Superiore Sant'Anna, Pisa, Italy.

His main research interests include the study, design, fabrication, and characterization of photonic integrated devices silicon-on-insulator and Indium Phosphide technology platforms.

He is also working with CNIT, Pisa, as a Research Assistant within the European Project IRIS (developing a high-capacity and reconfigurable wavelength-division multiplexing photonic switch based on ring resonators).

Pierre Labeye received the Graduate degree from Ecole Supérieure d'Optique (French leading engineering school in optics), Palaiseau, France, in 1987, and the Ph.D. degree from CEA-LETI, Grenoble, France, where he is currently a Senior Researcher. He has been researching in the fields of optical coatings, microoptics, optical sensor devices for various industrial applications, and integrated optics for more than 20 years. He is an expert in the fields of guided optics, micro- and nanotechnologies. He owns 15 patents and more than 75 publications.

Marco Romagnoli received the *Laurea* degree in physics from the Università di Roma "La Sapienza," Roma, Italy, in 1982. He is the Head of Advanced Technologies for Photonic Integration at CNIT, Pisa, Italy, a contract Professor at Scuola Superiore Sant'Anna, Pisa, and the former Director in the R&D Department. In 1983, he started his activity with IBM Research Center, San Jose, CA, USA. In 1984, he joined the Optical Communications Department, Fondazione Ugo Bordoni, working on optical components and transmission systems. In 1998, he joined Pirelli. In Pirelli R&D Photonics, he served as the Director of Design and Characterization and the Chief Scientist. In 2001, he pioneered the activity on Si Photonics and started the development platform for optical components, specifically silica-based PLC's and Si-based nanophotonics.

In October 2010, he joined PhotonIC Corporation, a Si-Photonics company, as the Director of Boston Operations and the Program Manager at the Massachusetts Institute of Technology (MIT) for the development of an optically interconnected multiprocessor Si chip. In this period, he contributed to the demonstration of the first electrically injected Ge laser. He is the author of more than 190 journal papers and conference contributions, and also an Inventor of more than 40 patents. He has more than 35 years of experience in the research field, especially in the area of photonic technologies for TLC.

Dr. Romagnoli is in the Technical Committee of the major conferences in photonics (CLEO/QELS, CLEO Europe, ECOC, MNE, Group IV Photonics), he served as an Expert Evaluator for EC in the 6th Framework Program, and since 2001 till 2006 coordinated a framework program between Pirelli and MIT in which he pioneered the development of Silicon Photonics. He received the "Phillips Morris" Prize for the optical innovation in 1994, and in Pirelli, he got the Title of Chief Scientist.

Lorenzo Pavesi (M'08–SM'11) was born in 1961. He received the Ph.D. degree in physics from the Ecole Polytechnique Federal of Lausanne, Lausanne, Switzerland, in 1990.

He is a full Professor of experimental physics, the Director of the Nanoscience Laboratory, and the Head of the Department of Physics, University of Trento, Trento, Italy. He is the author or coauthor of more than 300 papers, author of several reviews, editor of more than ten books, author of two books, and holds seven patents. His research interest includes silicon-based photonics.

He was the first President and Founder of the IEEE Italian chapter on Nanotechnology. During the last years, he was the Chief Specialty Editor of the section Optics and Photonics of *Frontiers in Materials*, in the editorial board of *Research Letters in Physics*, in the editorial board of the *Journal of Nanoscience and Nanotechnologies*, in the directive council of the LENS (Florence), and in the Board of Delegates of E-MRS. In 2001, he received the title of Cavaliere by the Italian President for scientific merit. In 2010 and 2011, he was elected as a Distinguished Speaker of the IEEE Photonics Society.

Horst Zimmermann (M'98–SM'02) received the Dr.-Ing. degree from the Fraunhofer Institute for Integrated Circuits (IIS-B), Erlangen, Germany, in 1991. Then, he was an Alexander-von-Humboldt Research Fellow with Duke University, Durham, NC, USA, where he worked on diffusion in Si, GaAs, and InP. In 1993, he joined the Chair for Semiconductor Electronics at Kiel University, where he lectured optoelectronics and worked on optoelectronic integration. Since 2000, he has been a full Professor for electronic circuit engineering at the Vienna University of Technology, Vienna, Austria. His main research interests include design and characterization of analog deep-submicrometer nanometer CMOS and optoelectronic integrated (Bi)CMOS circuits as well as electronic-photonic integration. He is the author of the two Springer books entitled *Integrated Silicon Optoelectronics* and *Silicon Optoelectronic Integrated Circuits* as well as the coauthor of *Highly Sensitive Optical Receivers*, *Optical Communication Over Plastic Optical Fibers: Integrated Optical Receiver Technology*, *Analog Filters in Nanometer CMOS*, and *Comparators in Nanometer CMOS Technology*. Furthermore, he is the author and coauthor of more than 450 scientific publications.

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He has filed 20 international patents and he is the author and coauthor of more than than 150 scientific journals and conference papers in the areas of optical amplifiers, optical communications systems, liquid crystal displays, and distributed optical fiber sensors. His current research interests include optical amplifiers, WDM transmission systems and networks, and optical fiber sensors.

Prof. Di Pasquale is on the Board of Reviewers of the IEEE PHOTONICS TECHNOLOGY LETTERS, the IEEE/OSA JOURNAL OF LIGHTWAVE TECHNOLOGY, *Optics Communications*, *Optics Express*, and *Optics Letters*.

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