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Hybrid III-V Silicon Quantum Dot and Quantum Well Lasers

John Bowers

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http://optoelectronics.ece.ucsb.edu/

UCSB: Jared Bauters, Dan Blumenthal, Daoxin Dai, Mike Davenport, Art Gossard, Martijn Heck, Jared Hulme, Alan Liu, Jon Peters, Daryl Spencer, Sudha Srinivasan

SLIDES:Arai, Arakawa, Baets, Fang, Gaeta, Inoe, Kippenberg, Koch, Krishnamoorthy, Liang, Paniccia, Roelkins, Vahala, VanThourhout, Yariv

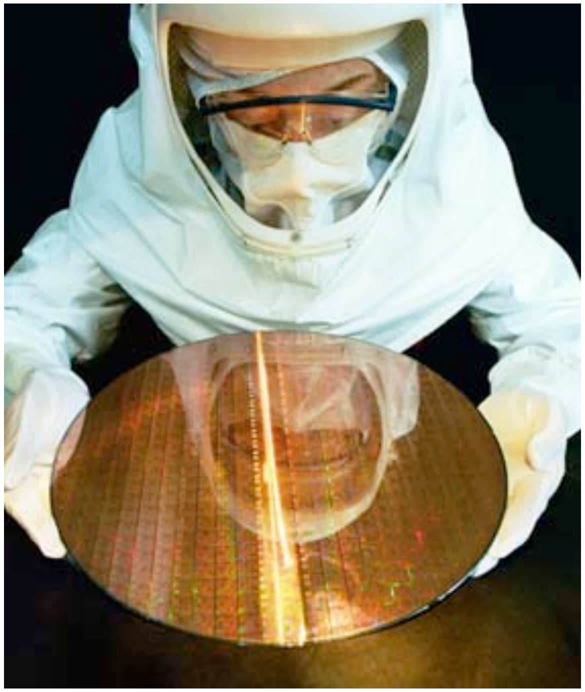
Research supported by Josh Conway and Jag Shah at DARPA MTO, Intel, Google, TE Connectivity, HP, Aurrion

Outline

- Silicon Photonics
- Lasers on Silicon
- Quantum Dot lasers
- Tunable Lasers
- Integration with Electronics
- Commercialization
- Future
- Summary

What is Silicon Photonics?

- Making photonic integrated circuits on Silicon using CMOS process technology in a CMOS fab
- Merging photonics and CMOS



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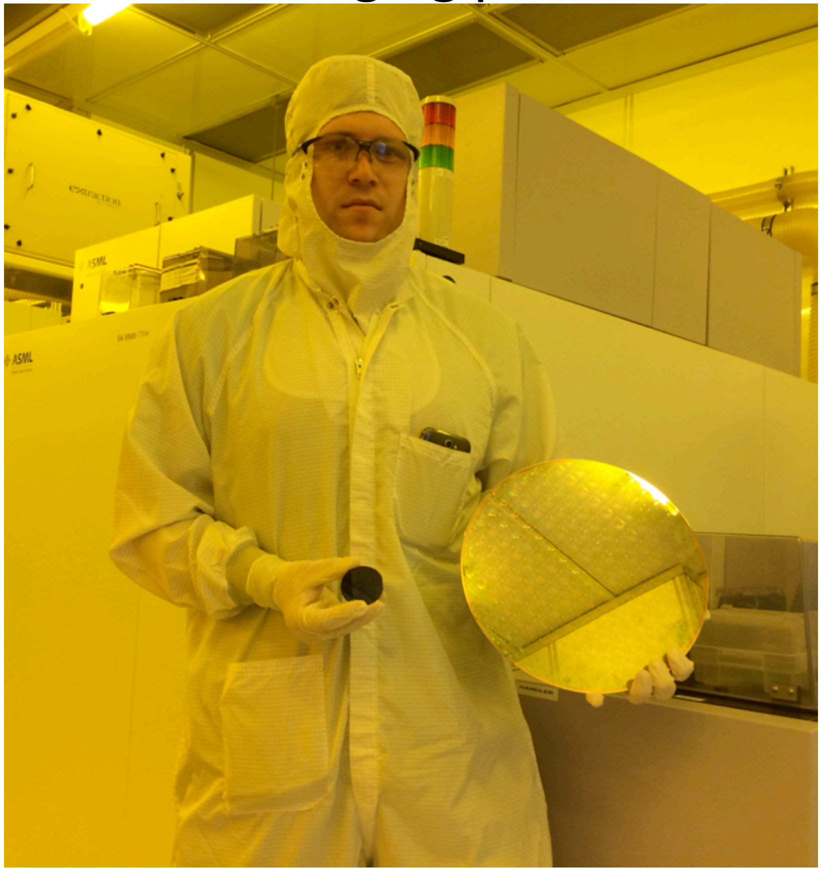
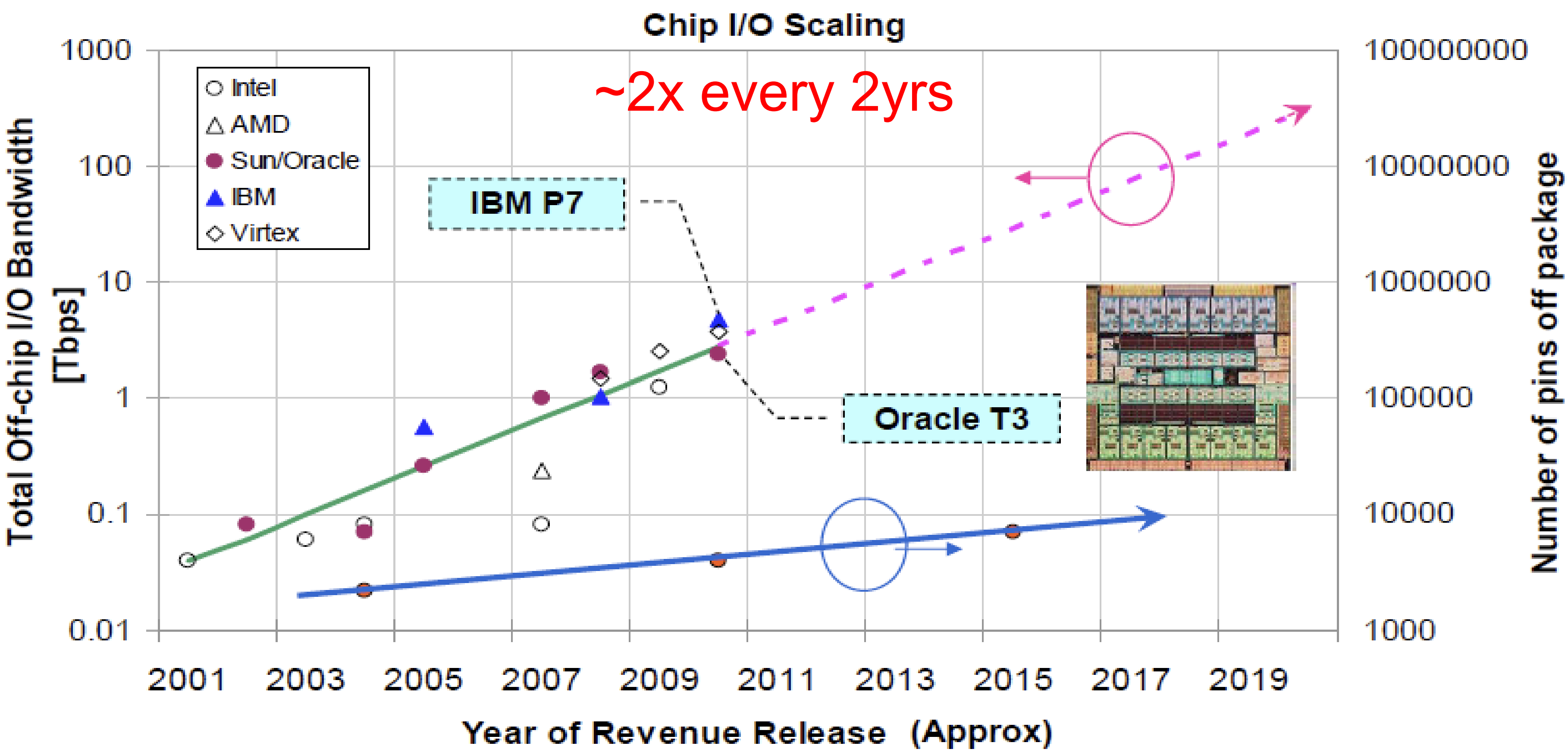


The issue is not InP or GaAs versus Si.
The issue is not VCSELs versus PICs
The issue is
1) Scaling photonics to high levels of integration with improved performance and better process control at low cost.
2) Wafer scale testing
3) Low cost packaging
4) WDM and scaling to >1 Tb/s
5) Solving electrical interconnect limits in Data centers, Supercomputers and ICs with higher capacity, lower cost optical interconnects

Chip I/O bandwidth requirements

- Scale-out of Engineered Systems hinges on off-chip IO
  - Future projections of 100Tbps of Off-Chip BW
  - Pin-growth at a different trajectory – drives (40+ Gbps data rates)



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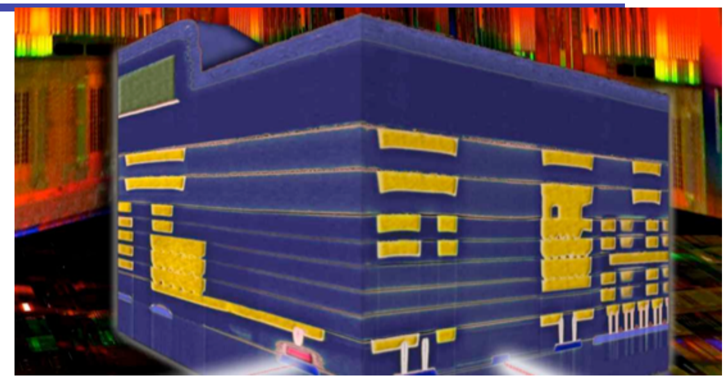
Why Silicon Photonics?

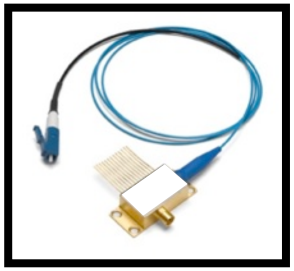


Cross-sectional view of an IBM Silicon Nanophotonics chip combining optical and electrical circuits
Vlasov et al. IEDM postdeadline

- Integrate photonics with electronics
  - Same wafer
  - Bump bonding of silicon PIC with silicon IC
    - Same coefficient of thermal expansion
  - 3D stacking
- Reduce cost by going to larger diameter wafers (300 mm)
  - InP limited by wafer breakage to 100 mm diameter
- Reduce cost by sharing VLSI facility with electronics
- Improve yield by taking advantage of silicon process development
- Volume driver: Solve IC interconnect bottleneck (from 4 Tbps to 1 Pbps). Embedded transmitters/receivers on processors, memories, switches (see Intel/Altera commercialization slide)

Bringing Si Manufacturing to the Laser

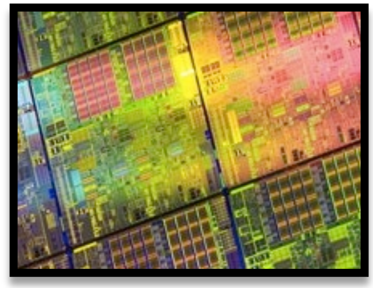
Lasers



- High bandwidth
- Long distances
- Noise Immunity

+

Si Manufacturing



- High volume,
- Low cost
- Highly integrated
- Scalability

InP VCSELs and Photonic Integrated circuits → Six Generations → Silicon Photonic Integrated circuits

Year of Production	1995	1998	2001	2004	2007	2010	2013	2016
DRAM 1/2 Pitch (nm)	270	190	130	90	65	43	32	22
Wafer Size (mm)	150	200	200	200	300	300	300	450

2014: Silicon Photonics Participants

Silicon Photonics Companies	Silicon & Systems Co's	Silicon Photonics Foundries
LIGHTWIRE	CISCO	ST
KOTURA	IBM	IBM
Caliopa silicon photonics	ORACLE	GLOBALFOUNDRIES
aurrion	intel	imec
LUXTERA	Mellanox TECHNOLOGIES	MOSIS
RANOVUS	TeraXion	A*STAR Institute of Microelectronics
	HUAWEI	OpSIS
		PETRA
		cea leti

This is not exhaustive list

Numerous Silicon Photonics Entrants
Across Start-ups, Products, Foundries and Research

Needs

- What is needed is a photonics platform for interconnects and switching that is scalable to
  - Low power
  - High capacity
  - Low cost
  - High volume
  - High yield
  - High reliability
  - Focus here: Wafer scale. (bonding/soldering laser die, not considered)

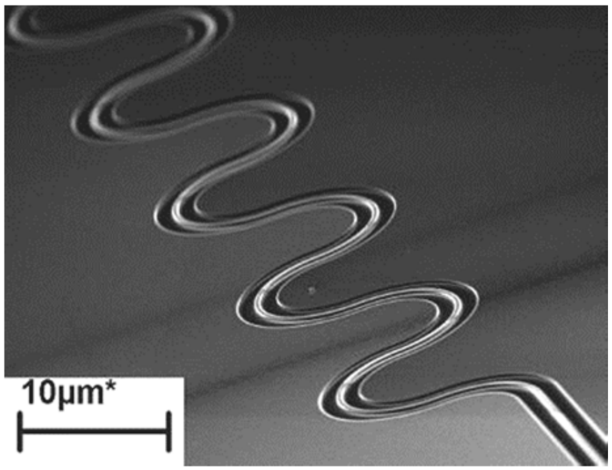
Required Silicon Photonic Components

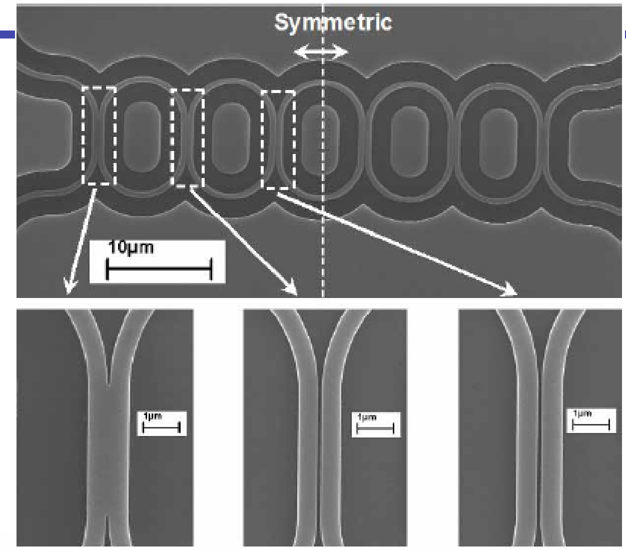
- Passives
  - Low loss waveguides
  - Splitters
  - Wavelength selective combiners/splitters
  - Isolators/Circulators
  - Comb generators
- Actives
  - Lasers (single frequency, tunable, mode locked)
  - Modulators
  - Switches
  - Amplifiers
  - Photodetectors

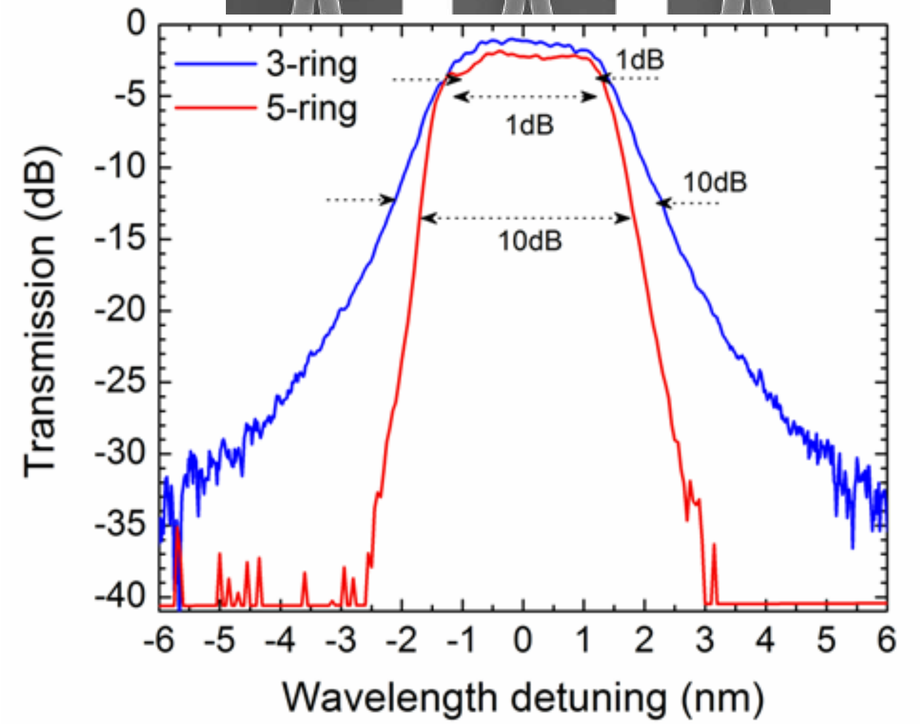
Superior Passive Si Photonic Devices

Si/SiO2 High index contrast:

- **Small wires**
- **Small passive devices**







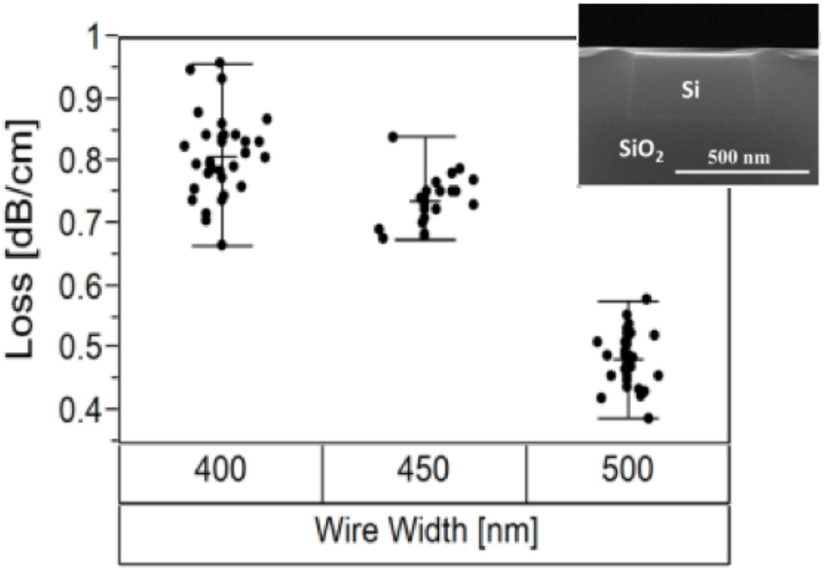
Example of losses for high-index-contrast "wire" waveguides:

- **For 6.5 mm radius bends, losses are 0.0043 dB per 180° turn**

Source: Y. Vlasov, IBM

Move to 193nm immersion lithography, 300mm wafers

Lower loss waveguides

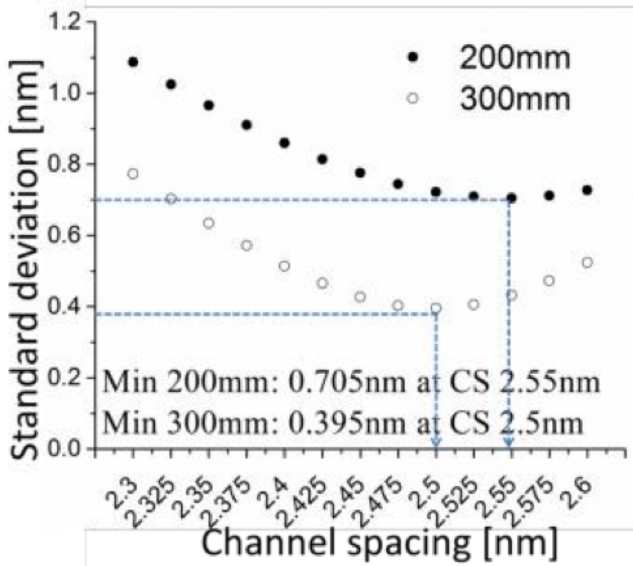


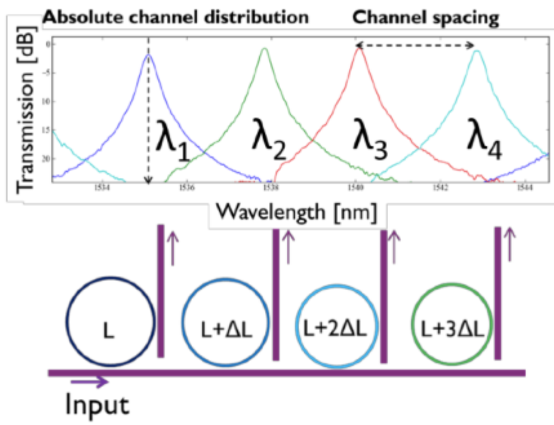
Also:

- < 0.15dB/cm loss in ridge waveguides
- <2dB/cm loss in slot waveguides

S. Selvaraja e.a., OFC '14

More uniform channel spacing in ring demux





P. De Heyn, PhD Thesis UGent, May '14

Silicon Photonic Components

- Passives
  - Low loss waveguides
  - Splitters
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  - Comb generators
- Actives
  - Lasers (single frequency, tunable, mode locked)
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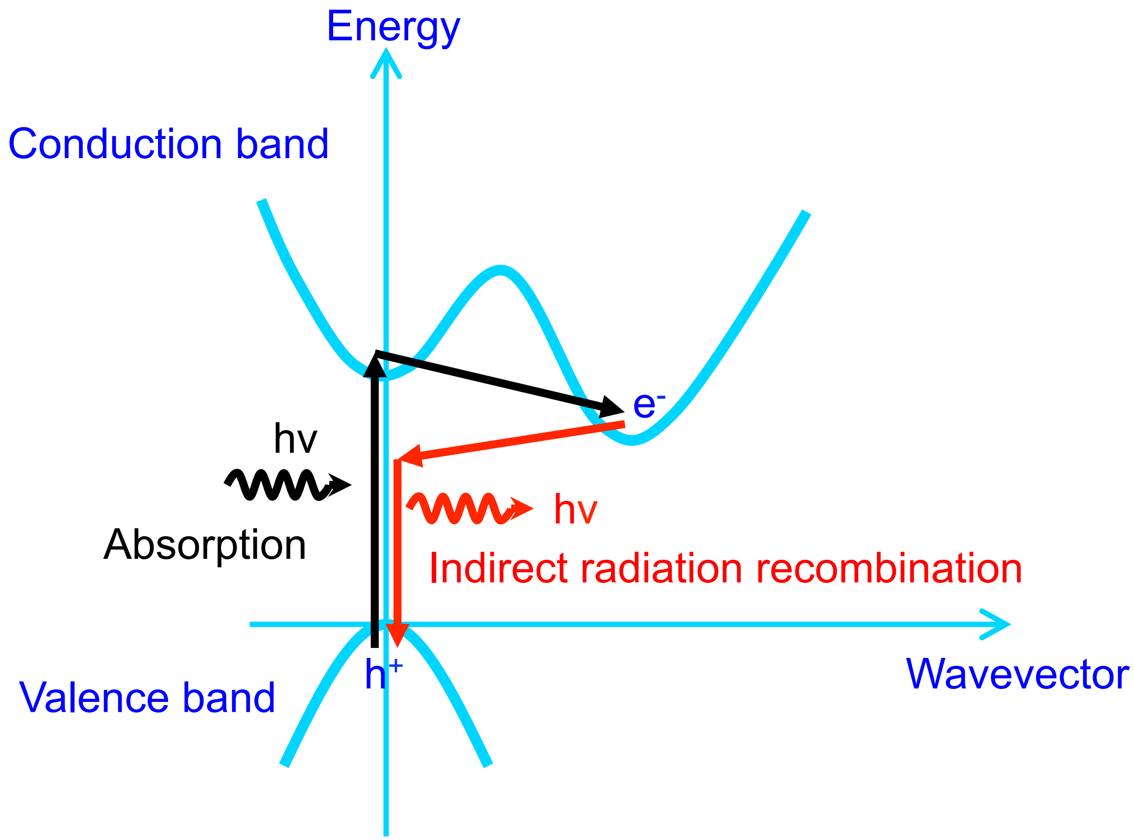
  - Switches
  - Amplifiers
  - Photodetectors

Silicon: Indirect Bandgap

Low internal quantum efficiency in bulk silicon (10^{-6})



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Silicon light emission – How?

- Bulk silicon
- Low dimension Silicon
  - Silicon nanocrystal (Pavesi, …)
  - Periodic nanopatterned crystalline silicon (Jimmy Xu)
- Er dopants (Dal Negro, Watts, Blumenthal…)
- Raman laser (Kyoto, UCLA, Intel)
- Another material for gain (hybrid approach)
  - Epitaxial
    - Ge
    - Quantum Dot
  - Bonding
    - Die level
    - Wafer level (BCB or Molecular)

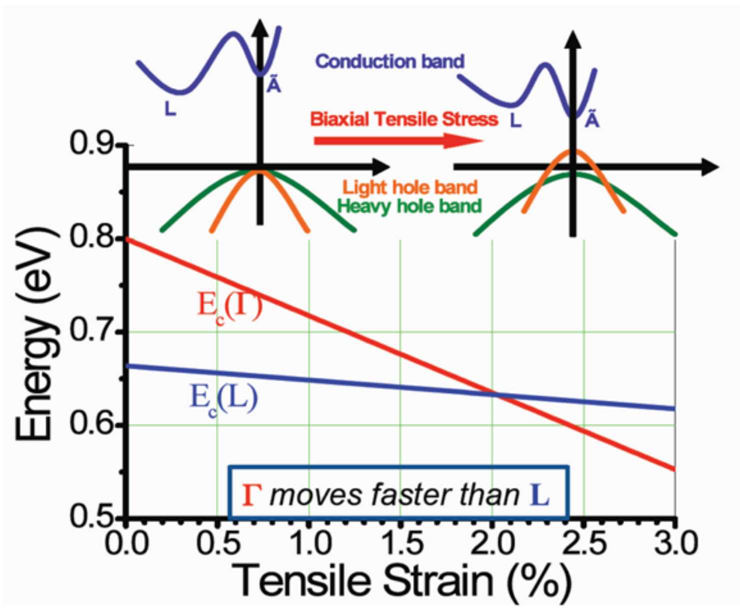
LEDs

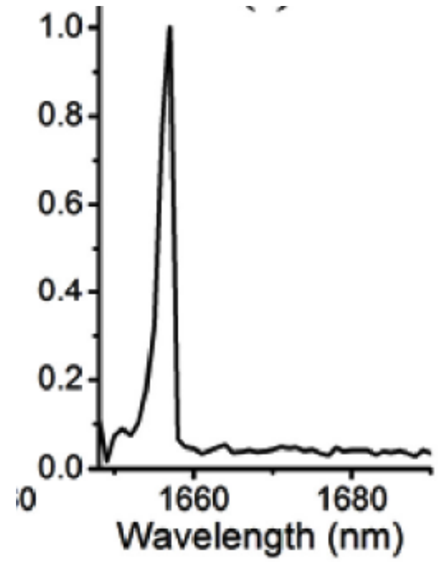
Optically Pumped Lasers

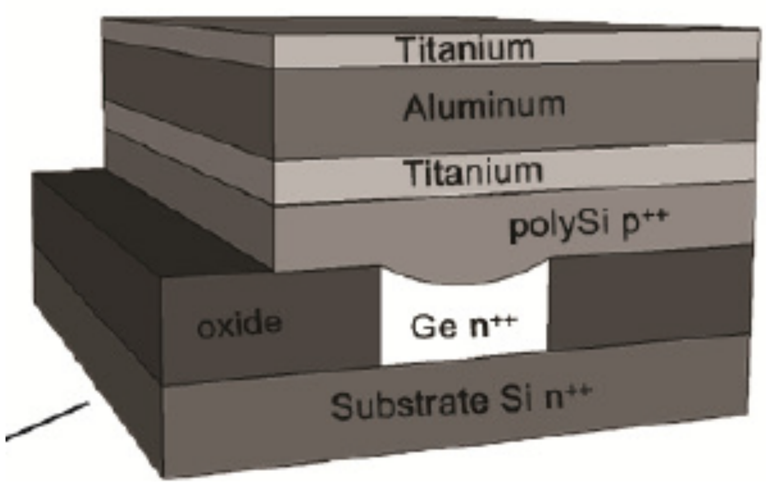
Electrically Pumped Lasers

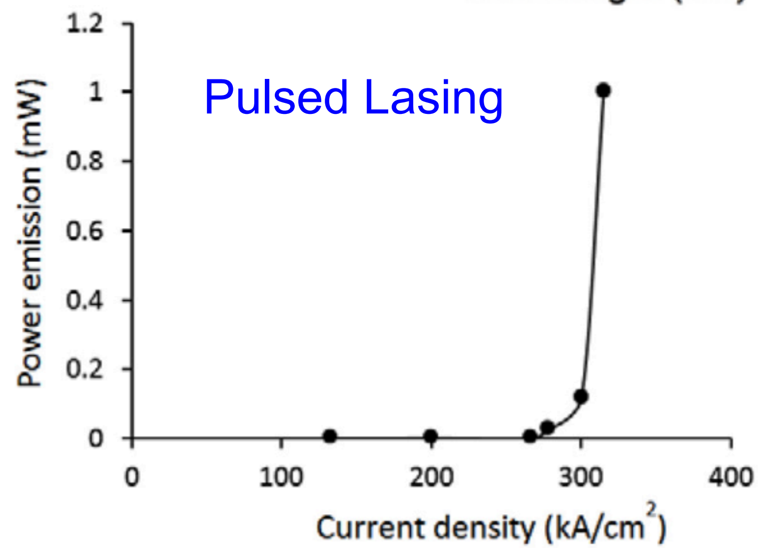
An electrically pumped germanium laser

Rodolfo E. Camacho-Aguilera,[1] Yan Cai,[1] Neil Patel,[1] Jonathan T. Bessette,[1] Marco Romagnoli,[1,2] Lionel C. Kimerling,[1] and Jurgen Michel[1,*]









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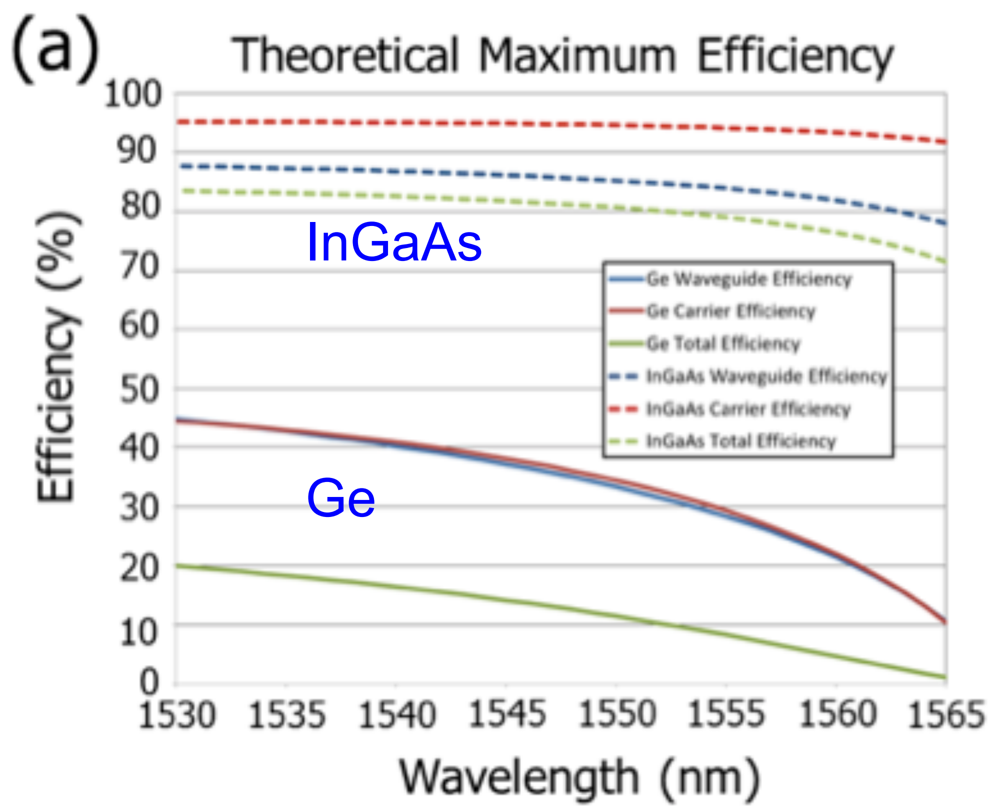
Theoretical efficiency of electrically pumped, strained Ge lasers

David C. Nielsen,[1,*] and J. Scott Rodgers,[2]

[1]Booz Allen Hamilton, 3811 N Fairfax Dr. Arlington, VA 22203, USA
[2]Defense Advanced Research Projects Agency, 675 N. Randolph St., Arlington VA 22203, USA
[*]nielsen_david@bah.com



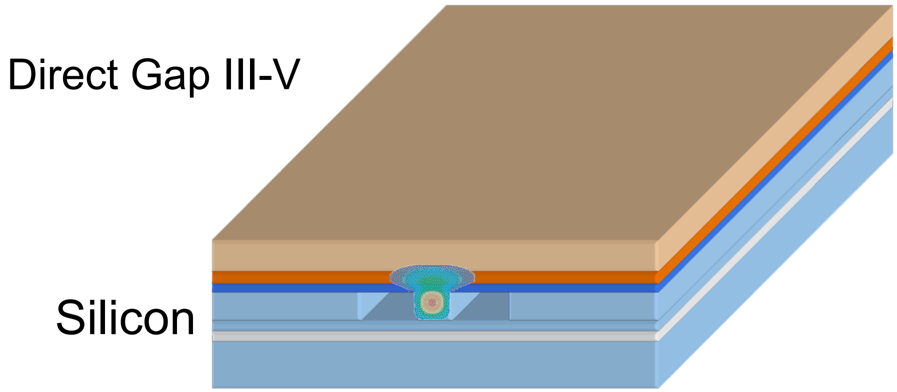
Direct bandgap is essential

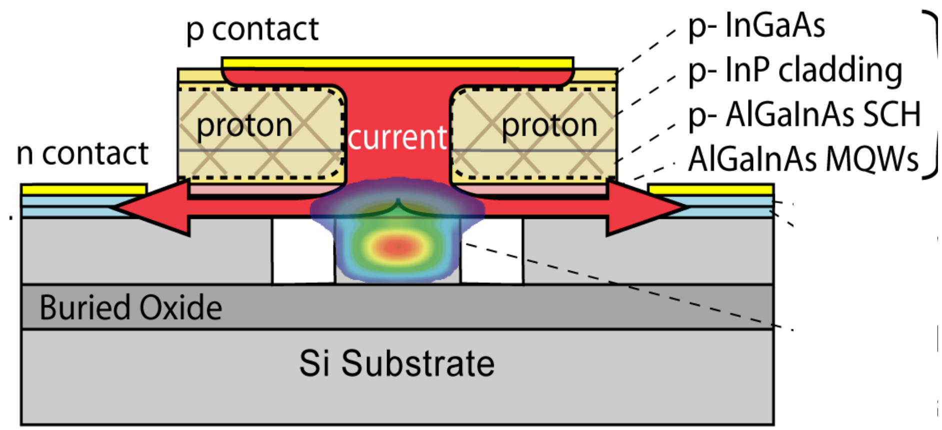
Heterogeneous Integration

Quantum Well (UCSB, Ghent, Caltech, Tokyo Inst. Of Tech, Intel, HP, Aurrion)

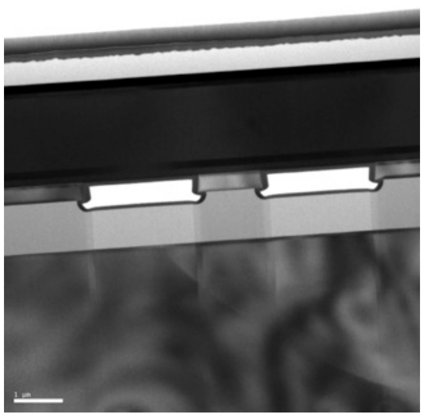
Quantum Dot (Univ. Tokyo, UCSB)

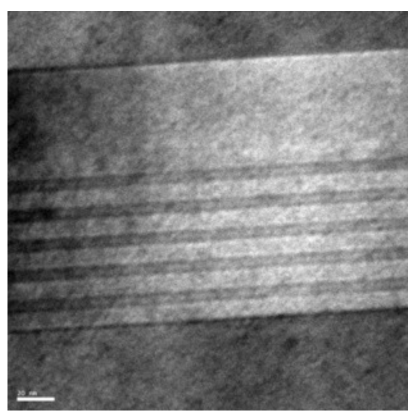
Hybrid Silicon Photonics

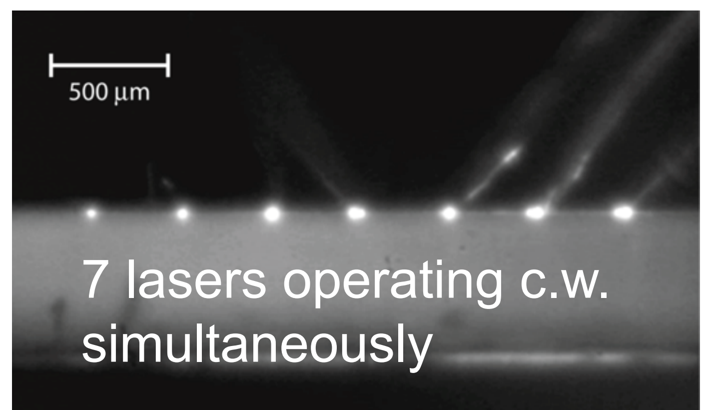




- Optical gain from III-V Material
- Efficient coupling to silicon passive photonic devices
- No bonding **alignment** necessary: suitable for high volume CMOS
- All back end processing low temperature (<350 C)



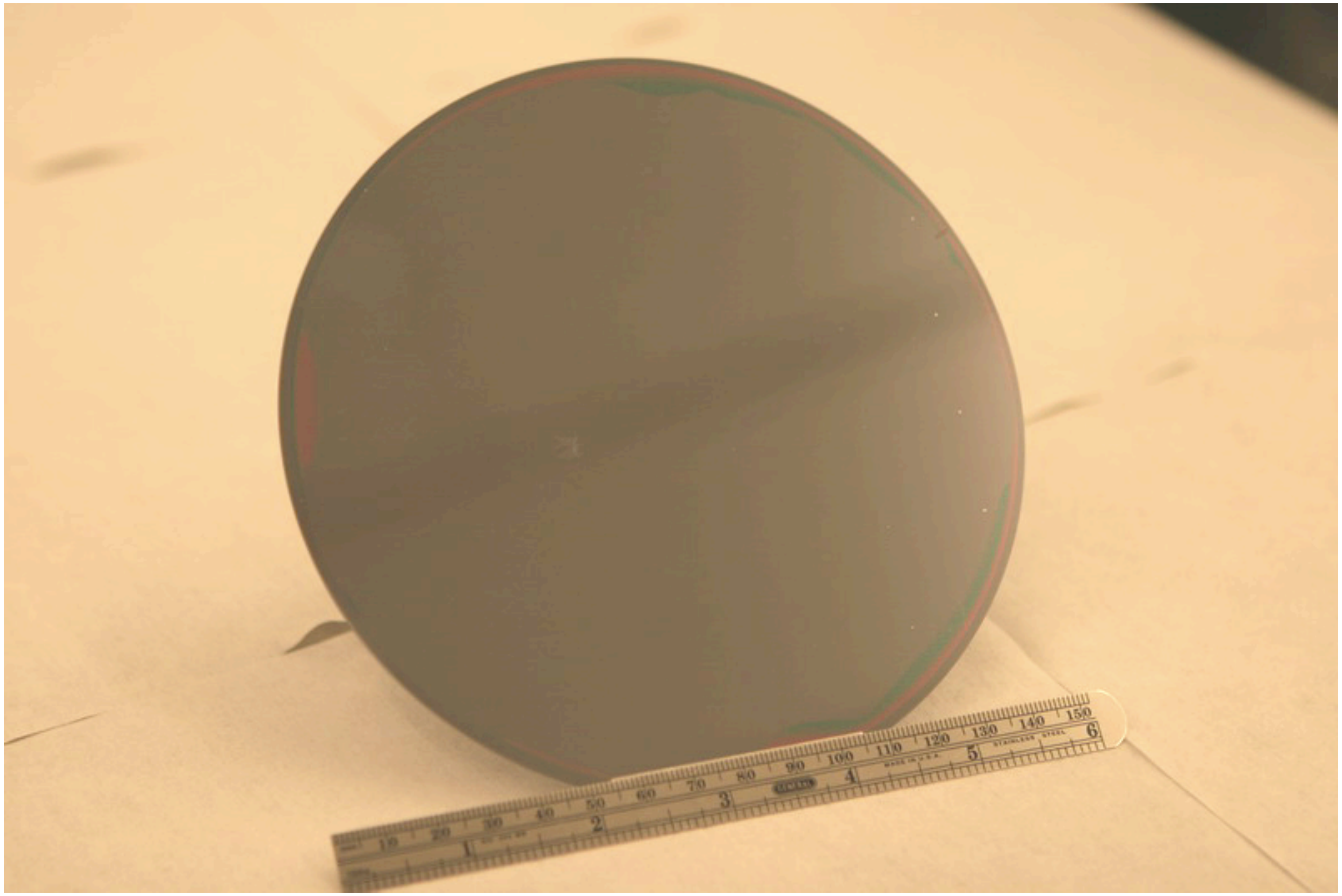




A.W. Fang, et al., “A Continuous Wave Hybrid AlGaInAs-Silicon Evanescent Laser,” IEEE Photonics Technology Letters, 18 (10), 1143-1145, May 15, 2006

Quantum Well Epi on 150 mm Silicon

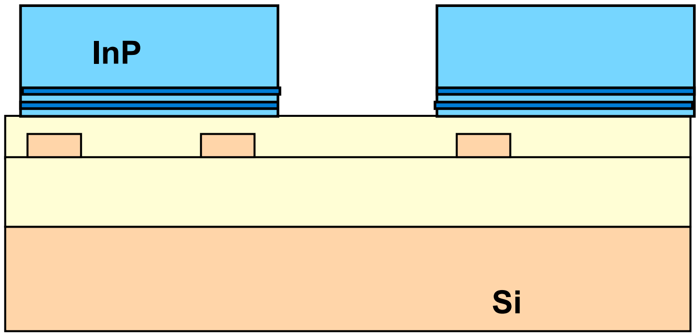
Oxygen Plasma Enhanced Molecular Bonding

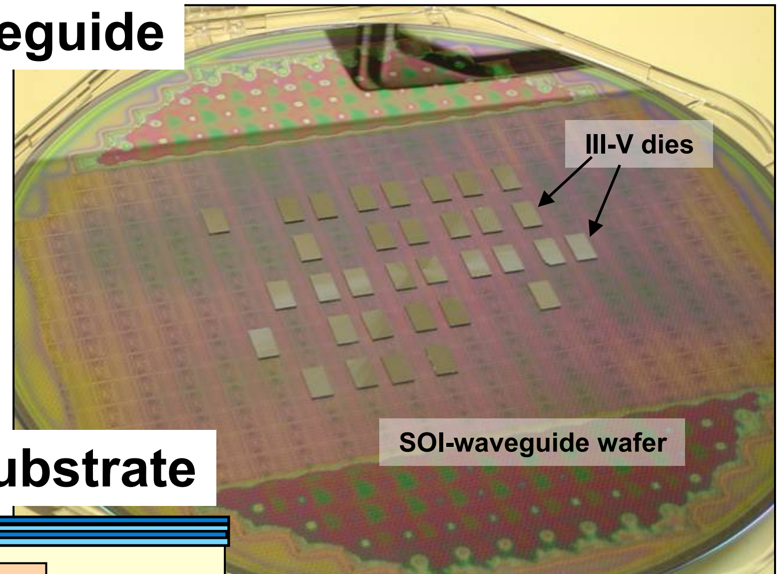


Heterogeneous integration

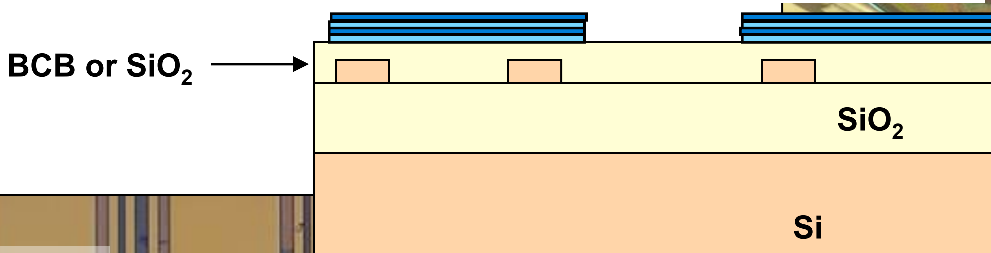
UCSB, Intel, HP, Ghent, IMEC,TIT, Caltech, NTT, Aurrion

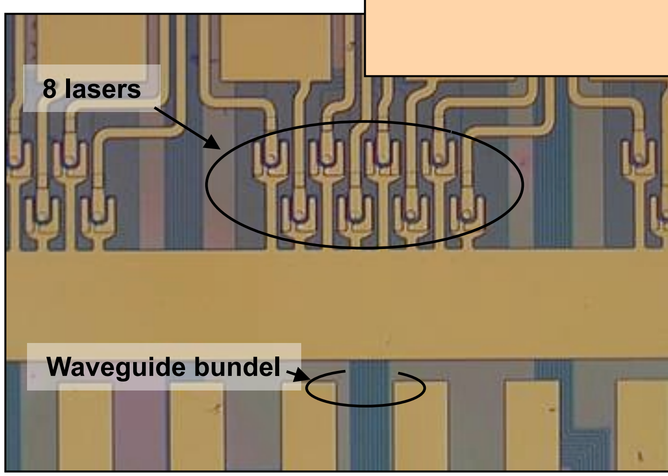
Step 1: Bond InP-dies on SOI waveguide



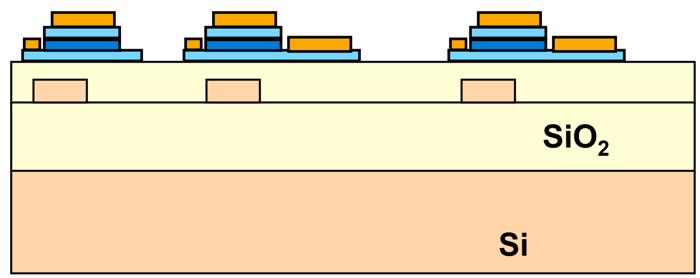


Step 2: Remove substrate





Step 3: Process lasers <u>at wafer scale</u>

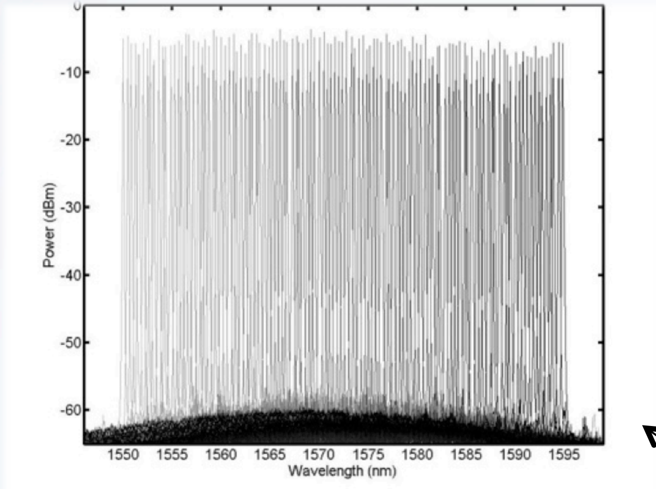


IMEC/Ghent

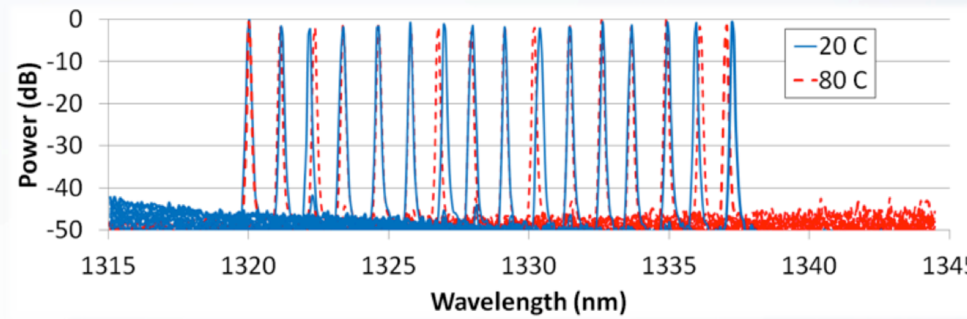
Aurrion PIC Integration

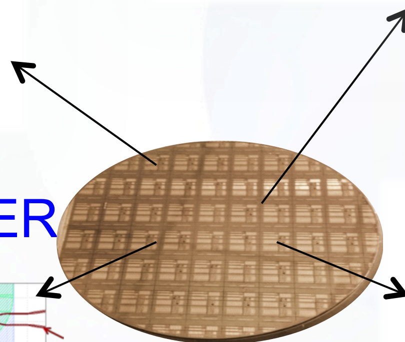
Brian Koch *et al.*, OFC Postdeadline 2013

Telecom Tunable Lasers

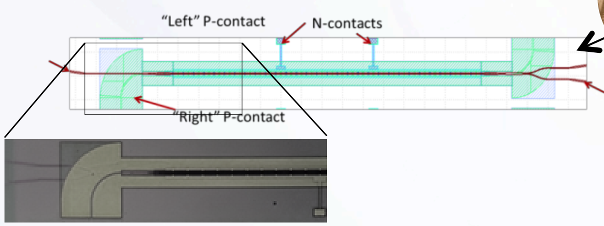


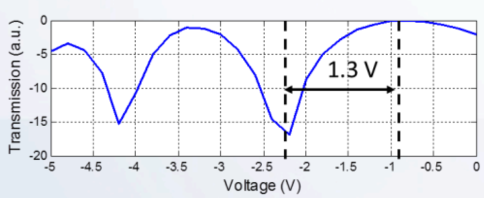
Datacom uncooled WDM laser arrays

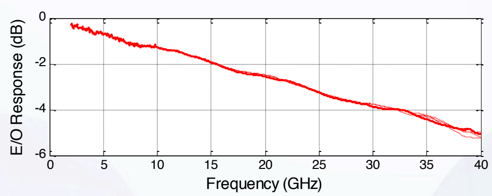


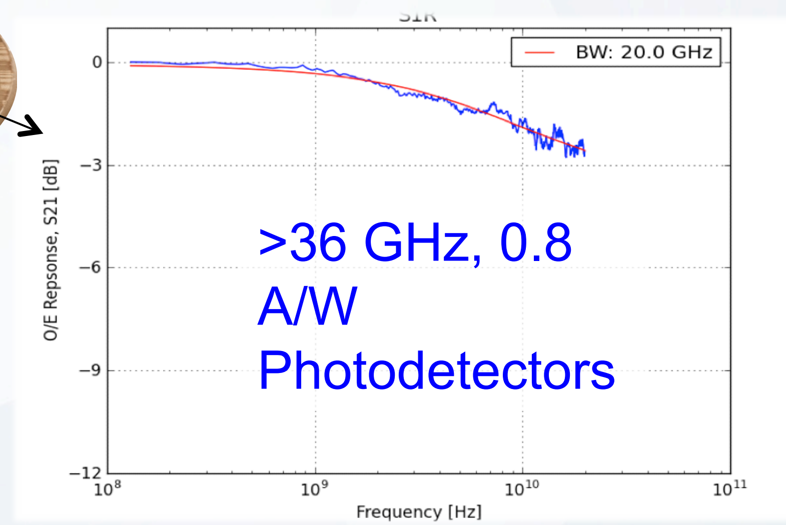


Modulators: 23 GHz, >15 dB ER







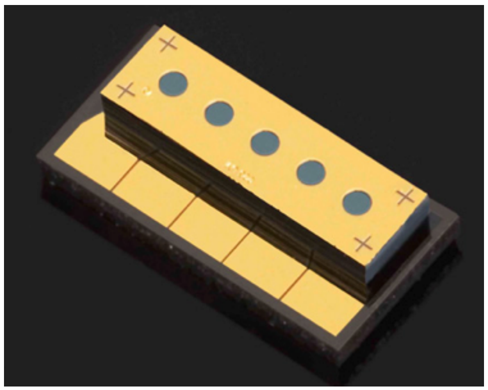


>36 GHz, 0.8 A/W Photodetectors

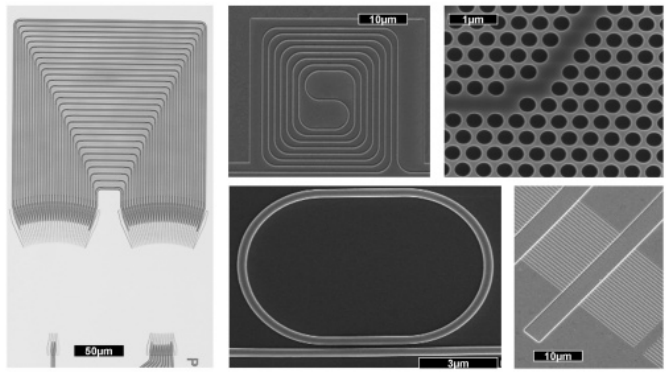
aurrion

Heterogeneous Integration of 6 Photonic Platforms

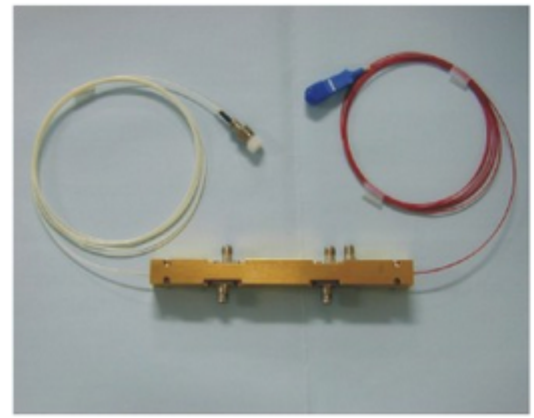
GaAs



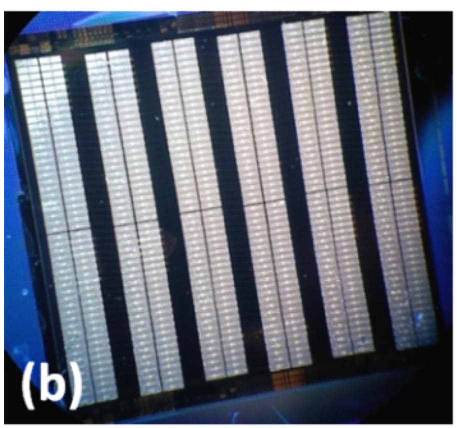
Silicon



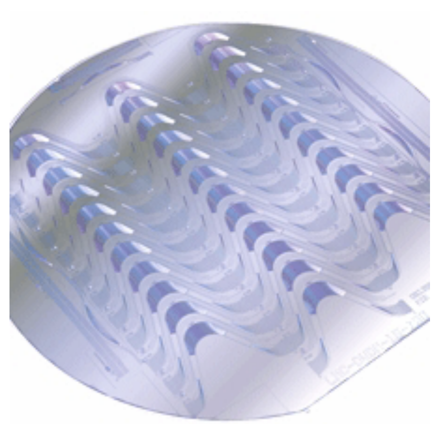
$LiNbO_3$



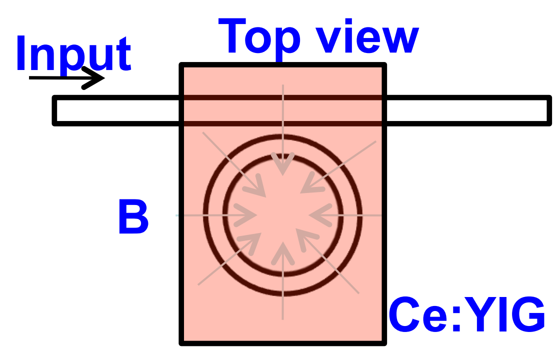
InP



SiN/SiON/SiO2

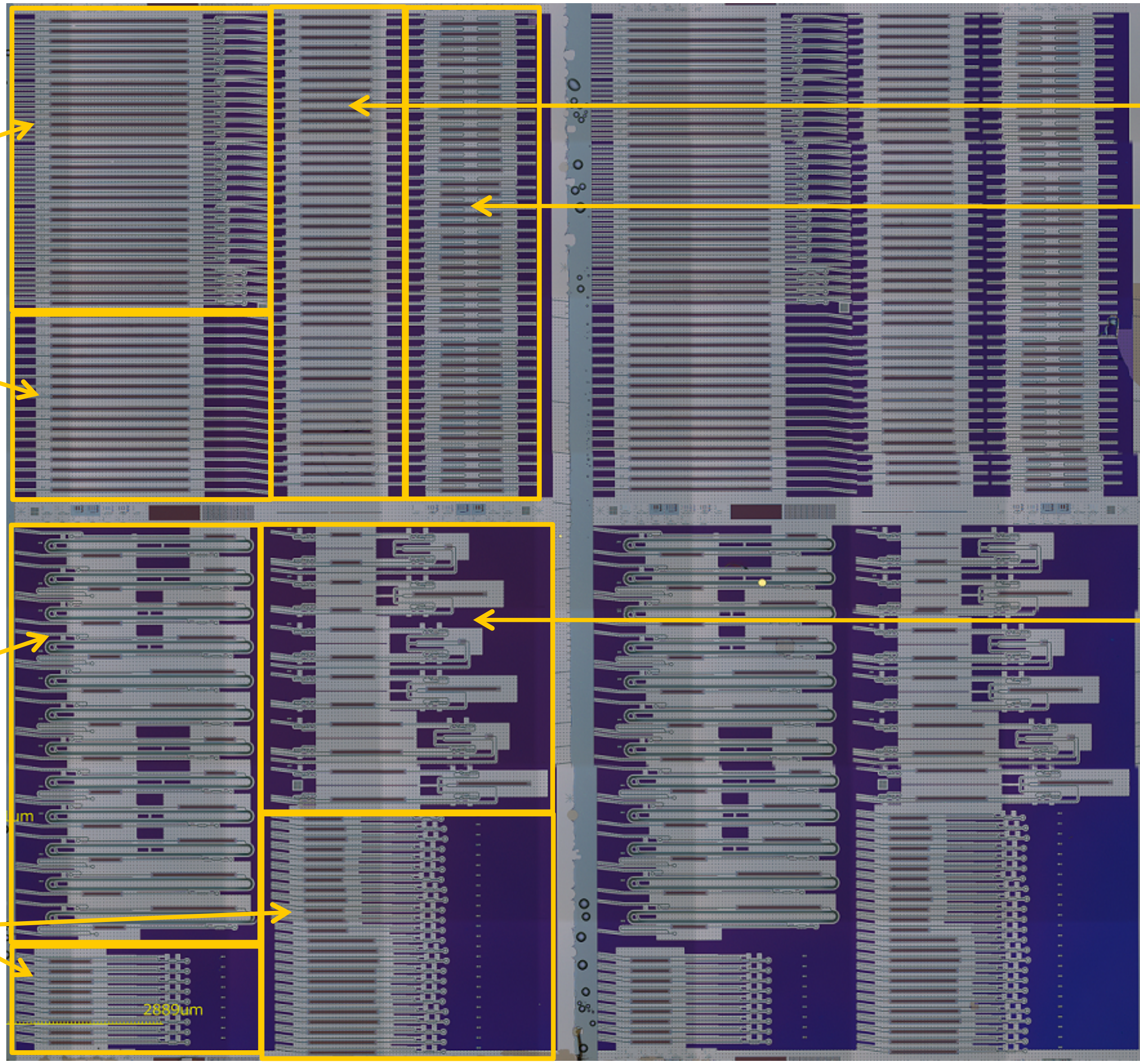


Ce:YIG Isolator



Heck et al. JSTQE 2013

UCSB Shuttle Run



Loop mirror lasers

DBR lasers

Feedback stabilized MLLs

DBR MLLs

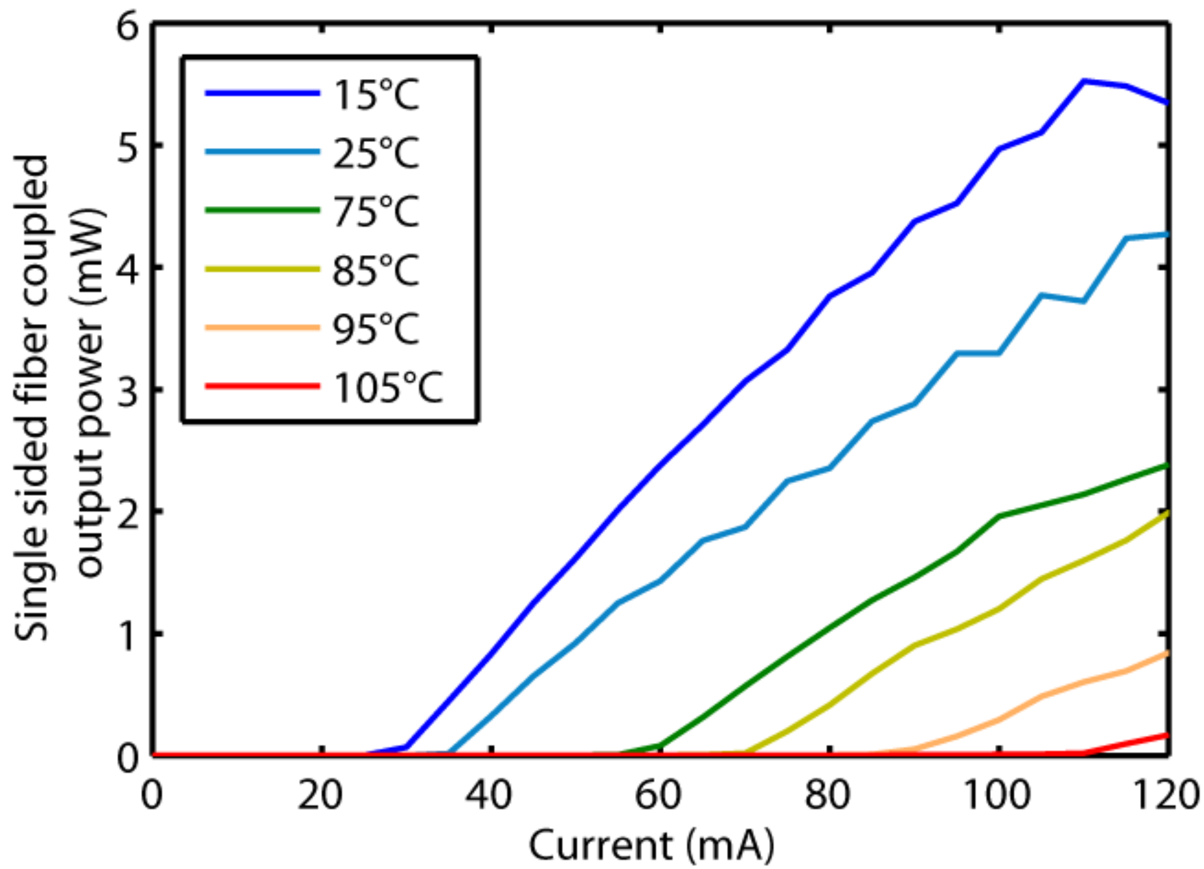
Taper test structures

FP-MLLs

Tunable laser microwave generators

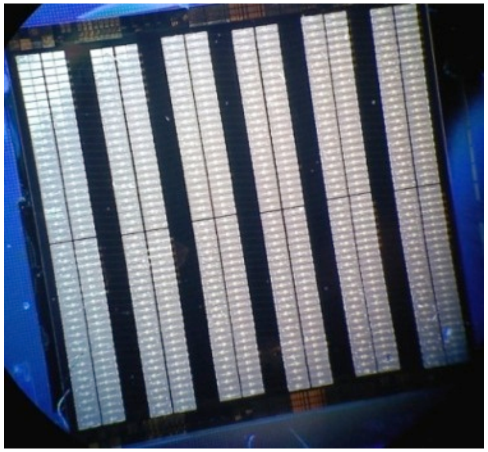
Hybrid Silicon Quantum Well Lasers
105 C CW 1310 nm laser

- Max fiber coupled output power: 5.5 mW/facet
- T_0: 80 °C
- Injection efficiency: 52 %

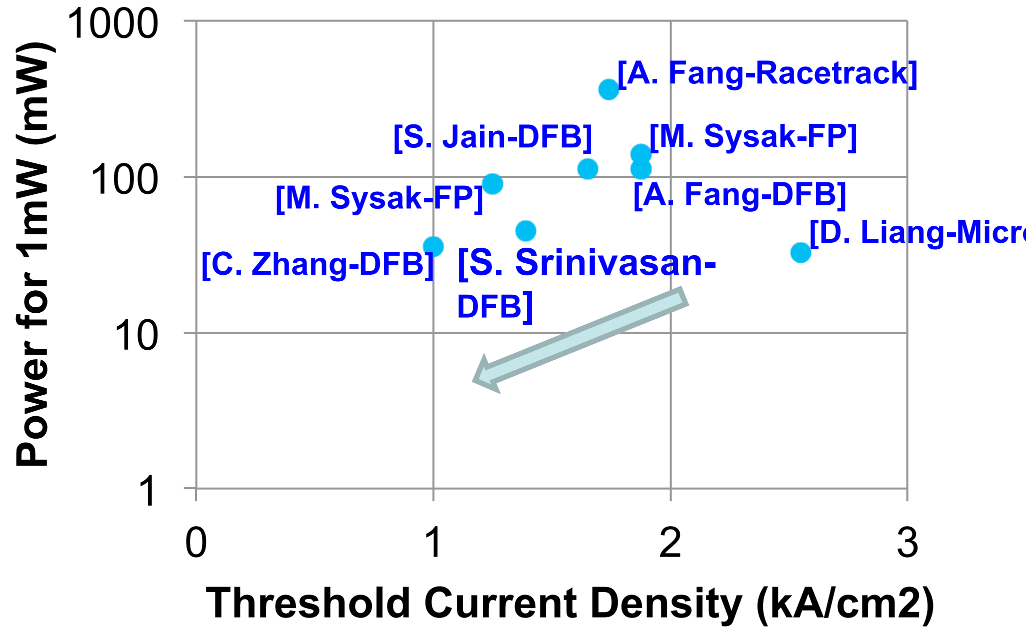


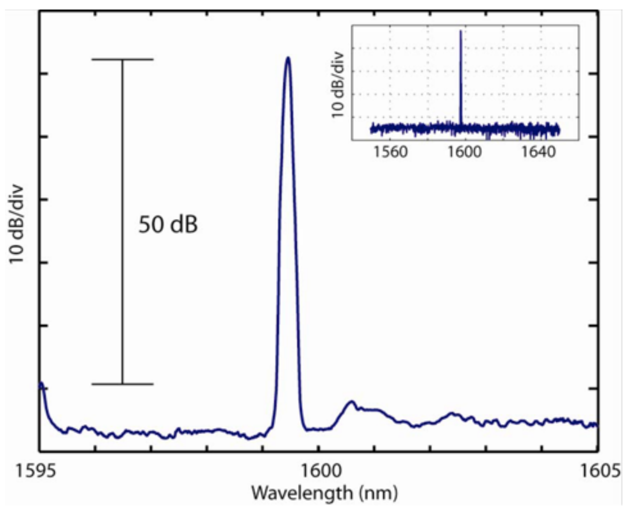
Chang et al., Optics Express 15(18), 11466, August (2007).

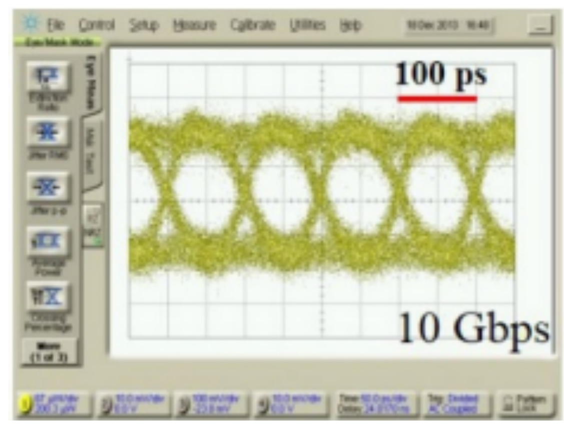
DFB Quantum Well Hybrid Silicon Lasers



Chip showing 300 DFB lasers with yield >95%





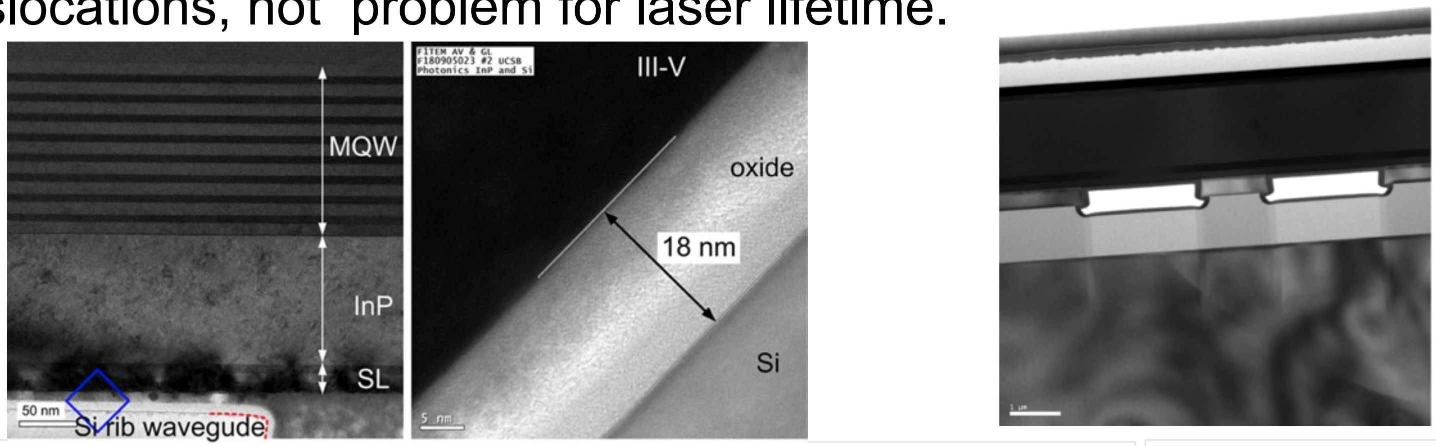


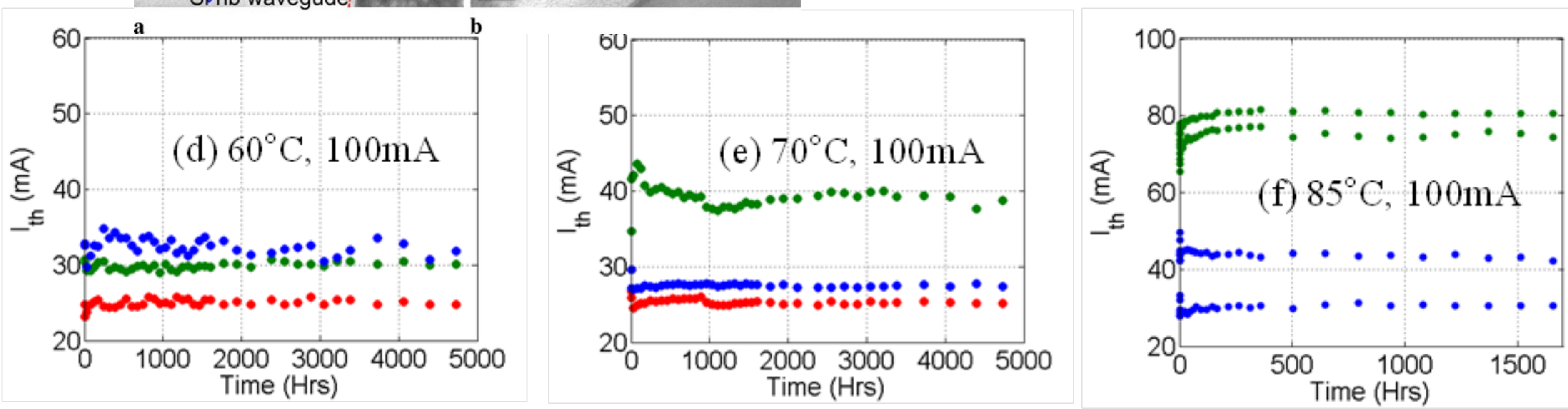
10Gbps direct modulation of a 200μm DFB laser

C. Zhang, et al. "Low threshold and high speed short cavity distributed feedback hybrid silicon lasers", Optics Express 2014

Aging of Bonded Devices: No threading dislocations

- Epitaxial growth on InP or GaAs followed by bonding to Si results in edge dislocations, not problem for laser lifetime.



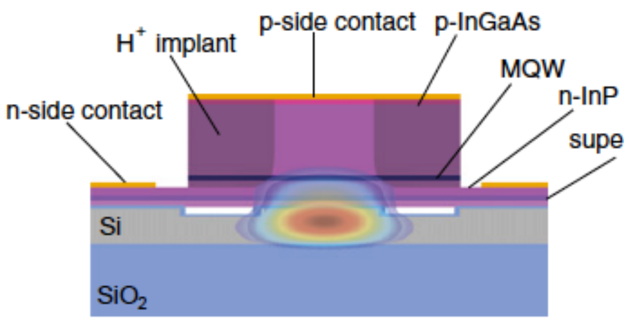


Time to reach 50% degradation in threshold current at 70°C is >40,000hrs

S. Srinivasan and J.E. Bowers . "Reliability of hybrid III-V on Si distributed feedback lasers," JSTQE 2014

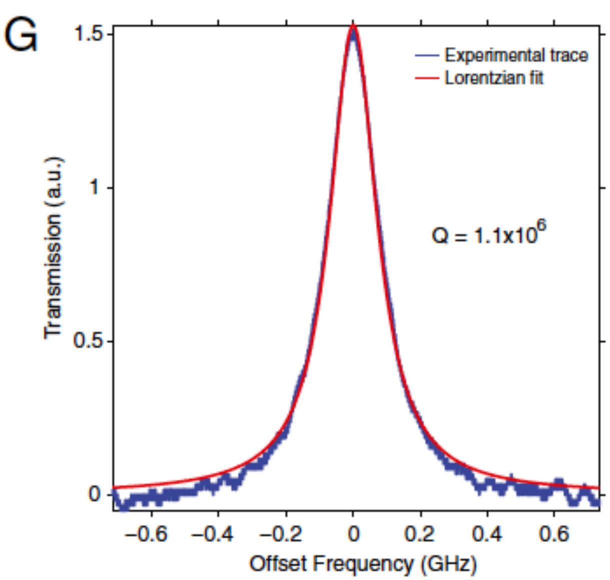
High-coherence semiconductor lasers based on integral high-Q resonators in hybrid Si/III-V platforms

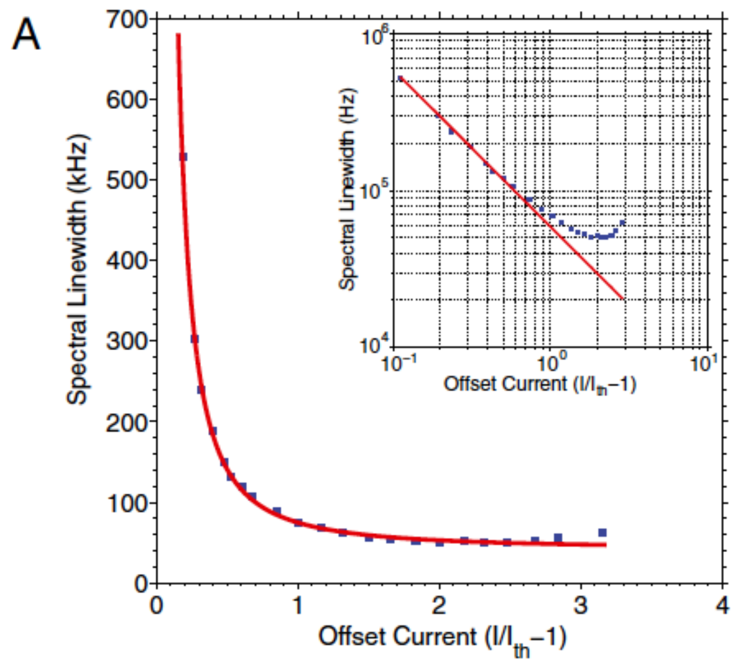
Christos Theodoros Santis[1], Scott T. Steger, Yaakov Vilenchik, Arseny Vasilyev, and Amnon Yariv[1]



$$(\Delta \nu)_{laser} = \frac{2\pi h \nu_o^3 \mu (1+\alpha^2)}{Q^2 P}$$

High Q (1 million)
20 kHz linewidth

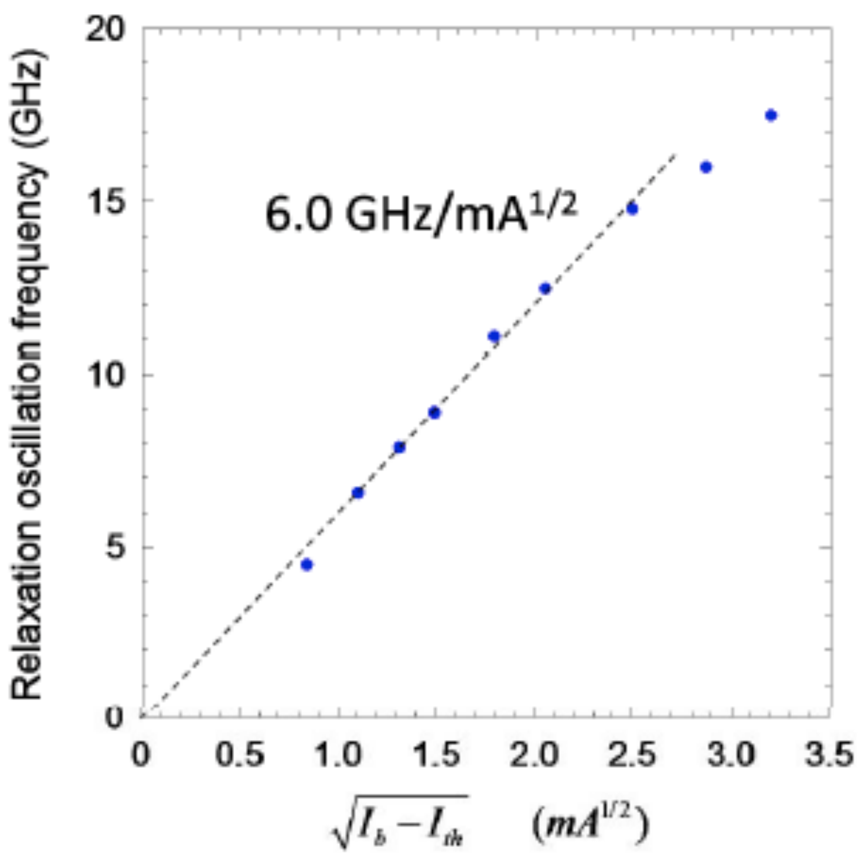




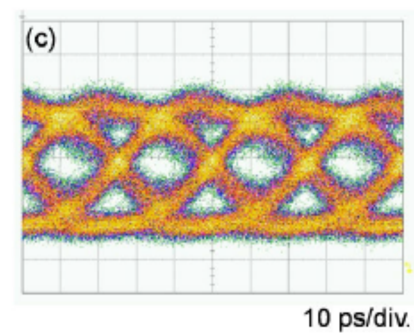
40-Gbit/s Direct Modulation of Membrane Buried Heterostructure DFB Laser on SiO_2/Si Substrate

Shinji Matsuo, Takuro Fujii, Koichi Hasebe, Koji Takeda, Tomonari Sato, and Takaaki Kakitsuka

NTT Photonics Laboratories, NTT Corporation



40 Gbit/s



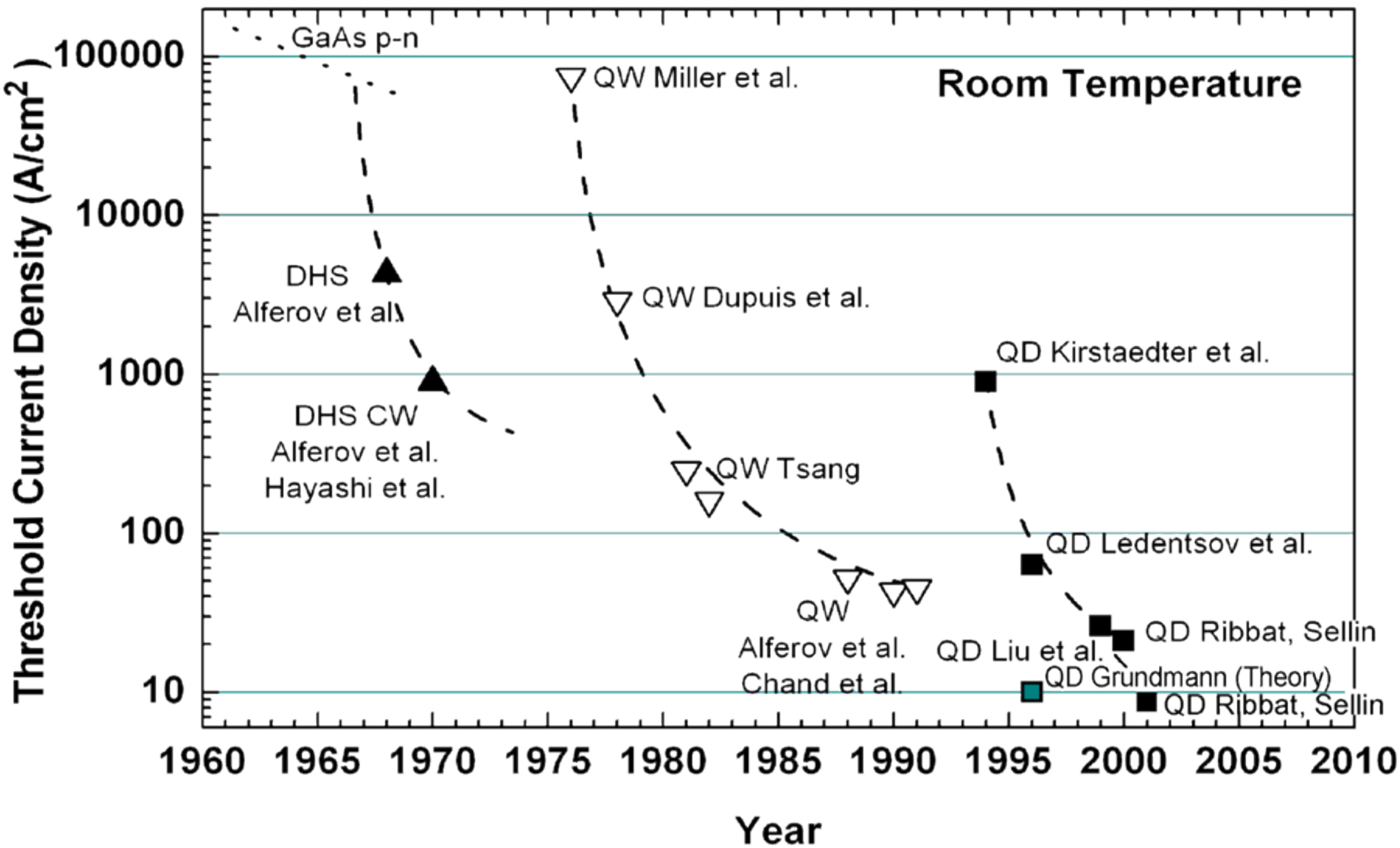
377 fJ/bit

Quantum Dot Lasers

Lower threshold

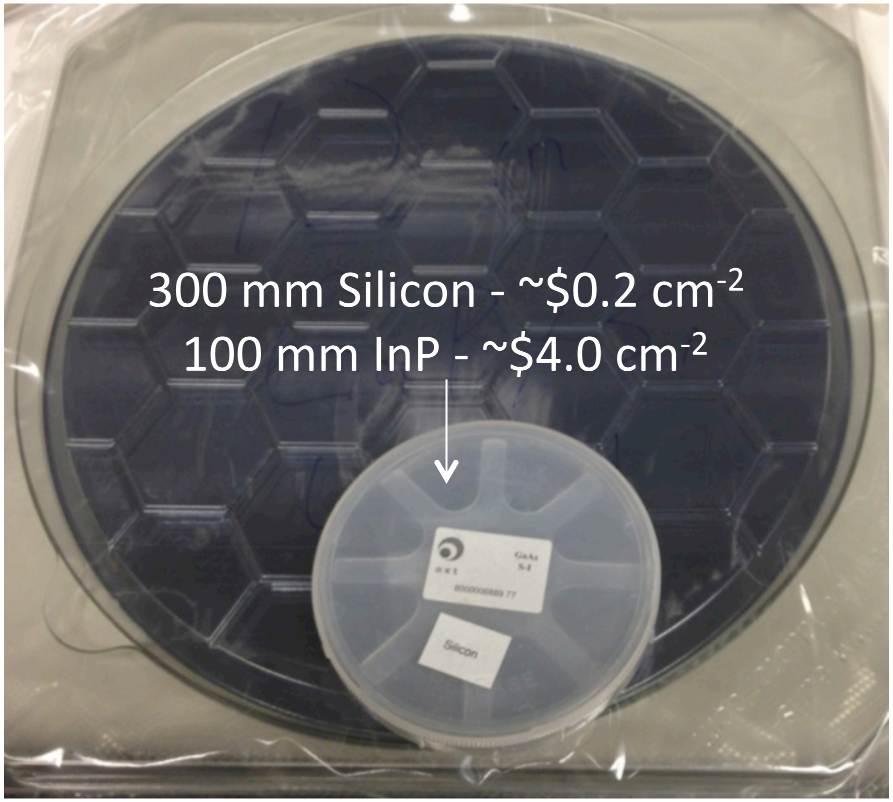
Lower cost (epitaxial growth on Si)

Threshold Current Densities of Semiconductor Lasers



QD-lasers for lower power

III-V Laser Growth on Silicon



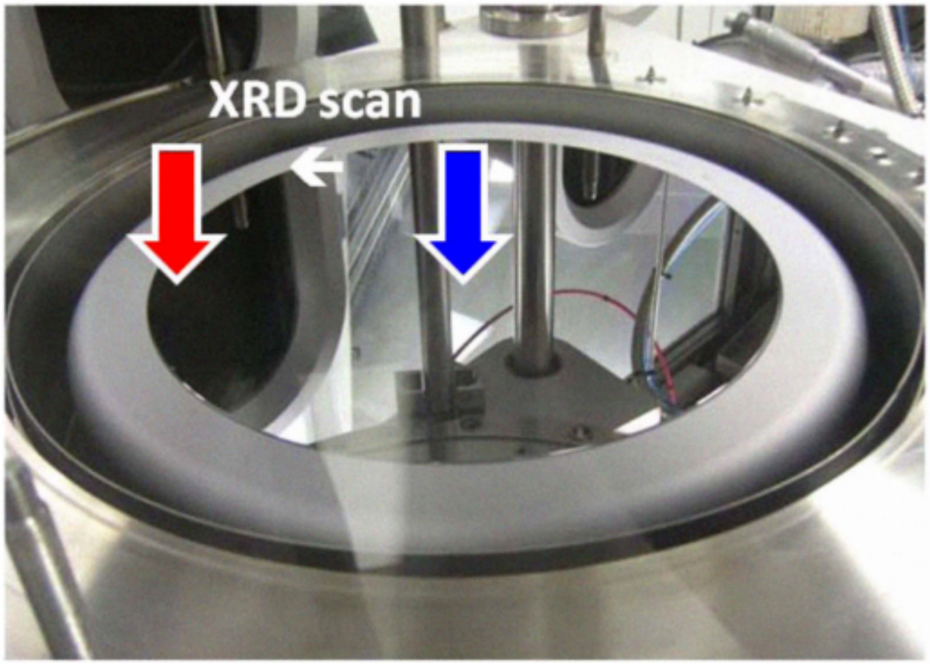
(Photo courtesy of Dr. Jordan Lang, Yale)

- CMOS processing of photonics is already happening, yet high cost and small size of III-V wafers remains an issue.
- **Goal:** Grow III-V lasers on larger and cheaper silicon substrates without sacrificing laser performance for <u>lower cost and higher throughput.</u>

[1] Bowers, John E., et al. "A Path to 300 mm Hybrid Silicon Photonic Integrated Circuits." OFC 2014

III-V growth on 300 mm Silicon Wafers

GaP on 300 mm Silicon using MOVPE



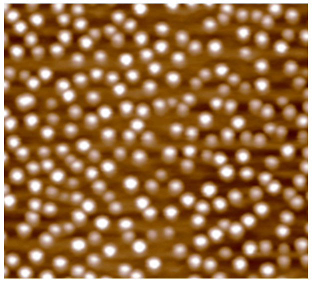
B. Kunert *et al*. *69th Device Research Conference,* Santa Barbara (2011)

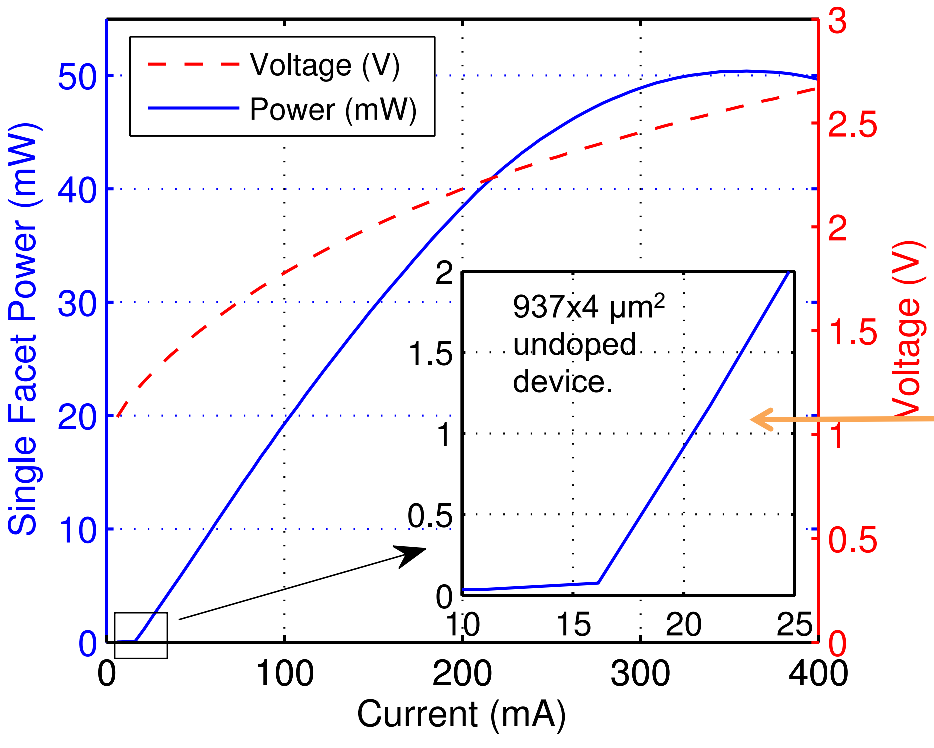
GaAs on300 mm Silicon using MBE

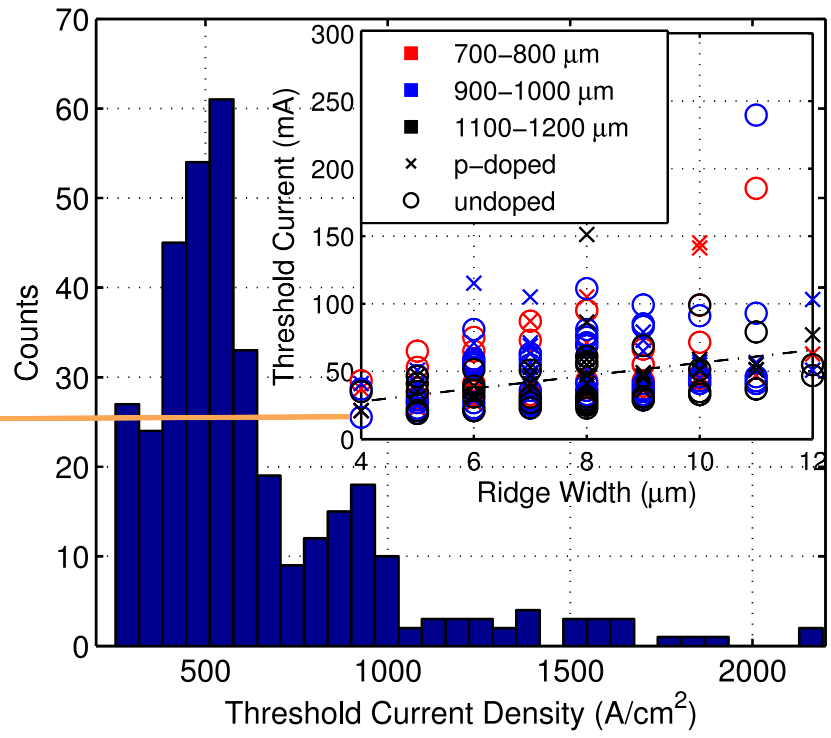
Amy Liu, IQE Inc.

Low Thresholds

- Uniform threshold current densities across die/wafers.
- Low CW threshold (150 A/cm^2)



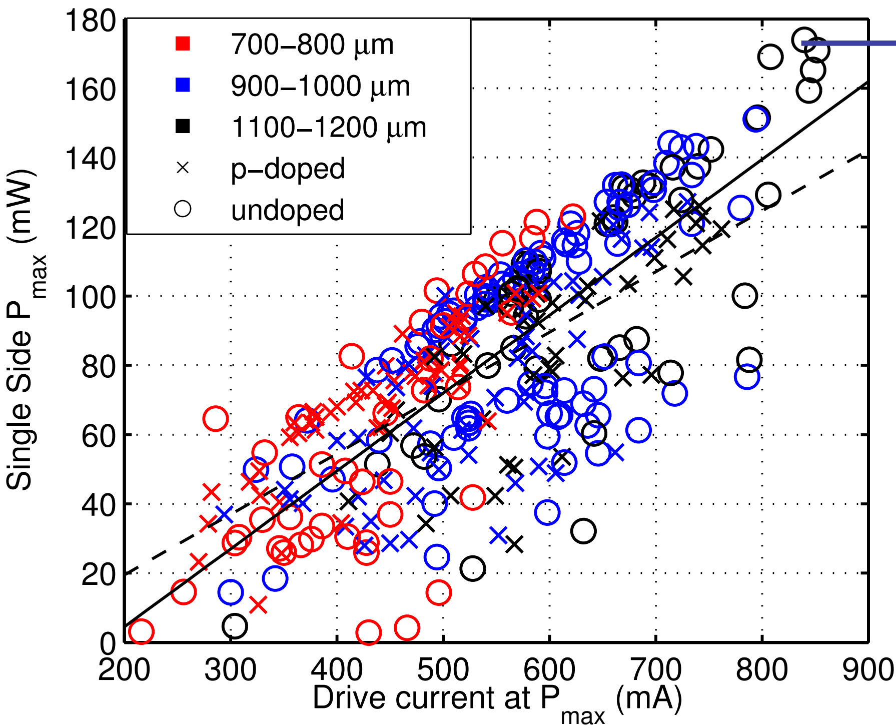


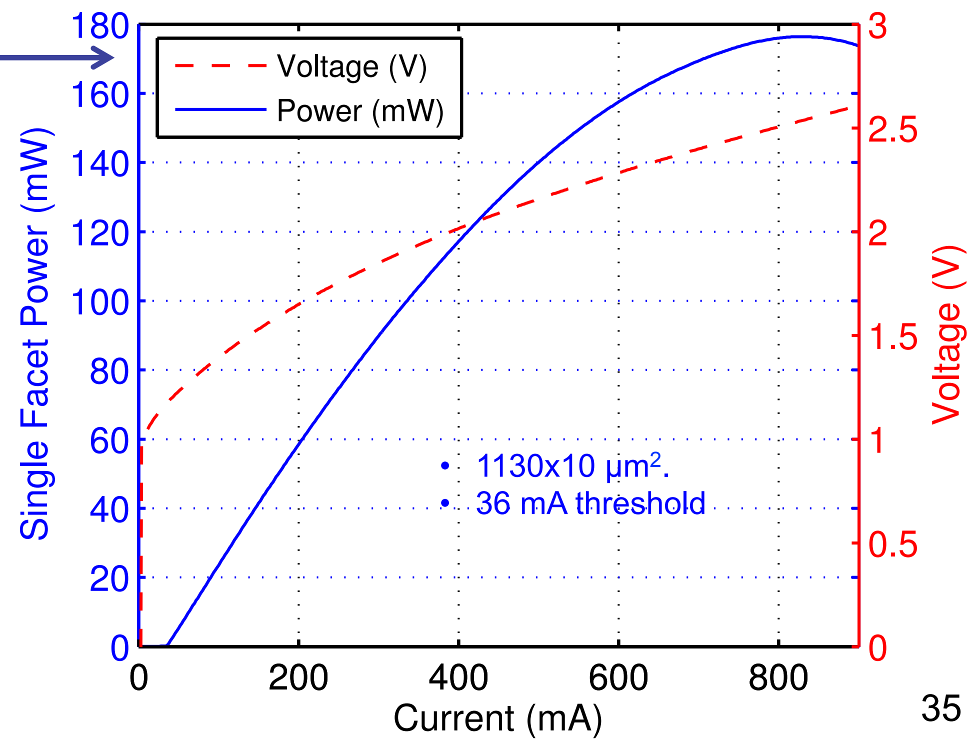


Liu, Alan Y., et al. "High performance continuous wave 1.3 μm quantum dot lasers on silicon." Applied Physics Letters 104.4 (2014): 041104.

High Output Powers

- CW powers over 100 mW routinely achieved.
- Nearly 180 mW maximum CW single side output power at 20 °C from HR coated 1130x10 μm² intrinsic active region (undoped) device.
  - 33% differential efficiency and 18% WPE (at 150 mA)

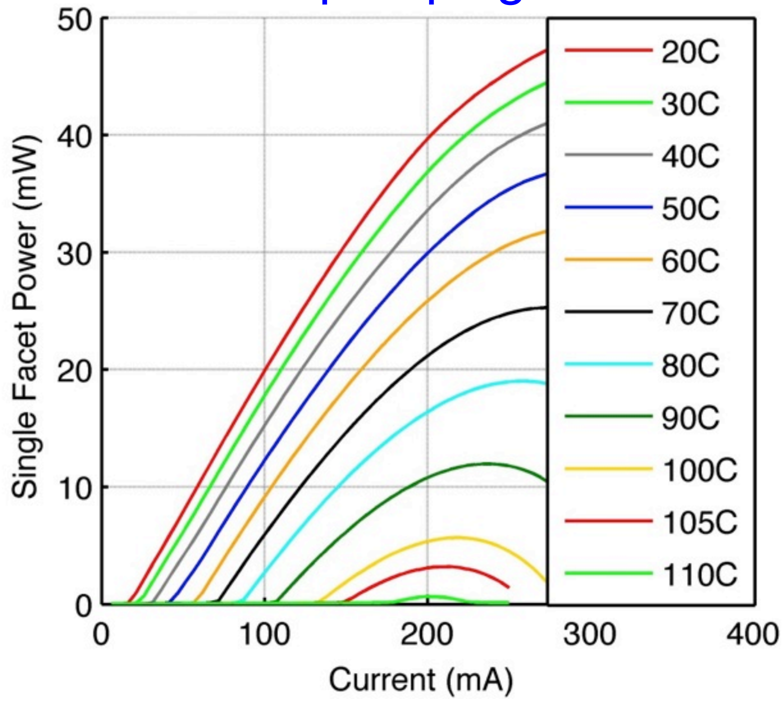




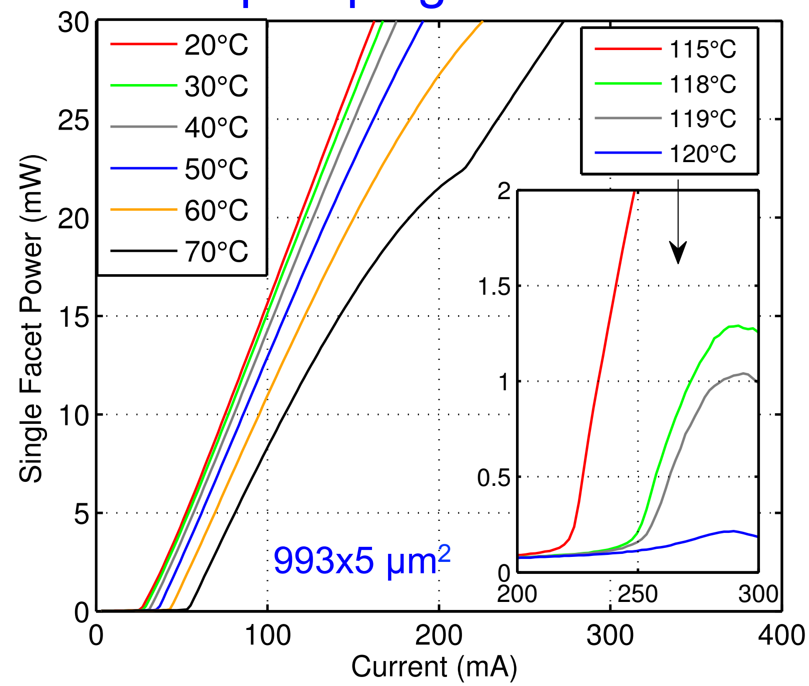
High Temperature Performance

- P-doping the active region improves thermal performance.[1]
- Continuous wave lasing up to 119°C
  - (dual state lasing at high currents/temperatures).

Without p-doping



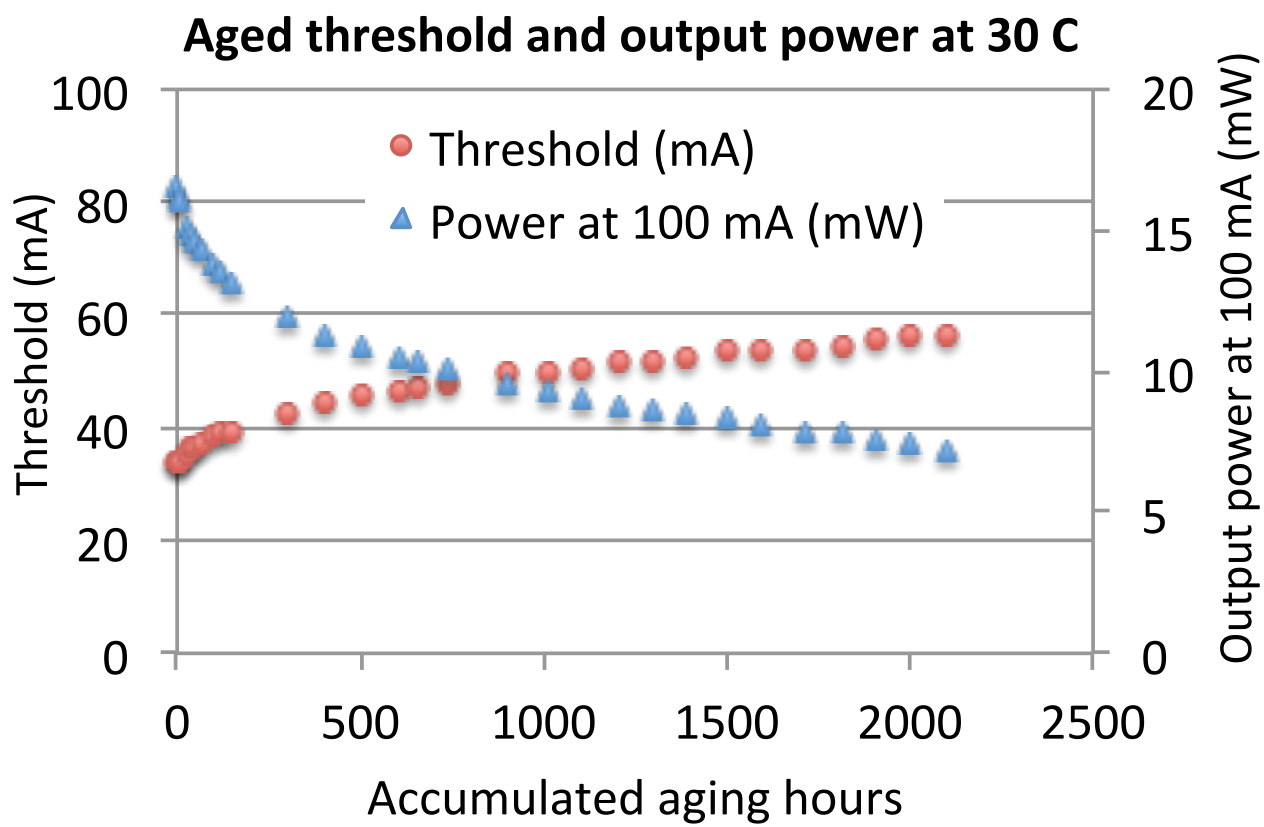
With p-doping



[1] Alexander, Ryan R., et al. "Systematic study of the effects of modulation p-doping on 1.3-μm quantum-dot lasers." Quantum Electronics, IEEE Journal of 43.12 (2007): 1129-1139.

Reliability Studies of QD lasers on Silicon

- Lattice mismatch causes dislocations, which have limited quantum well laser reliability on Si.
- Over **2100 hours** of continuous operation
- **>26x** improvement over best reported lifetime for GaAs laser on Si
- Not yet adequate for real applications



Heterogeneously Integrated Quantum Well Transmitters

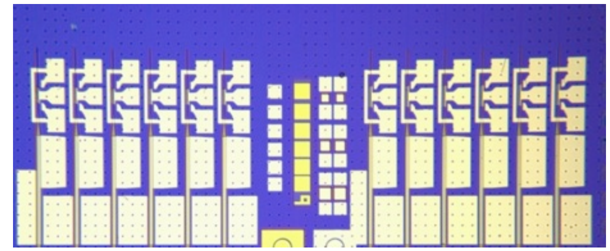
Modulators

Photodetectors

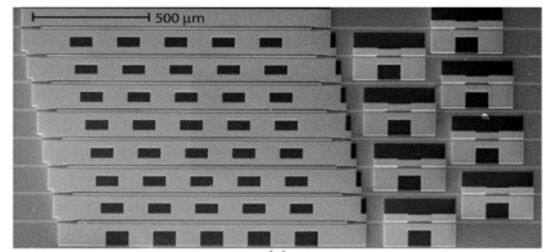
Integrated Transmitters

Active Elements needed for PICs

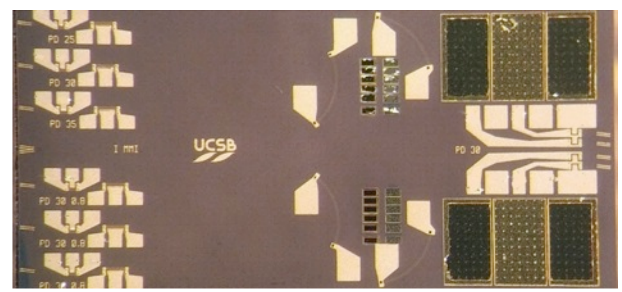
- Range of components for PICs:
  - Lasers
  - Modulators
  - Amplifiers
  - Photodetectors
- Integration
- High yield
- Good reliability



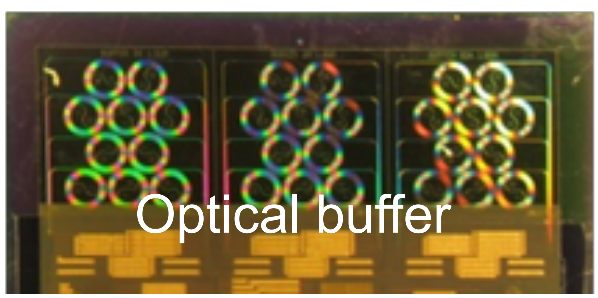
DFB/EAM/PD Array



Optical preamplifier PD array



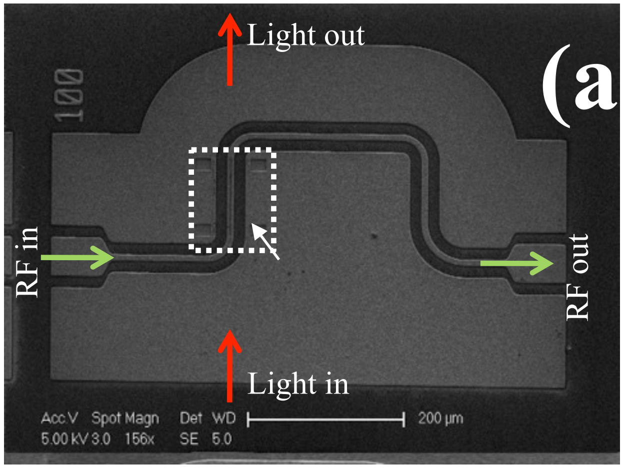
DQPSK Receiver

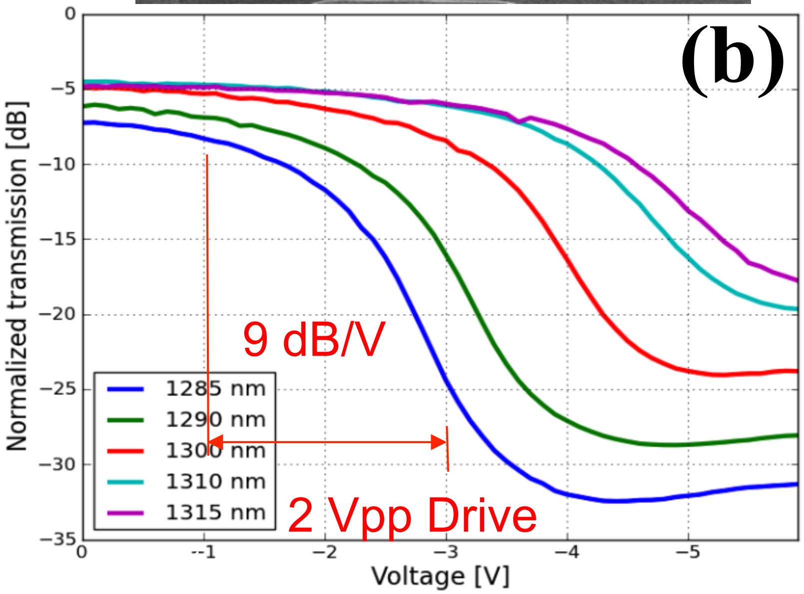


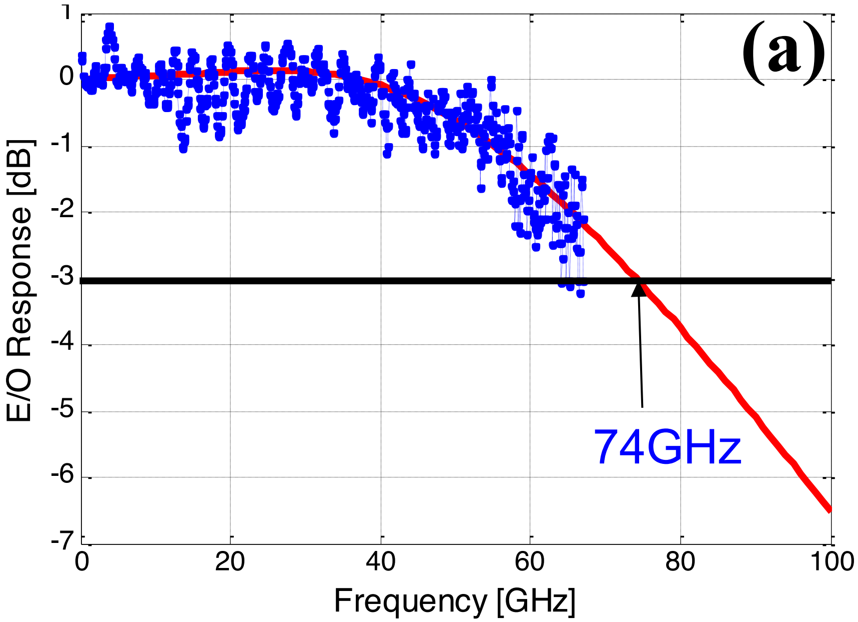
Optical buffer

Hybrid Silicon Electroabsorption Modulator

- Segmented electrode
- Length: 100 µm
- >67 GHz Bandwidth



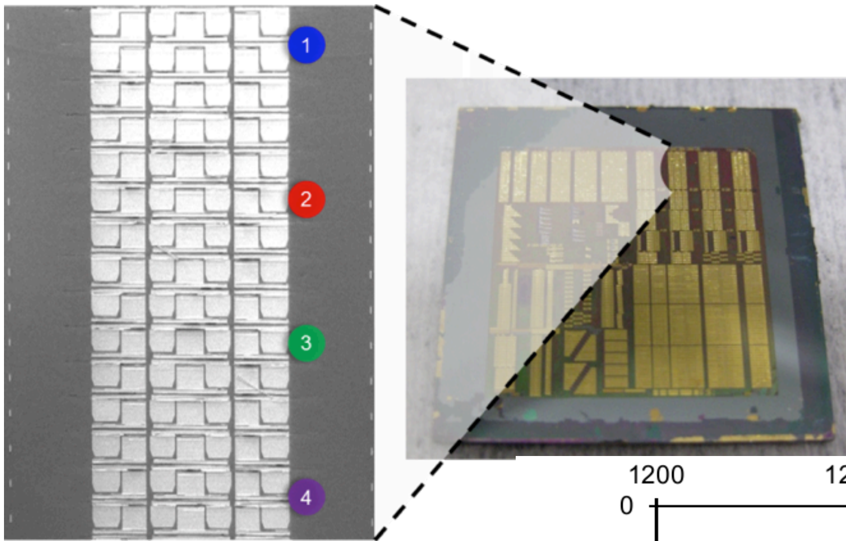




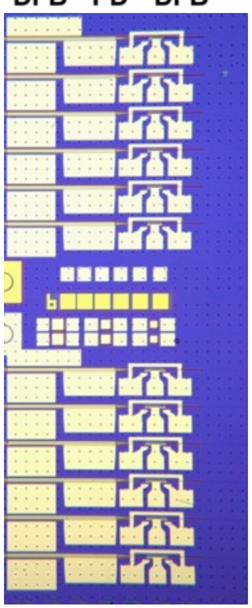
330 fJ/bit

Tang, Peters, Bowers OFC Postdeadline 2012

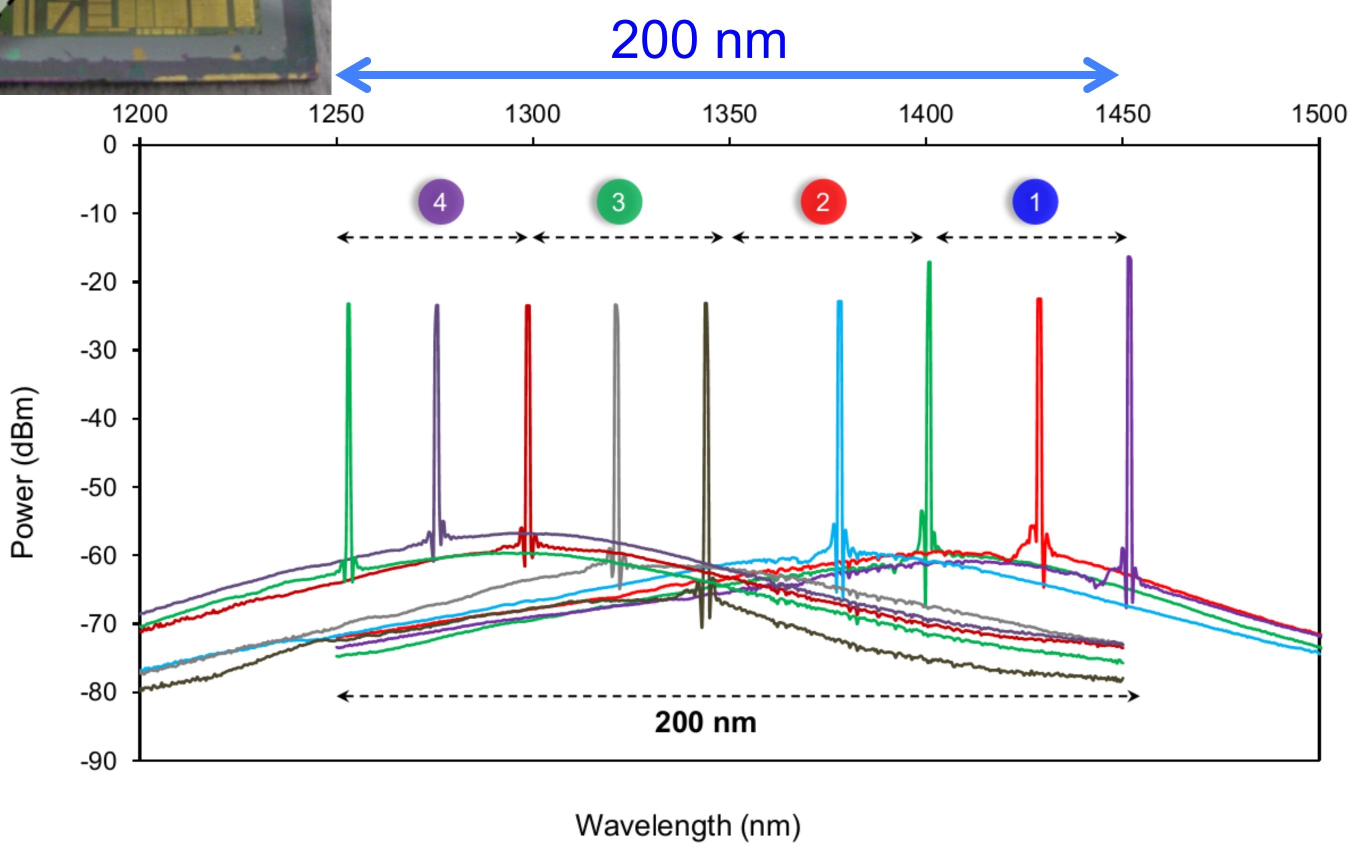
Integrated Transmitters
Using Quantum Well Intermixing



DFB PD DFB



PD DFB EAM

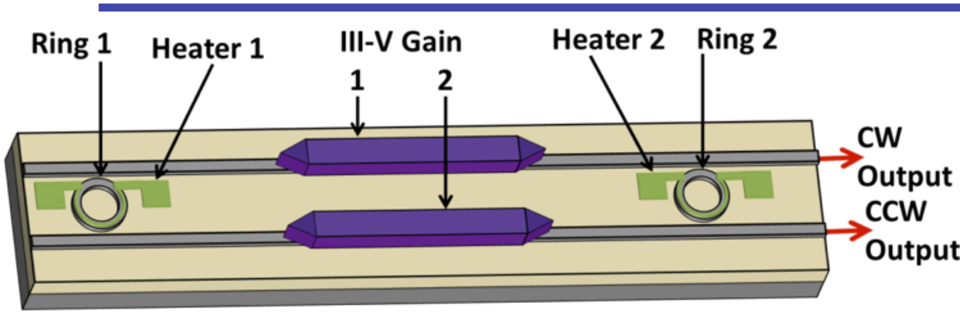


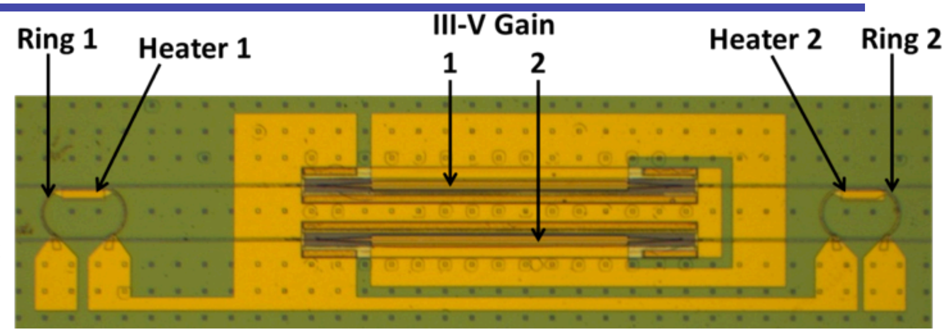
Tunable Lasers

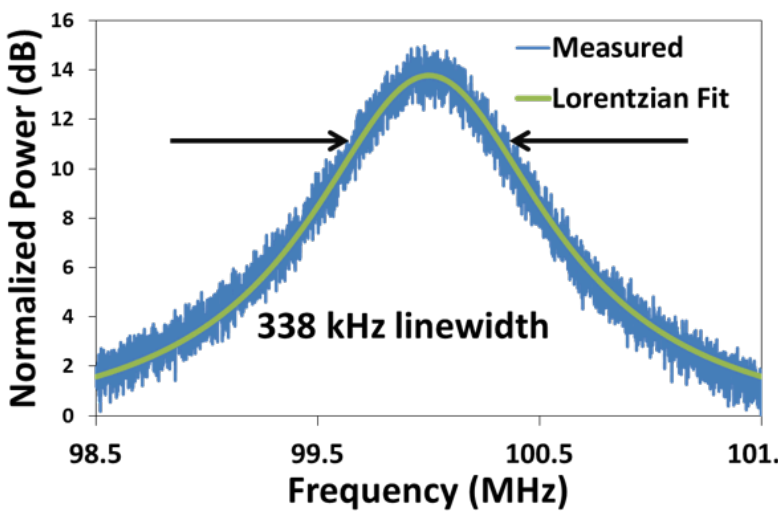
UCSB

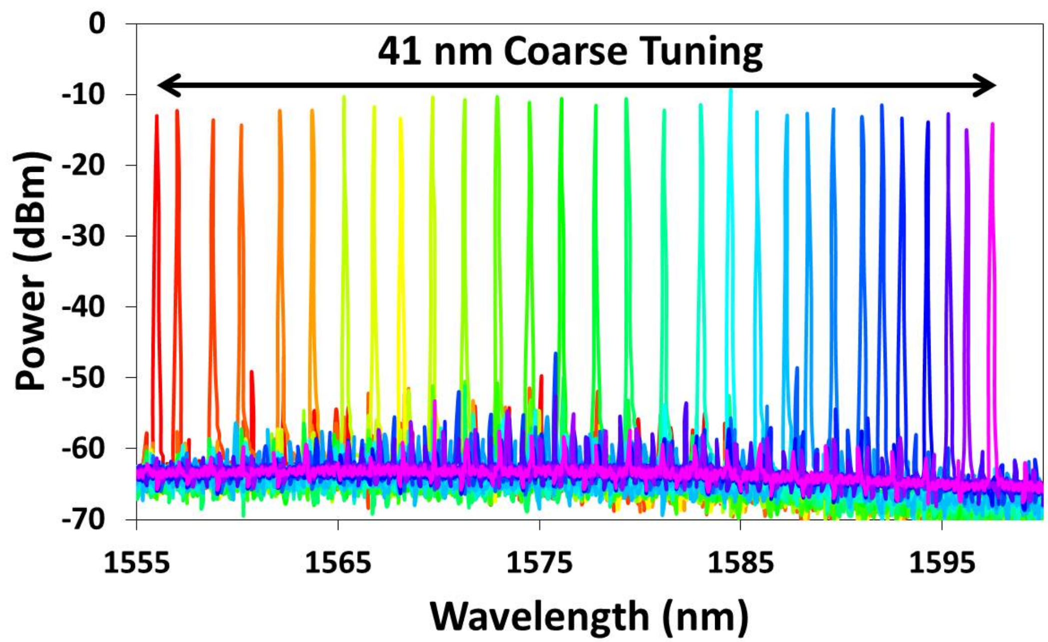
Ghent

Widely Tunable Vernier Ring Laser







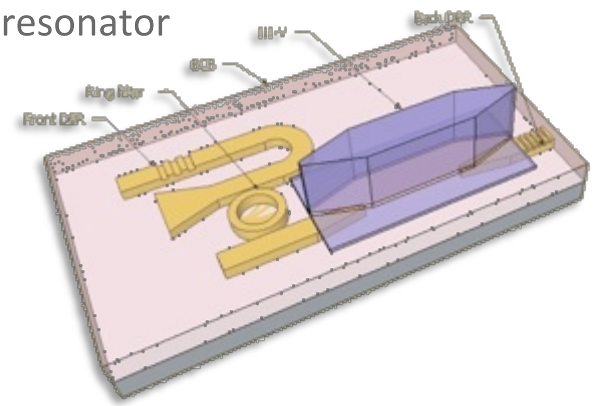


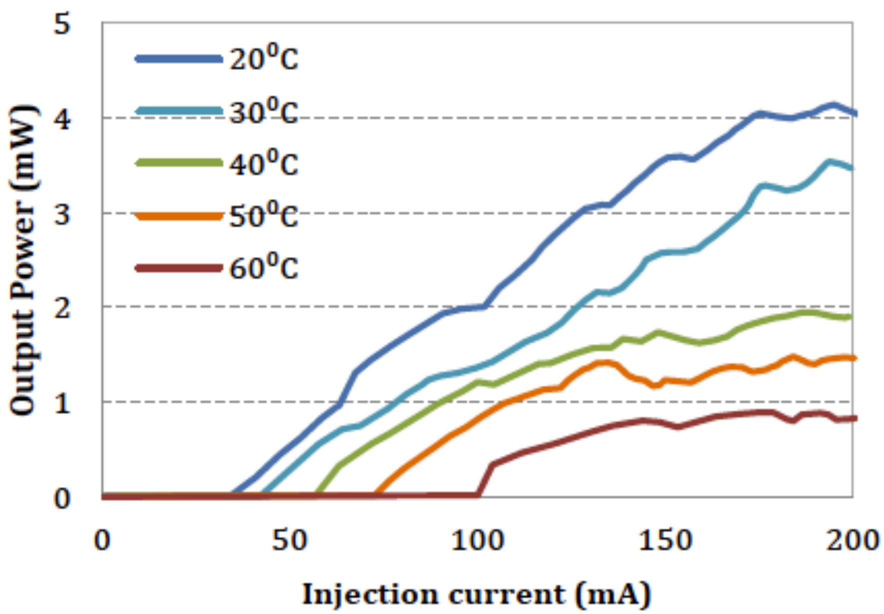
J. C. Hulme, J. K. Doylend, and J. E. Bowers, "Widely tunable Vernier ring laser on hybrid silicon," Opt. Express **21**, 19718-19722 (2013)

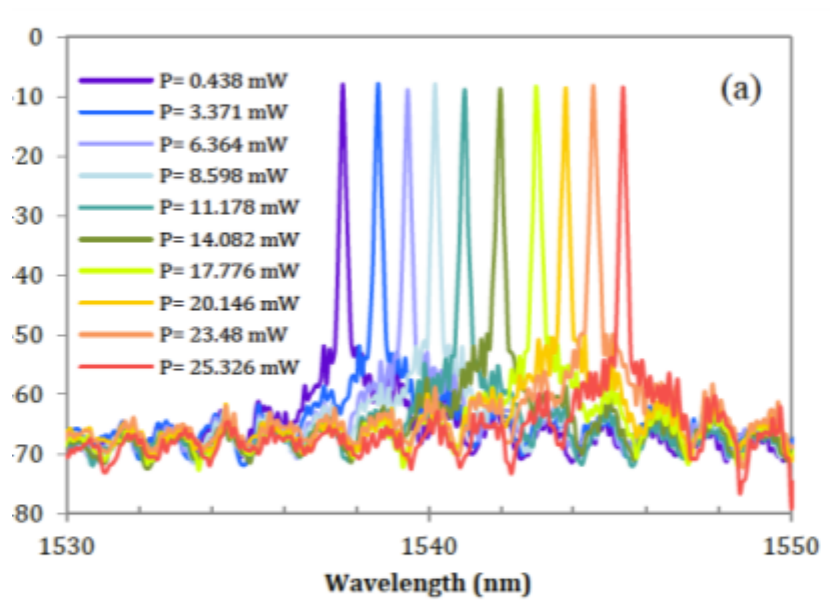
III-V/Si extended cavity laser

III-V/silicon tunable laser

- 8nm tuning range, based on thermo-optic tuning of silicon ring resonator
- > 40dB SMSR
- threshold of 35mA
- 4mW optical output power
- co-integrated with 10G silicon electro-optic modulator
- Realized in EU-project HELIOS (jointly with CEA-LETI, III-V labs)







Keyvaninia, Opt Express 2012

Integration

2D Scanners

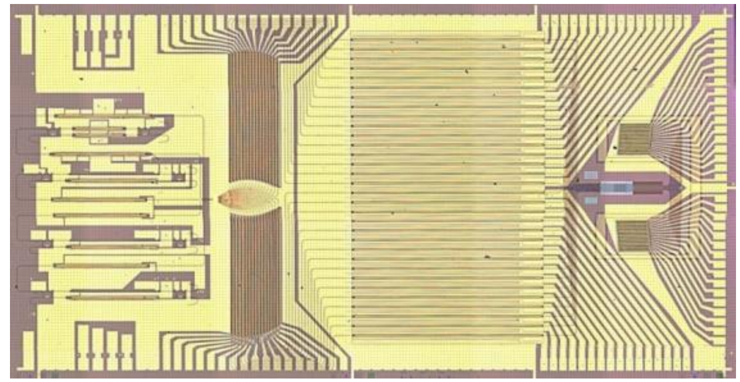
Triplexers

Buffer Memories

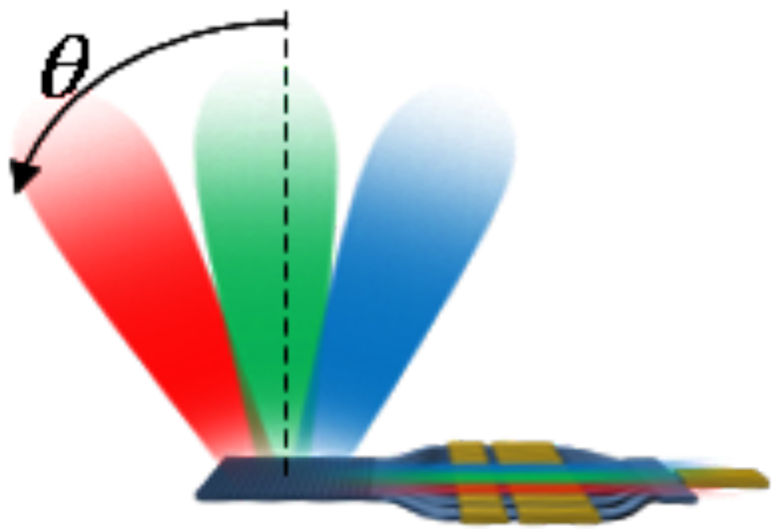
Mode Locked Lasers

Fully Integrated hybrid silicon free-space beam steering source using a tunable laser phased array

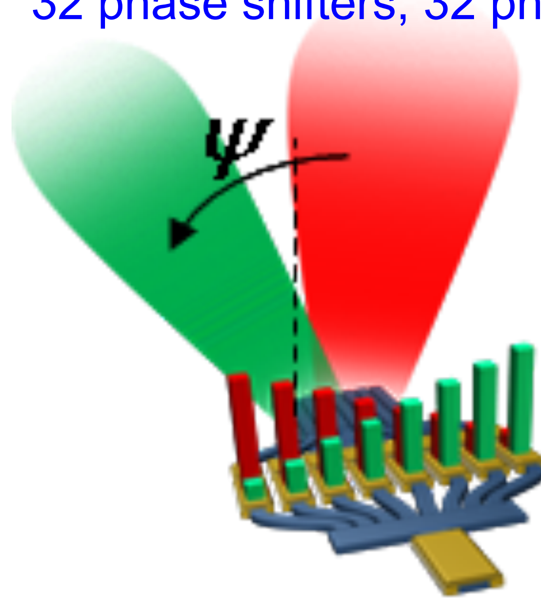
2D Scanning with
- Tunable laser and grating for θ
- Phased array emitter for ψ



4 tunable lasers, 32 amplifiers,
32 phase shifters, 32 photodetectors



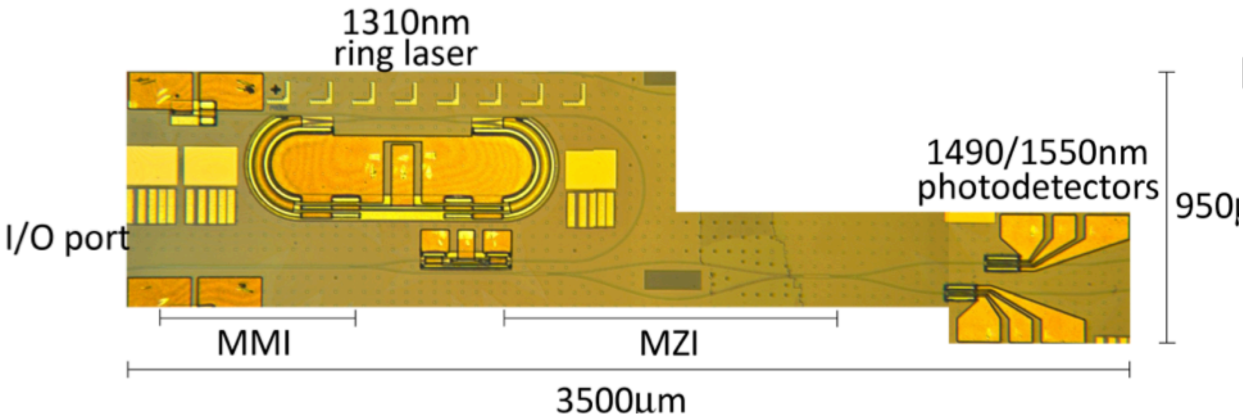
1 (wavelength)

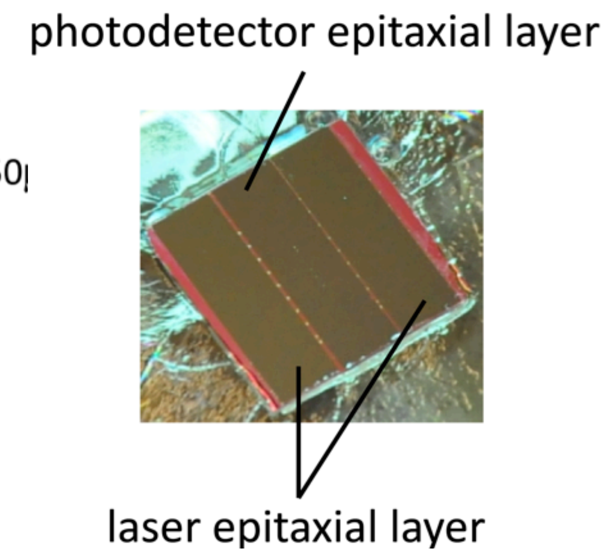


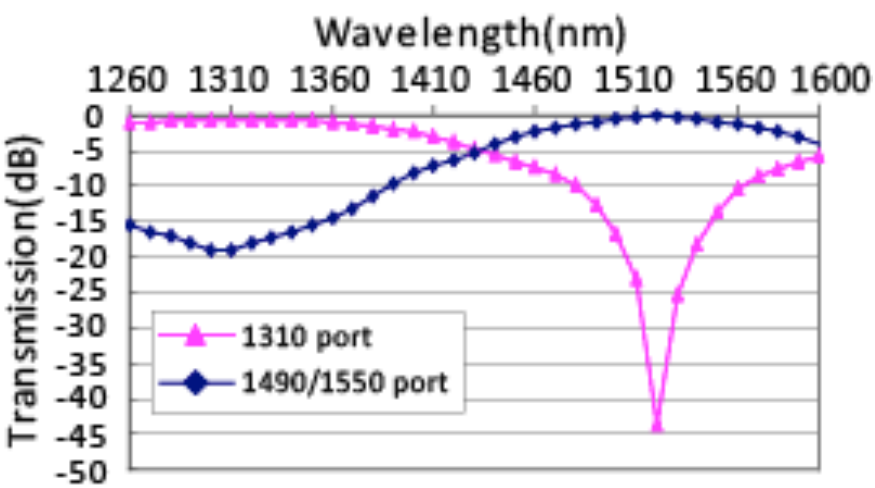
N (number of emitters)

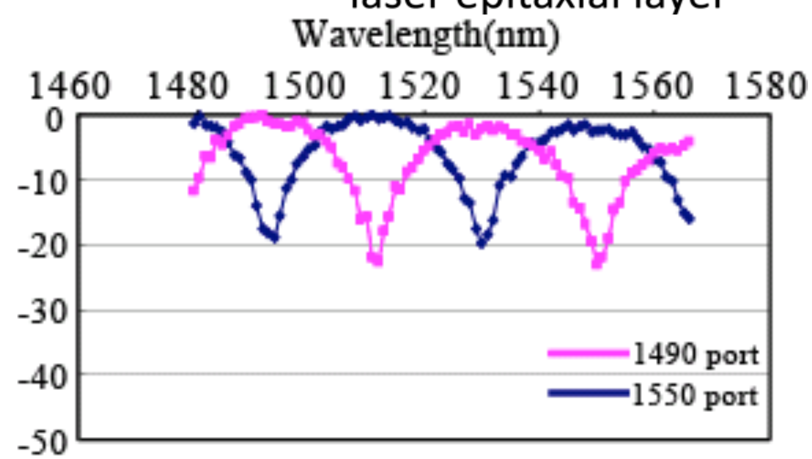
Hybrid Silicon Triplexers (FTTH)

Laser, 1310/1500 nm MUX MMI, MZI 1550/1490 MUX, PDs integrated



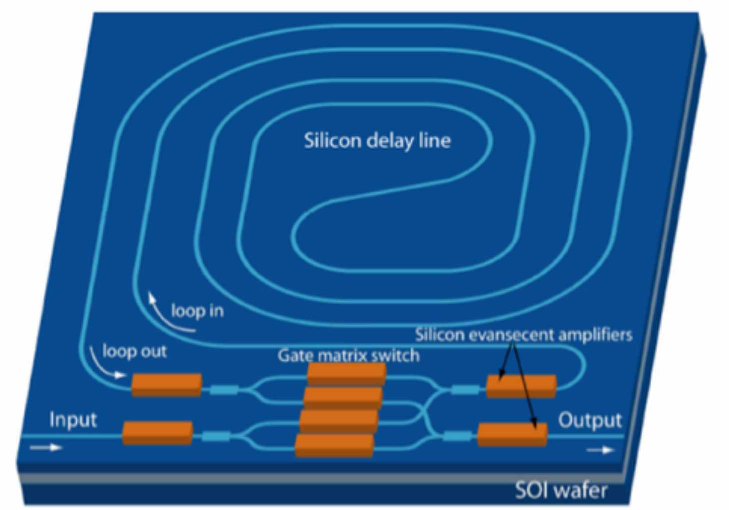


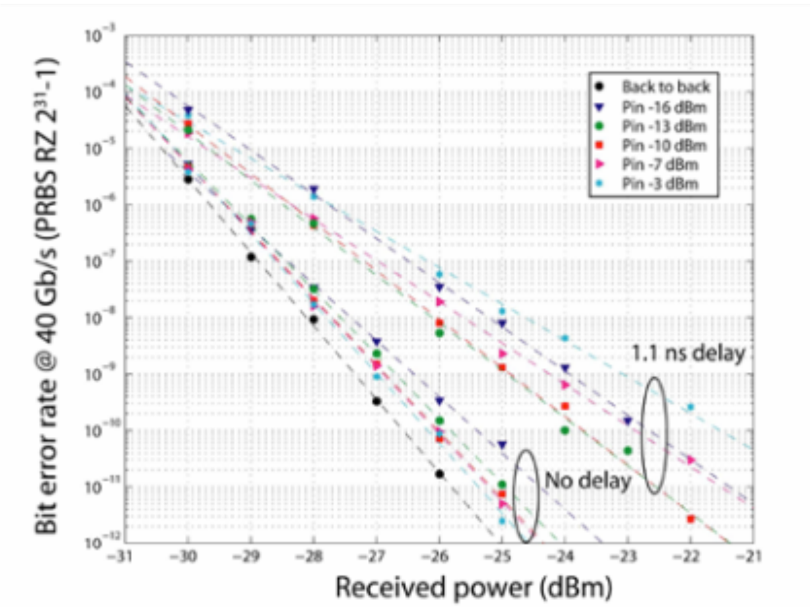


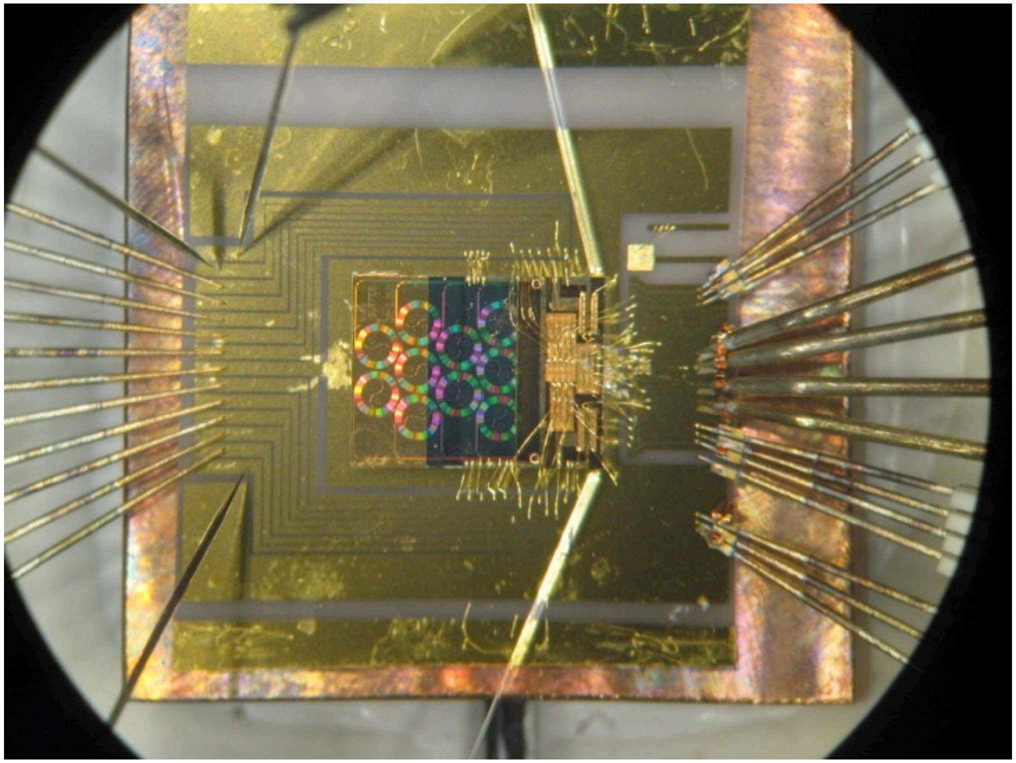


Chang et al. OFC 2010

40 Gb/s Optical Buffer Memory







Integration with Electronics

Co-processed (expensive)

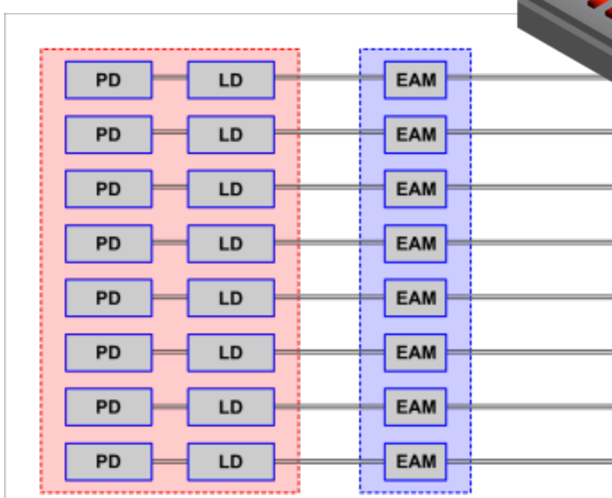
Bump bonded

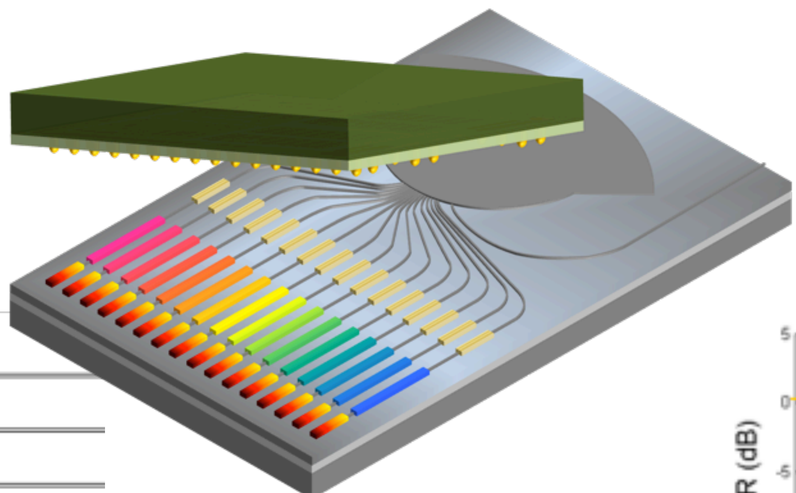
Inserted

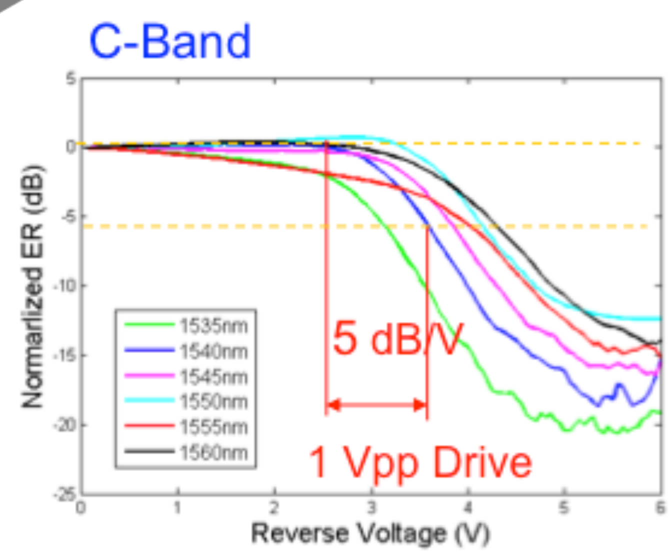
Integration of DFB and EAM on hybrid silicon platform with Oracle ICs

Low power, high speed, integrated photonic transmitter based on hybrid silicon platform

- High capacity optical interconnects between processors and memory.
- Low power optical transmitters with high impedance modulators Flip chip bonding with CMOS driver chip

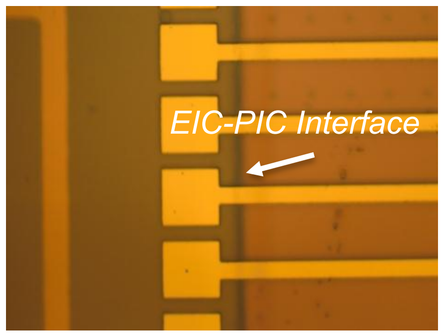


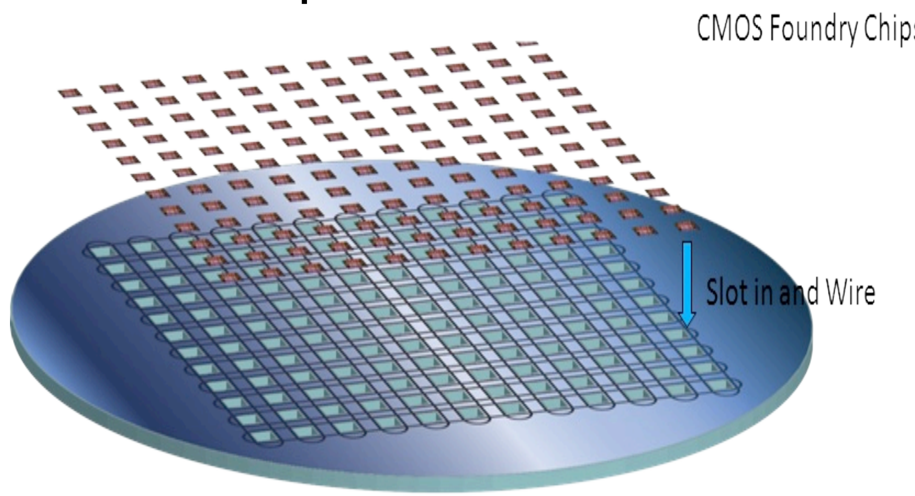


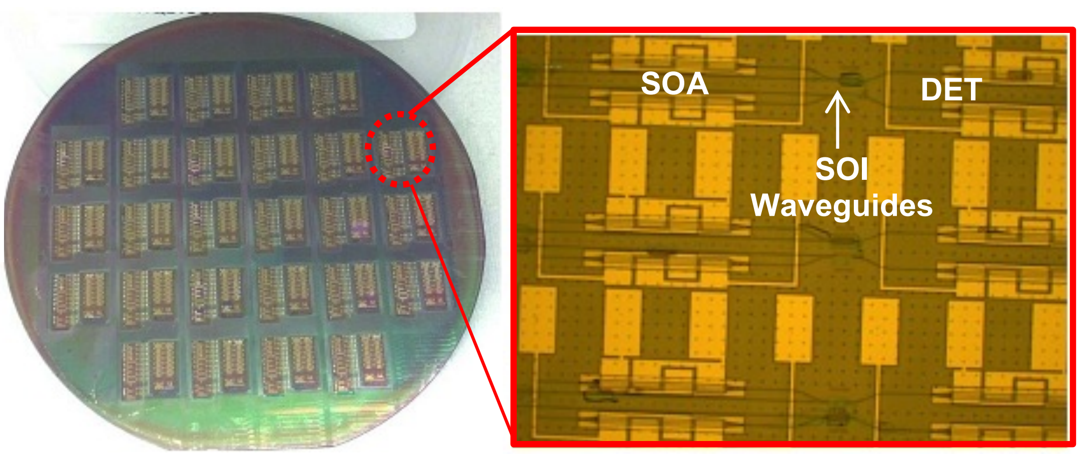


CMOS Integration in Photonic IC

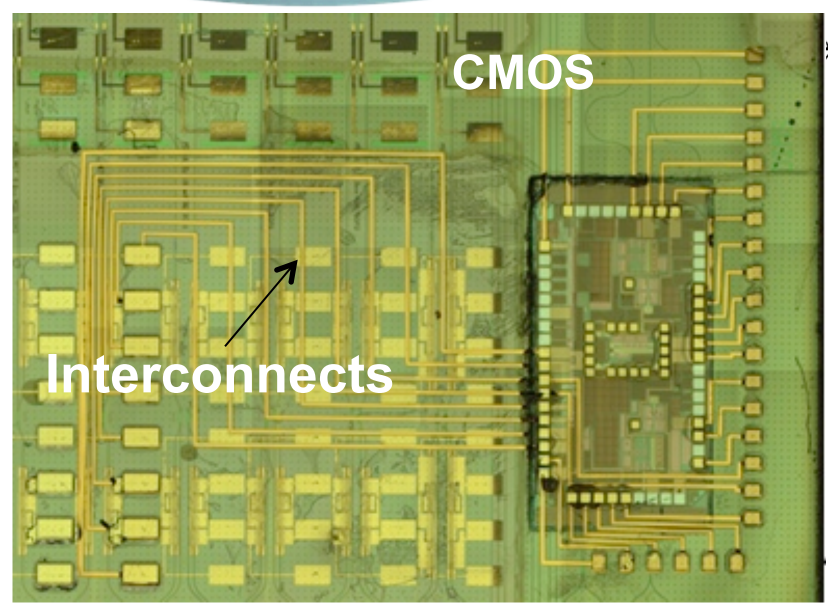
- "Smart Photonics" – Integrated electronic w/ photonic ICs
- Avoid driving 50Ω terminations
- Active feedback control
- Self-calibration







Hybrid Silicon PIC from Aurrion



L. Chen, A. Sohdi, J. E. Bowers, and L. Theogarajan, "Electronic and photonic integrated circuits for fast data center optical circuit switches", IEEE Communications Magazine , **Invited Paper**, Volume: 51 Issue: 9 Pages: 53-59, 5, September 2013

Commercialization

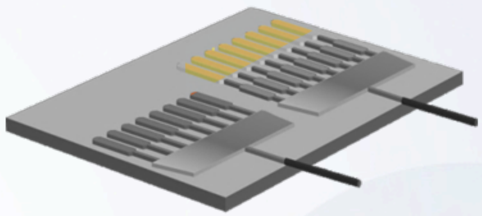
Aurrion

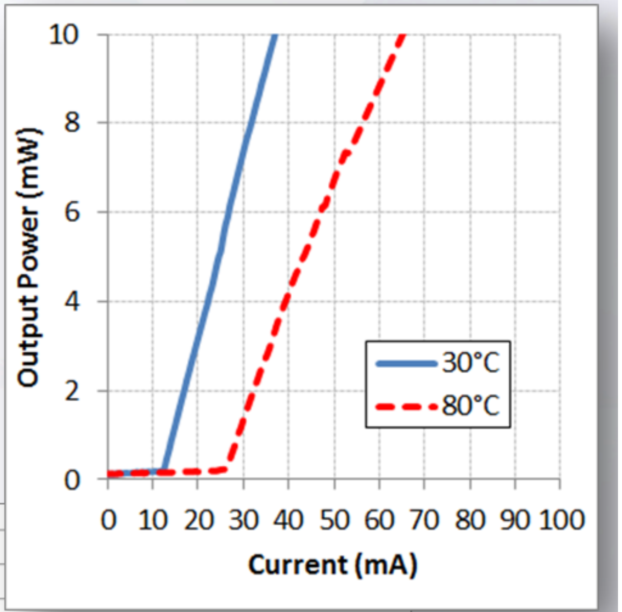
Intel

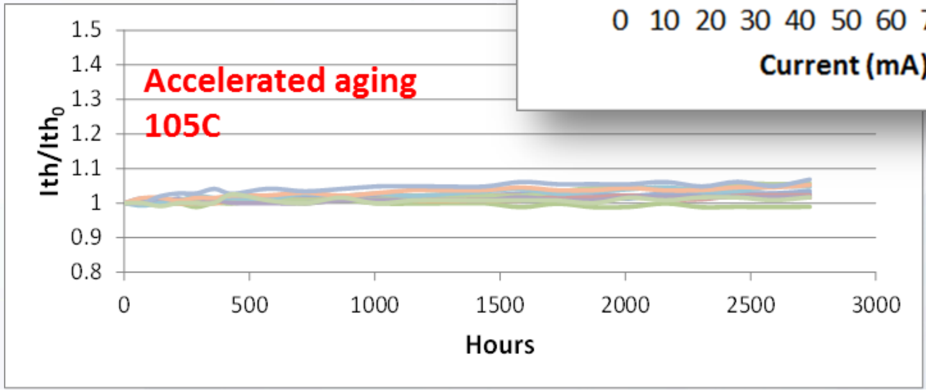
Hewlett Packard

Integrated Lasers

- III-V gain integrated on silicon waveguides
- High power/High efficiency
  - >25% at 30C
  - 15% at 80C
  - >20mW
- Uncooled operation
  - Wavelength-locking across 20-80C) without a TEC
  - 200GHz (or 800GHz)



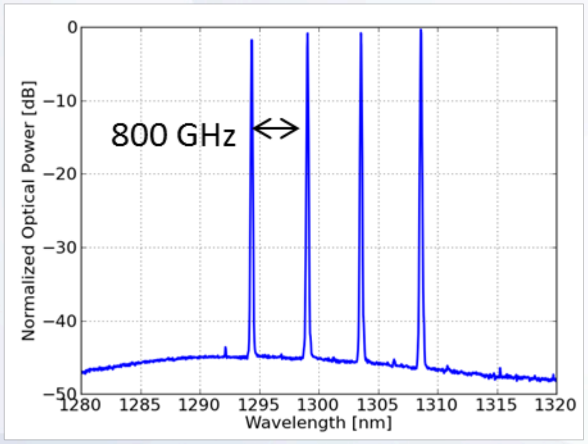




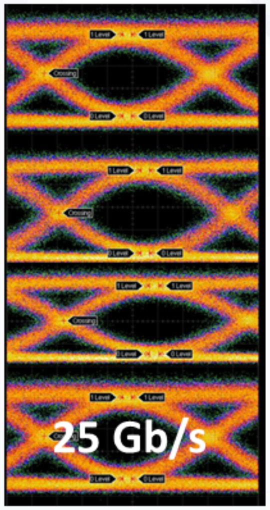
aurrion

100G PIC Links

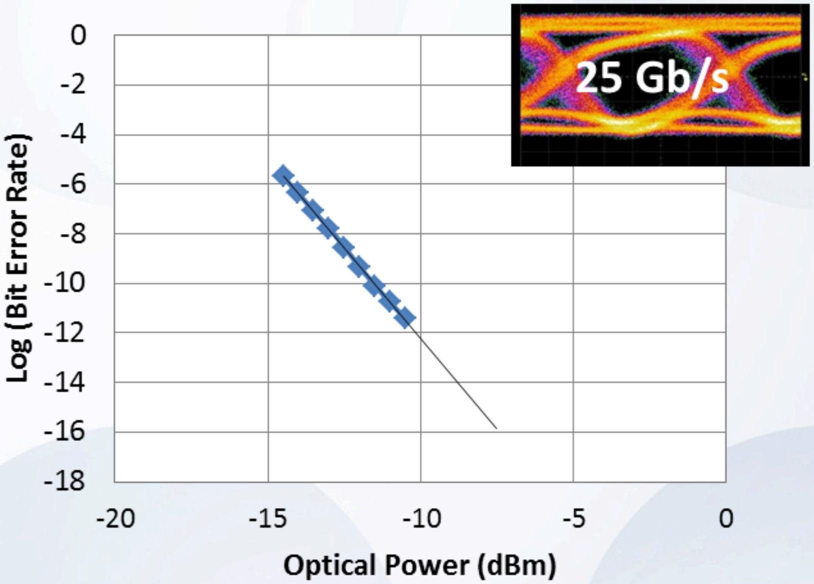
Laser Spectrum



Tx Eye Diagrams

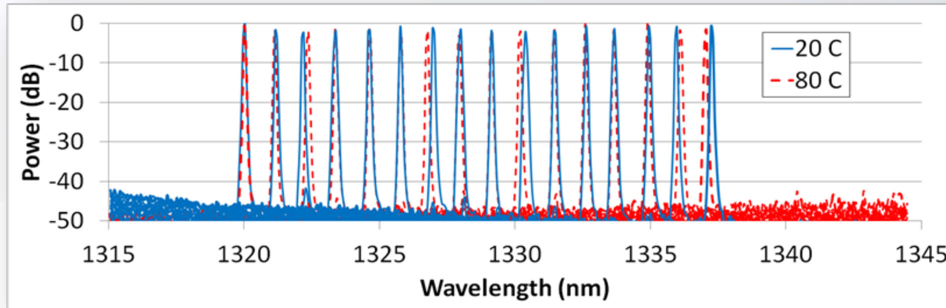


Rx Eye Diagram

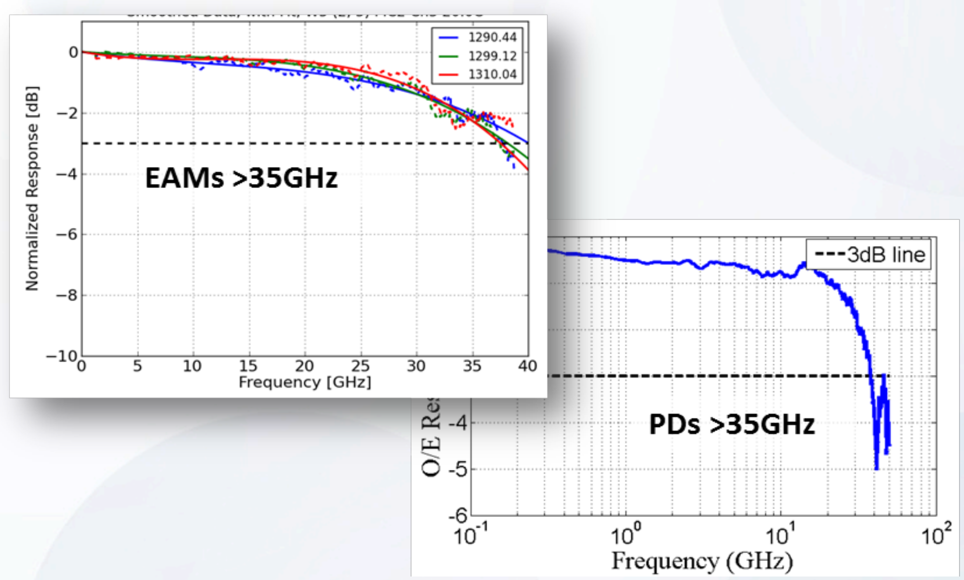


Scaling to 400G+

- **Uncooled 16x laser arrays on silicon demonstrated**
  - Locked to 200GHz grid from 20-80C = no TEC required

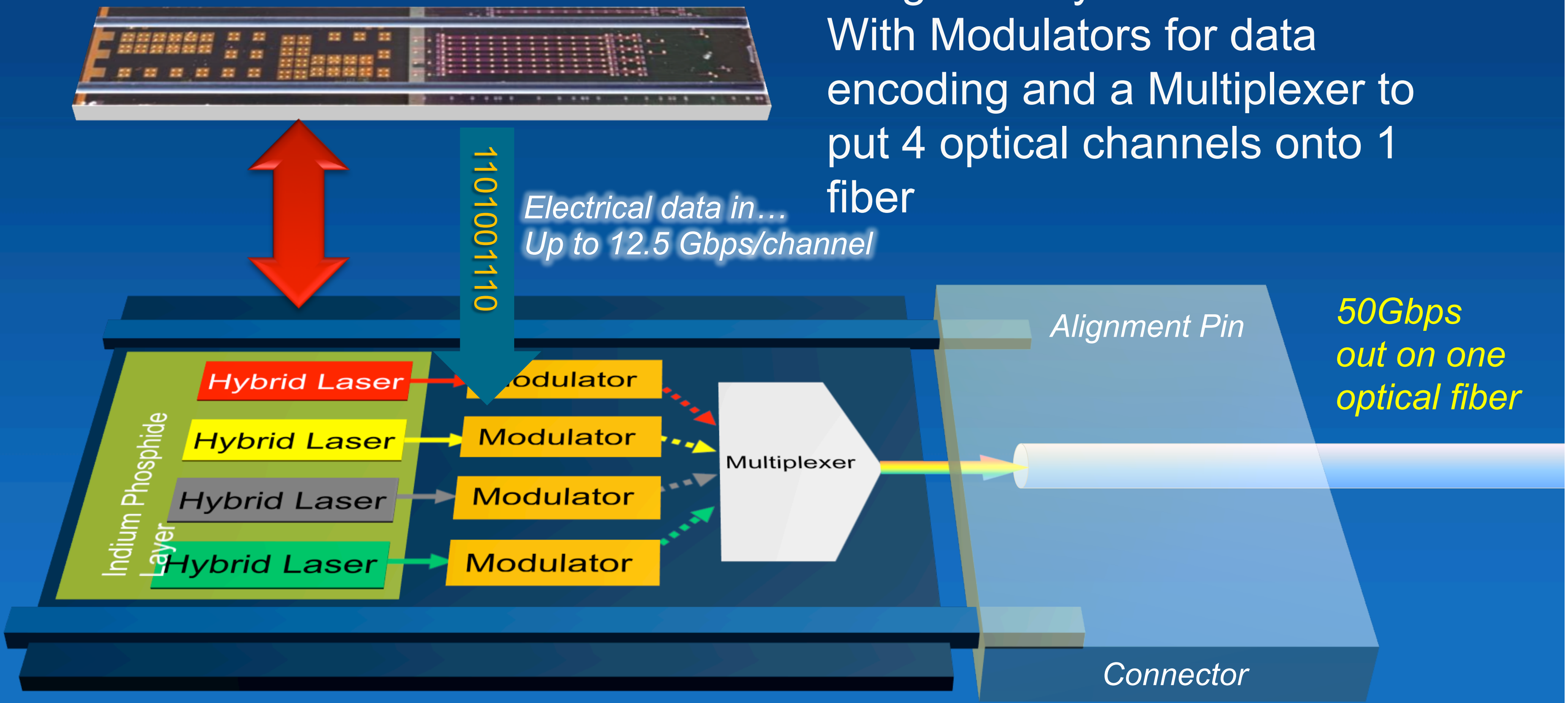


- **3dB bandwith of EAMs & PDs >37 GHz**
  - Supports 50Gb/s



Integrated Transmitter Chip

Integrates Hybrid Silicon Lasers With Modulators for data encoding and a Multiplexer to put 4 optical channels onto 1 fiber



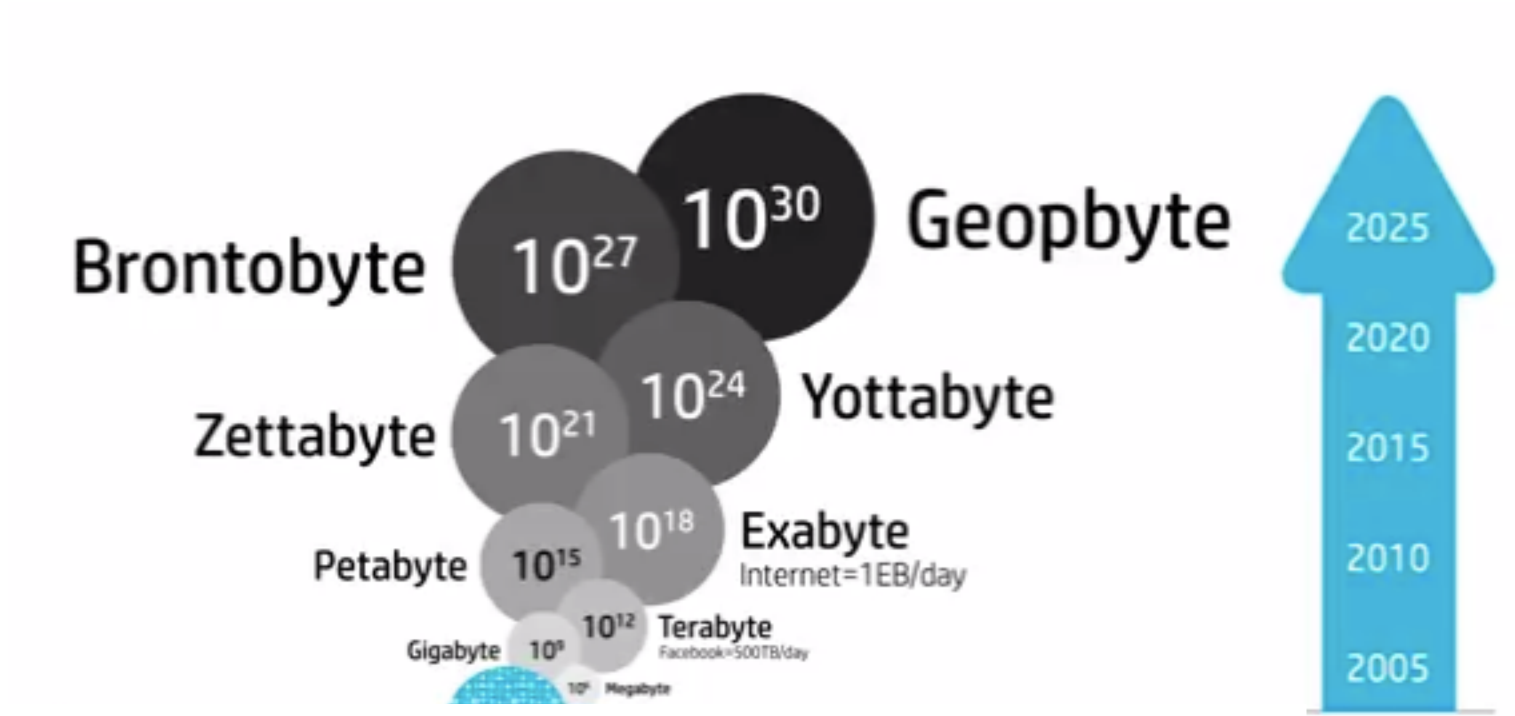
Parallel channels are key to scaling bandwidths at low costs

Sept. 2014: Intel Developer Forum

- **Arista:** Showing Network Products with 100G Intel Silicon Photonics
- **Advantech**: Showing Network Security Appliance with 100G Intel Silicon Photonics
- **Altera**: Showing FPGAs with embedded 100G Intel Silicon Photonics
- **Corning**: Showing the breadth of innovative MXC optical cable technology, along with 100G Intel Silicon Photonics running over a 300m+ distance
- **Fujitsu**: Showing an Application-Optimized Server that enables pooled resources capability provided by Intel Silicon Photonics optical PCI
- **Quanta**: Showing a 100G TOR switch and server with 100G Intel Silicon Photonics
- **Tabula**: Showing a functional demo with 800Gbps of interconnectivity in one box, based on 100G Intel Silicon Photonics

Hewlett Packard: “The Machine”

“The Machine started to take shape two years ago…a new form of memory known as memristors and silicon photonics, the transfer of data inside a computer using light…”

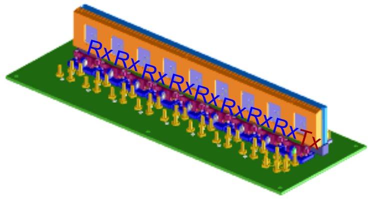


HP’s proposed silicon photonics would also be a big deal. HP, Intel (INTC), and others have been struggling to shrink speedy fiber-optic equipment enough to replace cheap, proven copper wiring inside a computer. In theory, fiber could also replace Ethernet cables and link entire racks of servers together.

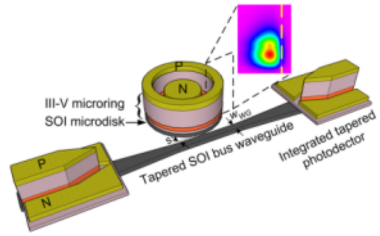
Supercomputing: HP hybrid silicon technologies

Active cable

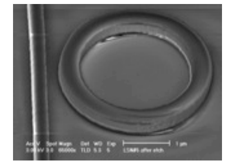
Optical bus



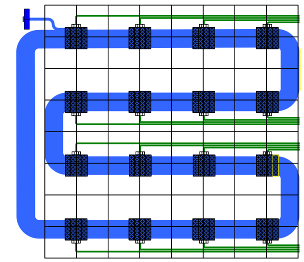
Hybrid microring laser



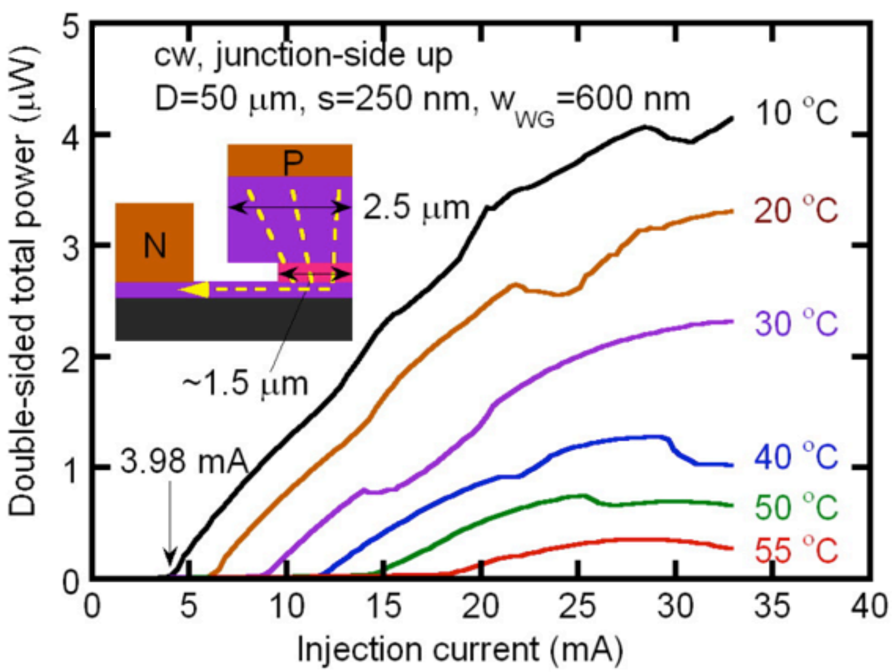
Silicon PIC

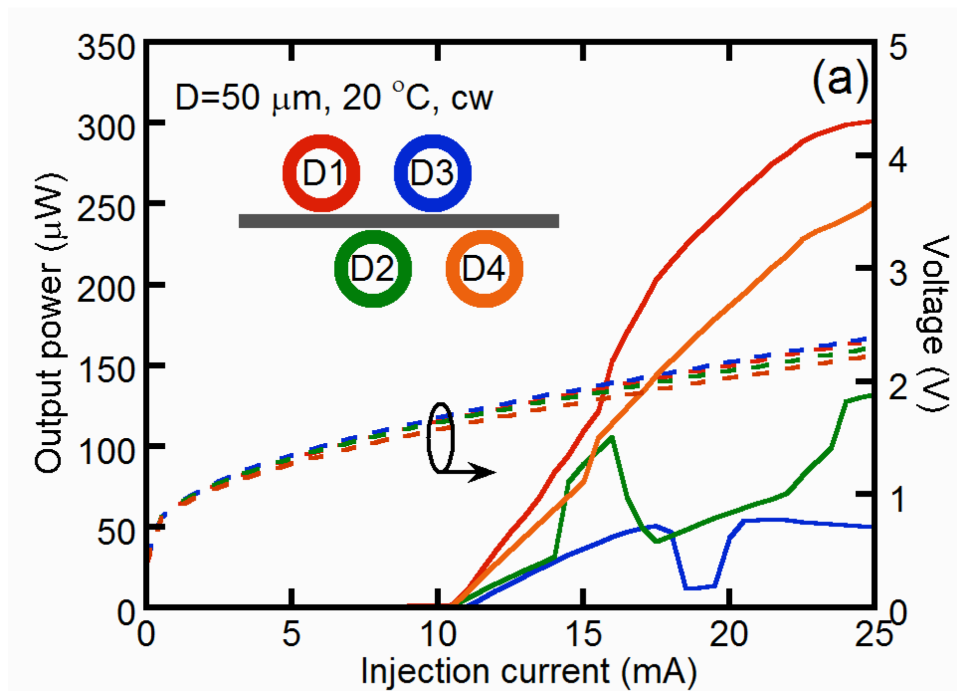


On-chip interconnect



Now → 1 Year → 3 Years → 5 Years → 7 Years → 10 Years





The Future of Hybrid Silicon Photonics

The Path to Tera-scale Data Rates

Today: 25 Gbps x 4 = 100Gbps

25G
25G
25G
25G

Scale UP

50Gbps x 4 = 200Gbps

50G
50G
50G
50G

200G

Scale OUT

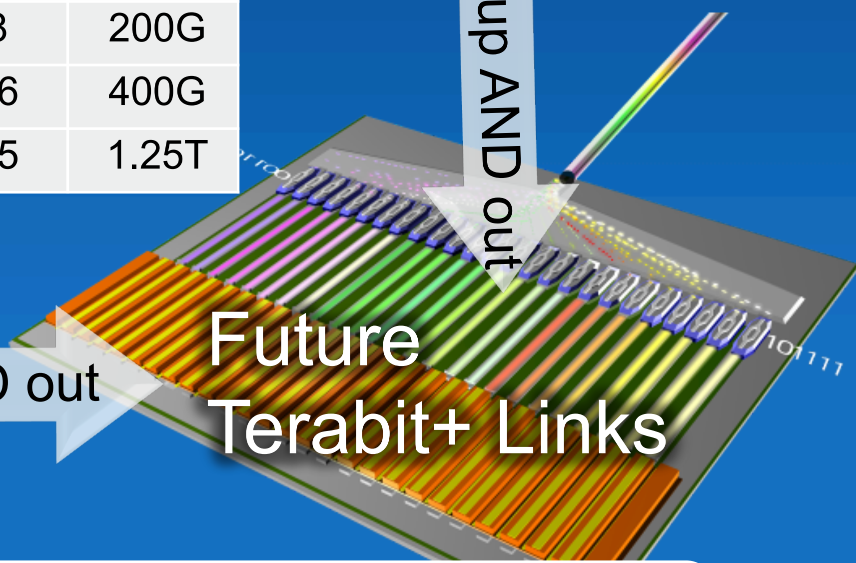
Scale up AND out

Speed	Width	Rate
25	x4	100G
25	x8	200G
25	x16	400G
50	x25	1.25T

25 Gbps x 8 = 200Gbps

25G
25G
25G
25G
25G
25G
25G
25G

Scale up AND out



x16, x32…

Low cost integrated photonics allows for Scaling from 50Gbps to >1Tbps

Summary

- Silicon Photonic Integrated Circuits are here with good performance (and lower cost in volume).
- Integration is essential for size, weight, power and cost reduction and improved yield and reliability
- Photonics can allow lower power and higher capacity for
  - Data Centers
  - Supercomputers
  - Sensors
  - Integrated Circuits with embedded PICs