

Heterogeneously Integrated InP Based Evanescently-Coupled High-Speed and High-Power p-i-n Photodiodes on Silicon-on-Insulator (SOI) Substrate

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Abstract—We demonstrate InP based evanescently-coupled p-i-n photodiodes heterogeneously integrated onto silicon-on-insulator substrate. Using advanced waveguide structures and fabrication processes, it simultaneously achieves 67 GHz O-E bandwidth (RC-free), broad optical window (1520-1600nm) with 0.5 A/W internal responsivity, and high saturation currents (9 mA at 70 GHz).

I. INTRODUCTION

There is an urgent demand for data capacity on the gigabyte scale to satisfy the rapidly growing market for the next generation of wireless access services [1]. Millimeter-wave-over-Fiber (MoF) communication systems [2-4] are considered as one of the most suitable candidates to meet such demand. The last mile of such systems consists of numerous remote antenna units (RAUs) [1], in which high-power/speed integrated photodiodes, lasers, and modulators, serve as key components [5]. The use of heterogeneous silicon-III/V technology to integrate all the essential optical-to-electrical (O-E)/electrical-to-optical (E-O) components on one chip is an effective way to further reduce the size, cost, and energy consumption of RAUs.

The Ge-on-SOI waveguide PD is one attractive solution for the receiver-end in Si-photonic integration [6,7]. High speed with high internal responsivity (~ 0.8 A/W) performance has been demonstrated at $1.55 \mu\text{m}$ wavelength. However, as compared to the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ based photo-absorption layer, the Ge absorption layer usually exhibits a much smaller absorption constant when the incident wavelength is longer than $1.53 \mu\text{m}$ [8], which limits the application of Ge-on-SOI PD in L- and U-bands (1565-1675 nm). Heterogeneously integrated InP based uni-traveling-carrier (UTC)-PD with SOI substrate has thus been demonstrated with excellent performance in terms of speed, responsivity, and saturation power at 40 GHz operating frequency [9]. In this study, we demonstrate a novel heterogeneously integrated InP based evanescently-coupled p-i-n photodiode on silicon-on-insulator (SOI) substrate. By use of a thick BCB layer ($\sim 3 \mu\text{m}$) for device planarization, the parasitic capacitance of probe pads and conductive SOI substrate can be greatly minimized, which leads to a transit-time limited 3-dB

optical-to-electrical (O-E) bandwidth as high as 67 GHz. By optimizing the structure of evanescently-coupled (EC) optical waveguide, a reasonable internal responsivity (0.5 A/W) with a wide optical operation window, which covers from 1.52 to $1.6 \mu\text{m}$ wavelengths can be achieved. Furthermore, our designed ECPD structure can uniformly distribute the absorption and avoid the input-end saturation problem. At 70 GHz operating frequency, the measured saturation current of our demonstrated p-i-n PD can be as high as 9 mA. Such a number is close with the reported III-V based p-i-n ECPD (9 vs. 11 mA) at lower operating frequency (40 vs. 70 GHz) [10].

II. DEVICE STRUCTURE AND MEASUREMENT RESULTS

Figure 1 (a) shows the top-view SEM picture of the fabricated PD, where the SOI waveguide is buried below the thick ($\sim 4 \mu\text{m}$) dielectric layers (oxide and BCB) and cannot be seen. Such a thick dielectric layer is used to reduce the parasitic capacitance of the device. Figure 1 (b) shows the conceptual top-view of the buried SOI waveguides in the demonstrated PD, which illustrates the detail size and layouts of buried waveguide with a tapered waveguide width to gradually couple the launched optical power from bottom SOI waveguide to upper III-V active layers. The areas surrounded by red and yellow dash lines, represent the p- and n- contact regions of topmost III-V active PDs, respectively. In addition, the size of fabricated III-V active PD for integration has a $4 \mu\text{m}$ waveguide width and $30 \mu\text{m}$ active device absorption length (red square region). Figure 1 (c) shows the measured dark I-V curve of fabricated device. The heterogeneously integrated PD shows a clear rectifying behavior with a low dark current (10 nA at -2 V bias). Figures 2 (a) and (b) show the conceptual cross-sectional view and simulated distribution of the optical field in the direction of optical wave propagation, respectively. As shown in Figure 2 (a), the III-V active region is mainly composed of a double hetero-structure p-i-n PD structure with a 400 nm intrinsic $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ absorption layer and InP cladding layers.

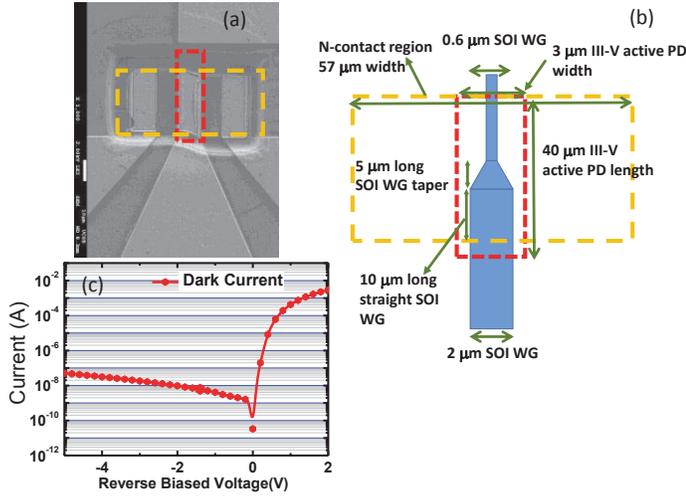


Figure 1. (a) SEM picture of top-view of fabricated PD. (b) Conceptual top-view of buried SOI waveguide in fabricated PD. Red and yellow dash line represent the p- and n- contact regions of topmost III-V active PD, respectively. (c) Measured dark current of fabricated PD.

According to the simulation result, as shown in Figure 2 (b), the launched optical power from the input facet can almost be completely absorbed within 30 μm device absorption length. After de-embedding the 10 dB coupling loss of input facet, the extracted dc internal responsivity is around 0.5 A/W, which shows a broad optical window, which extends to 1600 nm wavelengths, as shown in Figure 2 (c).

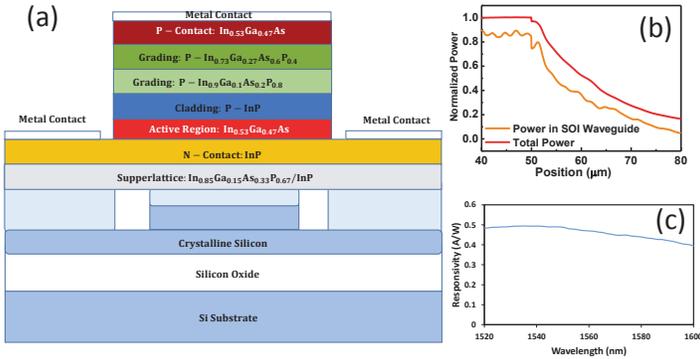


Figure 2. (a) Conceptual cross-sectional view of fabricated PD. (b) The simulated distribution of optical field along the direction of wave propagation. (c) Measured internal responsivity of PD under -3V bias versus optical wavelengths.

Figure 3 and 4 shows the measured bias dependent O-E frequency responses of demonstrated PD under low (1 mA) and high (3 mA) output photocurrent, respectively. From near dc (100 MHz) to 67 GHz, such measurement is realized through the use of a lightwave component analyzer (Agilent, N4373 D). When the measurement frequency is over 67 GHz, we change the setup to a two-laser heterodyne-beating system and measure the photo-generated MMW power by using an E-band (60-90

GHz) power sensor (Keysight, E8486A) and MMW waveguide probe (GGB, Model 90). As shown in Figure 3, under a low output photocurrent (1mA), the measured 3-dB O-E bandwidth under -3 and -5 V is very close as 67 GHz. On the other hand, the measurement result in Figure 4 indicates that when the output photocurrent reaches 3 mA, a high reverse bias voltage as -5V is necessary to minimize the degradation in speed and sustain the same 3-dB O-E bandwidth performance at 67 GHz. This indicates that a higher reverse bias voltage is necessary to compensate the space-charge screening (SCS) effect induced speed degradation, which is usually observed in high-speed PD under high-power operation [11]. In addition, under a low reverse bias as -1 V, a tremendous degradation in speed performance has been observed. This can be attributed to a more pronounced SCS effect and the lack of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ absorption layer depletion under such small reverse bias voltage.

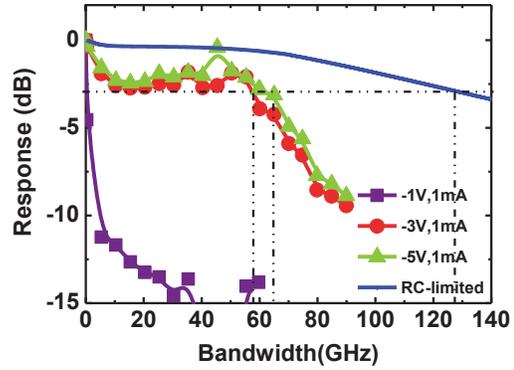


Figure 3. Measured bias dependent O-E frequency response under 1 mA output photocurrent. The solid blue line represents the extracted RC-limited frequency response.

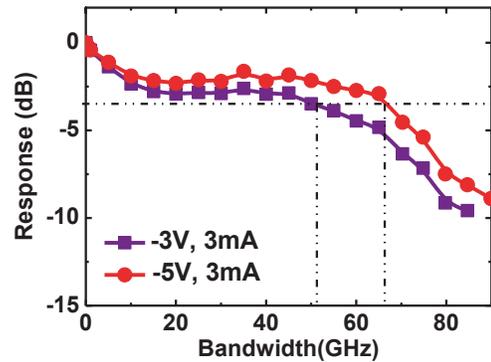


Figure 4. Measured bias dependent O-E frequency response under 3 mA output photocurrent.

The parasitic and junction capacitances usually result in an RC-limited speed performance of high-speed PD on Si platform [9]. Here, we used the equivalent-circuit-modeling technique to investigate whether the internal carrier transit or RC-limited

bandwidth dominates the measured net O-E bandwidth of our device [12]. With such an approach, the RC-limited bandwidth (f_{RC}) can be extracted by the use of the measured scattering parameters of the microwave reflection coefficients (S_{11}) [12] of the PD. Figure 5 (a) shows the adopted equivalent circuit models for the fitting of the S_{11} parameters and the fitted values of each circuit element, except for R_T and C_T , which are shown in the Table inserted into Figure 5 (b). Here, C_J , R_J , and R_C represent the junction capacitance, junction resistance, and differential resistance of the active p-n diode, respectively; C_P represents the parasitic capacitance induced by the interconnected metal lines between the passive probe pads (Co-planar waveguide; CPW) and active diode; R_P and L_P indicate the ohmic loss and inductance of this interconnected lines, respectively. R_g and C_g represent the dielectric loss and capacitance caused by the buried dielectric layer (BCB) below these metal lines, respectively. The parameters for the “PAD simulation” blocks include the parasitic effects for the whole co-planar waveguide (CPW) probe pad, which were calculated by using momentum simulation software (HFSS)¹.

During the device modeling process for the extraction of the extrinsic f_{RC} for the PD chips, two artificial circuit elements (R_T and C_T) are removed, due to the fact that they are used to mimic the low-pass frequency response of the internal carrier transit time [12]. Figure 5 (b) shows the fitted and measured S_{11} parameters as a Smith Chart, while the extracted RC-limited frequency responses are given in Figure 3, as solid blue trace. We can clearly see that the fitted S_{11} trace matches the measured ones well, from nearly dc to 67 GHz (on the Smith Chart). From the extracted RC-limited 3-dB bandwidth at around 130 GHz, we can conclude that the measured net O-E bandwidth (~ 67 GHz) is mainly determined by the internal carrier transit time. By assuming 5.3×10^4 m/s averaged electron/hole drift-velocity in the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ active layer [11] with a 400 nm thickness, the calculated transit-limited bandwidth is around 74 GHz, which is close to the measured bandwidth (~ 67 GHz).

Figure 6 shows the photo-generated MMW power versus output photocurrent obtained with our PD under sinusoidal signal excitation at the 70 GHz operating frequency. The output power was measured by an E-band power sensor (Keysight, E8486A) and the value of the power shown here has been carefully de-embedded, taking into account an insertion loss of around 1.12 dB for E-band WR-12 waveguide probe. As can be seen under -5 V bias, the maximum saturation current can reach 9 mA. Such number is close with that of the reported high-performance III-V based p-i-n ECPD (9 vs. 11 mA), which has a smaller 3-dB O-E bandwidth (48 vs. 67 GHz) [10]. Besides, as specified in this figure, there is an approximately 11 dB difference in power between the ideal (100% optical modulation depth) and measured traces. Such a discrepancy can be attributed to that the 5-dB high-frequency roll-off of the

device itself at 70 GHz operation, as shown in Figure 3, and the around 50% optical modulation depth in our optical system during power measurement, which corresponds to the other 6 dB loss of power.

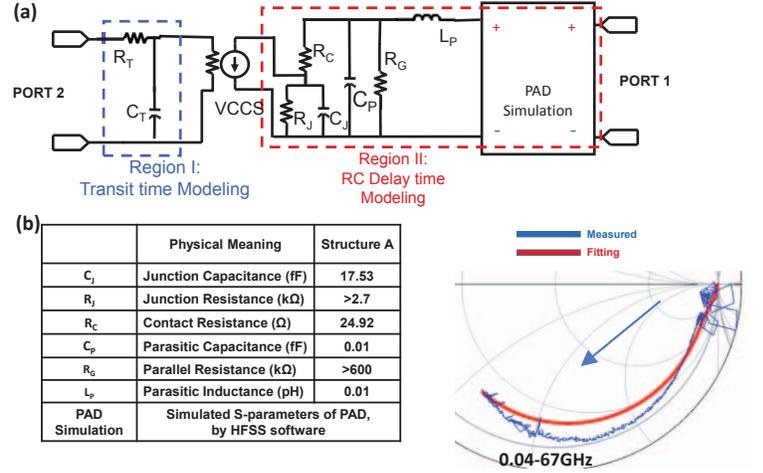


Figure 5. (a) Equivalent-circuit-model. VCCS: voltage controlled current source. (b) Measured (blue line) and fitted (red line) S_{11} parameters from near dc (100 MHz) to 67 GHz under a fixed dc bias (-3 V). The head of the blue arrow indicates the increase in the sweep frequency. The inserted table shows the values of the circuit elements used in the modeling process.

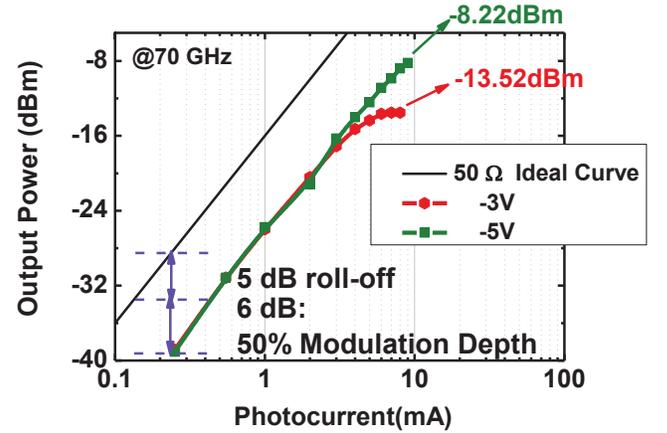


Figure 6. The measured photo-generated MMW power versus photocurrent under sinusoidal signal excitation and different reverse bias voltages (-3 and -5 V) at an operating frequency of 70 GHz. The solid line shows the ideal trace for a 100% modulation depth and 50 Ω load.

III. CONCLUSIONS

A heterogeneously integrated III-V p-i-n PD with SOI substrate has been demonstrated. By use of ECPD structure and thick BCB layer for planarization, such a device can achieve 3-dB O-E bandwidth as wide as 67 GHz, a wide optical operation window (1520 to 1600 nm) with a reasonable internal responsivity (~ 0.5 A/W), and a high saturation current (9 mA)

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at 70 GHz operating frequency. Such device can serve as the key component in photonic integrated circuits for the applications of MMW-over-fiber (MoF) systems. This research was supported by Keysight Technologies.

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