Compact Modeling for Silicon Photonic Heterogeneously Integrated Circuits

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***Abstract*—Photonic-integrated circuits fabricated on a heterogeneously integrated silicon platform have demonstrated record levels of integration and communication capacity. As photonic-integrated circuits become larger and more complex, designing and analyzing them demand modeling and simulation methodologies employed in matured electronic design automation. In this paper, the development of compact models for the building blocks of a fabricated optical network-on-a-chip is introduced. These models are implemented in both SPICE-compatible electronics design automation tools and dedicated photonic-circuit simulators. Model validation is conducted at both device and link levels, allowing the circuit designer to study the impact of individual device design on the overall link performance, paving the path for model-based design optimization of photonic-integrated circuits.**

***Index Terms*—Electronic and photonic design automation, network-on-a-chip, photonics integrated circuit, silicon photonics.**

I. Introduction

THE ever-increasing demand for bandwidth in telecommunications is driving the replacement of electronic data transmission with optical data transmission in networks and links exceeding 10-m lengths [1]. Over the last decade, tremendous advances in photonic integration technology have enabled broad development of optical links based on photonic integrated circuits (PICs) for short-reach datacom [2], [3]. Analogous to electronics, the integration density of PICs is growing exponentially over time, with its trend described as a photonic "Moore's Law" [4]. The fast growing complexity of PICs drives the need for photonic design automation tools [5]. A number of system and link level studies for optical interconnects have been reported [6]–[10]. However, due to the analog nature of photonics, it is imperative to perform accurate circuit-level (or equivalently SPICE-level) modeling and simulation of nanophotonic interconnects. Circuit-level compact models of a variety of photonic devices have been reported, e.g., carrier-injection [11], [12] and carrier-depletion [13] based silicon (Si) microring modulators, Mach-Zehnder modulators [14], vertical cavity surface emitting lasers (VCSELs) [15], etc. However, there is a lack of effort for integrating such models to enable simulation, validation, and optimization of a full optical link.

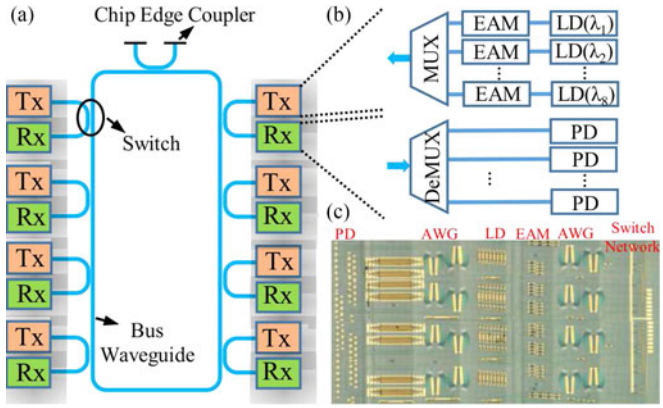

Fig. 1. (a) The ONoC architecture. (b) Enlargements of a transmitter (Tx) and a receiver (Rx). (c) Micrograph of the fabricated ONoC including 8 transceiver nodes.

In this work, an optical network-on-chip (ONoC) fabricated on a heterogeneous Si platform is studied [16], [17]. This technology enables low power consumption as well as integration of many lasers per chip [18]. The ONoC, illustrated in Fig. 1, consists of eight wavelength division multiplexing (WDM) transceiver nodes connected by a reconfigurable ring-bus network, with eight high speed transceiver channels in each node. Within one WDM node, on the transmitter end, there are eight single-mode distributed feedback (DFB) lasers, eight high-speed electroabsorption modulators (EAM) and eight monitoring photodetectors (MPD), one for each channel. On the receiver end, there are eight InGaAs/Si PIN photodetectors (PDs), one for each channel. Some of the receivers use semiconductor optical amplifiers (SOAs). Arrayed waveguide gratings (AWGs) are used for signal (de)multiplexing (Mux/DeMux) at the transmitter and receiver ends.

Although each optical link works at different wavelengths, the building blocks share similar designs. Among them, EAM and PD are broadband, while the lasing wavelength of DFB laser can be effectively tuned. Because the crosstalk between channels is below −25 dB, provided by the AWG, the characterization of a

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single wavelength optical link can be used to evaluate the overall network performance.

An accurate circuit-level model is developed for every type of photonic device in the ONoC. These models are expressed in formats that can be handled directly by traditional electronics design automation (EDA) tools (*e.g.,* Cadence Virtuoso [19]) as well as dedicated photonics simulators (*e.g.,* Lumerical INTERCONNECT [20] and Synopsys OptSim [21]). The photonic device models are validated in several aspects by experimental data from test structures on the same chip as the ONoC. Using these models, a full optical link is simulated in the mentioned software tools. The results are verified by link measurement data. Such a simulation approach enables electro-optical co-design and optimization of the PICs with electronic interface circuits, which have been separately designed in the past. Additionally, the enrichment of the photonic device library paves the way towards a process design kit (PDK) for our heterogeneously integrated Si photonics platform. The methodology employed in this work allows an EDA-style design process for PICs and electro-optical systems. In Section II, compact modeling, parameter extraction, and validation of each device are presented. Our compact model library is discussed in Section III for simulation and analysis of the ONoC. Conclusions and prospectives are drawn in Section IV.

II. Device Characterization and Model Implementation

A. Distributed Feedback Laser

An on-chip laser operating with single wavelength and high wall plug efficiency is crucial for a cost efficient WDM system [1]. The heterogeneously integrated III-V on Si platform has been shown to offer several on-chip single frequency laser solutions with progressively lower threshold and higher direct modulation bandwidth [22]–[24]. The DFB laser design implemented in the ONoC is similar to the one reported in [24].

The carrier and photon density of a diode laser, in both continuous-wave or directly-modulated operation, are governed by the coupled rate equations [25], [26]:

$$\frac{\partial N}{\partial t} = \frac{\eta_i I}{qV} - (BN^2 + CN^3) - g v_g N_p \tag{1a}$$

$$\frac{\partial N_p}{\partial t} = \Gamma g v_g N_p - \Gamma \beta_{\rm sp} B N^2 - \frac{N_p}{\tau_p}\,, \tag{1b}$$

where $g = g_{0\rm N}\ln(N/N_{\rm tr})$. The DC electrical characteristics follow the Shockley diode equation:

$$I = I_0 \exp\frac{q(V - IR)}{nkT}\,. \tag{2}$$

A list of laser parameters is shown in Table I. The numerical values are extracted from various sources including laser design parameters, material gain experiments and laser LIV tests. Fig. 2 shows the light-current (LI) and current-voltage (IV) curves of an on-chip DFB laser with a 400-μm long cavity, 26-μm mesa width, and 1-μm Si waveguide. This laser model, described by (1a), (1b), and (2), is expressed in Verilog-A. Expressing them in a standard hardware description language for traditional EDA tool allows co-simulation of active photonics devices jointly with their driving circuitry. The same set of laser parameters are also passed as inputs to the built-in laser models in specialized photonic circuit simulators such as Lumerical INTERCONNECT and Synopsys OptSim. Having device models in the photonic circuit simulators helps to accommodate the need for an accurate description of both active and passive components in an optical link. The simulated directly modulated laser (DML) eye diagrams matches the measured eyes in terms of modulation depth as well as overall eye shapes (Fig. 3). The agreement across different platforms supports the conclusion that the laser parameter extraction techniques are robust since the laser rate equation model is implemented differently in each software. Equipped with these laser parameters, circuit designers can accurately simulate the static and dynamic behaviors of these DFB lasers.

TABLE I
DFB Laser Parameter List

Parameter	Symbol	Value	Unit
Current injection efficiency	$\eta_{\rm i}$	0.5	
Electron charge	q	1.6×10^{-19}	C
Active region volume	V	3.36×10^{-11}	$\rm cm^3$
Radiative recombination factor	B	4.29×10^{-10}	$\rm cm^3/s$
Auger recombination factor	C	3.5×10^{-30}	$\rm cm^6/s$
Gain coefficient	$g_{0\rm N}$	1960	$\rm cm^{-1}$
Transparent carrier density	$N_{\rm tr}$	1.08×10^{18}	$\rm cm^{-3}$
Group velocity	$v_{\rm g}$	7.5×10^9	cm/s
Active region confinement factor	Γ	0.056	
Spontaneous emission factor	$\beta_{\rm sp}$	1×10^{-4}	
Photon lifetime	$\tau_{\rm p}$	4.98×10^{-12}	s
Reverse saturation current	I_0	8.05×10^{-11}	A
Series resistance	R	5.77	Ω
Ideality factor	n	2	

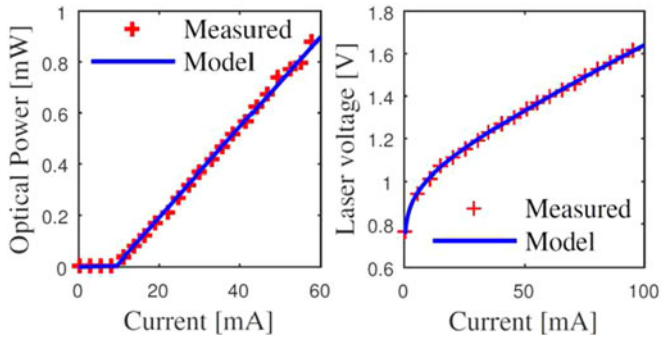

Fig. 2. Measured and simulated LI and IV curves of the DFB laser (light output is from one facet).

B. Electro-Absorption Modulator

A lumped EAM, relying on a strong quantum-confined stark effect (QCSE), has the advantages of small footprint and low energy consumption compared to traveling wave EAMs as well as Mach-Zehnder modulators (MZMs). Lumped EAM design on the heterogeneous Si platform has demonstrated significant

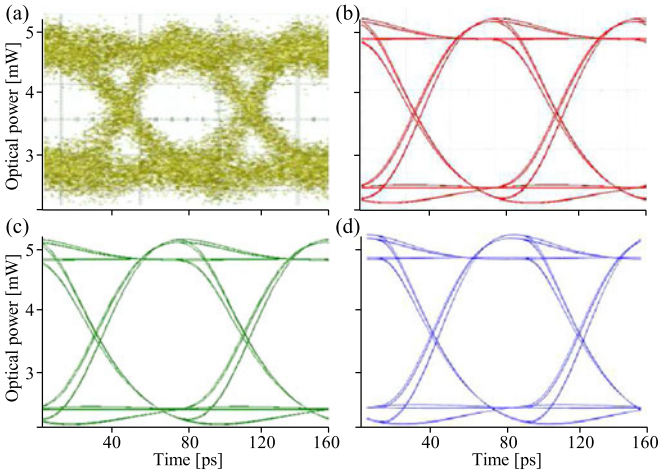

Fig. 3. The eye diagrams of the 12.5 Gbps directly modulated DFB laser [24]. (a) Measurement. (b) Simulation in Cadence Virtuoso. (c) Simulation in Synopsys OptSim. (d) Simulation in Lumerical INTERCONNECT. The modulation depth is 3 dB in all four eye diagrams. In both the experiment and simulation setups, the laser is biased at 2.14 V and driven by a pseudorandom binary sequence (PRBS) signal with 0.75 Vpp. Higher speed were required, so direct modulation was not used in this ONoC. The eyes share the same axes.

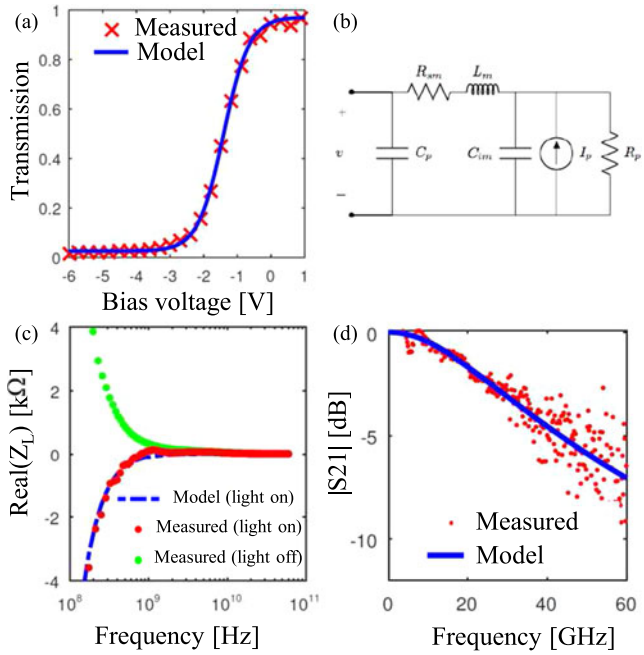

Fig. 4. (a) EAM transmission characteristics plotted as a function of bias voltage. (b) Quasi static circuit model for EAM. (c) The real part of the EAM load impedance as function of modulation frequency. (d) S_{21} (EO) response of EAM.

improvement in modulation bandwidth from 10 GHz to 30 GHz [27], [28]. The 3-dB bandwidth of the integrated DFB-EAM transmitters on Si fabricated by quantum well intermixing has achieved 2 GHz [23]. Due to separate optimization of active regions, the transmitter end of our PIC can operate at a much higher speed. The EAM design implemented here is similar to the one described in [28]. The device is 100-μm long and has 12 quantum wells centered at 1485 nm [16].

For DC optical transmission characteristics of the EAM, the dependence on bias voltage can be described by a logistic equation:

$$T_{\rm opt}(V_j) = \mathrm{L}\left(\frac{1-b}{1+\exp(-k(V_j-V_0))}+b\right), \qquad (3)$$

where V_j is the voltage on the PIN junction; L is the insertion loss; V_0 is the transition voltage; b is the residual optical transmission at a large bias voltage. Fig. 4(a) shows a close fit between measurements and the proposed model. Similar curves are observed from 1550 nm to 1580 nm, reflecting a wide optical bandwidth. By applying a bias around V_0 and a modulation driving signal, the EAM can perform on-off keying (OOK) modulation of the optical signal. The EAM in our PIC achieves a bias voltage lower than 2 V. This is more energy efficient than previously reported bias voltage of 3.5 V in [28].

The electrical characteristics of the EAM can be described by the equivalent quasi-static circuit model as shown in Fig. 4(b), where C_p is the parasitic capacitance introduced from the metal pads, $R_{\rm sm}$ the device series resistance, L_m the device series inductance, $C_{\rm im}$ the junction capacitance, V_j the junction voltage that determines the optical absorption and transmission in (3), I_p the photocurrent generated by the absorbed optical power and fed back into the electrical circuit, and $R_p = dV_j/dI_p$ the equivalent resistance of the photocurrent source [29], [30]. The circuit parameters can be extracted from static and high-speed measurements under different bias conditions. A lightwave component analyzer (LCA) is used for collecting the high-speed scattering parameters. The extracted values of a 150-μm long device are shown in Table II.

TABLE II
EAM PARAMETER LIST

Symbol	Extraction Source	Absolute Value	Unit
L	Transmission-voltage relationship at DC	30	dB
b	Transmission-voltage relationship at DC	2.54×10^{-2}	
k	Transmission-voltage relationship at DC	2.63	V^{-1}
V_0	Transmission-voltage relationship at DC	-1.41	V
$C_{\rm p}$	Metal pad test structure	15	fF
$R_{\rm sm}$	$Z_{\rm L}$ at high frequency under forward bias	17	Ω
$L_{\rm m}$	$Z_{\rm L}$ at high frequency under forward bias	21	pH
$C_{\rm im}$	$Z_{\rm L}$ at high frequency under reverse bias	71	fF
$R_{\rm p}$	Slope of IV curve under reverse bias	27.5	kΩ

The AC current in the junction is composed of the displacement current, related to the junction capacitance $C_{\rm im}$ and the

AC photocurrent, generated from optical absorption [30]. At very low modulation frequency and under high optical power, the EAM behaves principally as a PD, which sources current. Such behavior manifests as a negative real impedance. At a higher frequency ($1/\omega C_m \ll R_p$), almost all the AC current passes through the junction capacitance $C_{\rm im}$, making the EAM appear as a voltage-controlled device whose impedance has a positive real component. The EAM impedance as a function of frequency is shown in Fig. 4(c).

Since displacement current dominates the AC current at moderately high frequency, the transit time effect, which only affects the AC photocurrent, will have little impact on the microwave property of the EAM. As a result, the EAM performance is mainly RC-limited and the extracted electrical parameters can be used to predict the electro-optical response (S_{21}) of the EAM, as shown in Fig. 4(d). The 3-dB modulation bandwidth of this EAM is estimated to be 30 GHz.

The EAM compact model is constructed by implementing both the equivalent circuit and the optical transmission characteristics. When a modulating voltage is applied to the EAM, it is first filtered by the circuit network. The resulting voltage across the junction is then used in (3) to calculate the optical transmission $T_{\rm opt}(V_j)$. The validity of this model is supported by the close agreement between the measured and modeled curves in Fig. 4.

C. Waveguide

Single mode Si waveguides are used throughout the PIC to guide the light. The following equation is used to model the loss along the waveguide with a length L:

$$P_{\rm out} = P_{\rm in}\, e^{-\alpha L}\,, \tag{4}$$

where α is the waveguide propagation loss coefficient, which is estimated to be ~1 dB/cm in this work.

D. Arrayed Waveguide Grating

In this WDM system, (de)multiplexing light from multiple channels is accomplished with AWGs. These devices rely on an array of spatially seperated waveguides to disperse or combine different spectral channels [31]. The modeled spectrum of an AWG is shown in Fig. 5(a), where different colors represent each of the channel. The shapes of the transmission spectra indicate that each channel of the AWG functions as an optical bandpass filter. Consequently, the AWG will reduce the amplitude of the high speed optical signal due to this spectral filtering effect [32]. To illustrate this, the optical spectrum of a commercial band pass filter is plotted in Fig. 6(a), where f_c is the central carrier frequency and f_m is the modulation frequency. When the optical carrier is modulated by a sine-wave, two sidebands located at $f_c \pm f_m$ appear. The sidebands will be suppressed due to the band pass filter of the transmission spectrum. The small signal optical-to-optical (O-O) response of the filter can be calculated as $T(f_c + f_m)/T(f_c)$, where $T(f)$ is the optical power transmission at frequency f. In Fig. 6(b), the calculated frequency response is shown using this approach, which agrees well with the frequency response data obtained with an LCA.

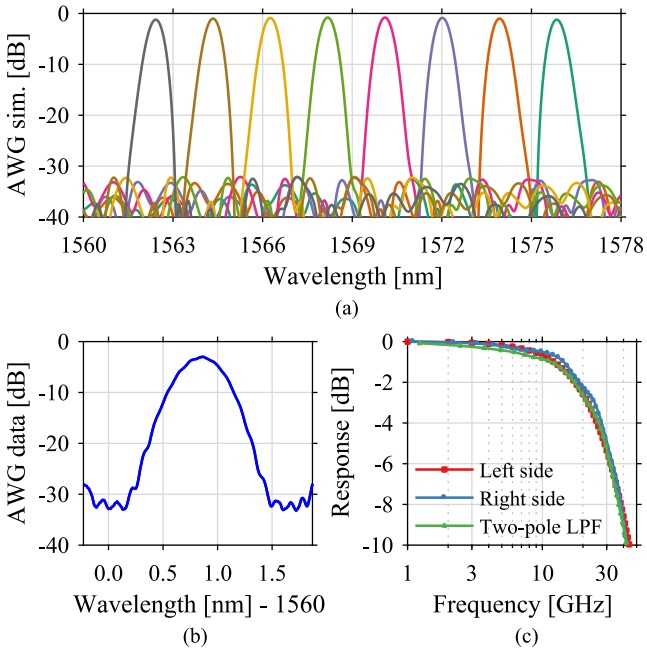

Fig. 5. (a) Theoretical optical spectrum of an AWG. (b) Measured single channel optical spectrum of an AWG. (c) The calculated frequency response using the AWG optical spectrum, with an approximation by a low pass filter (green line).

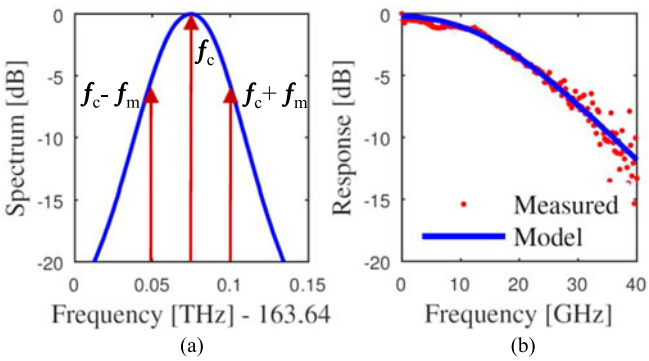

Fig. 6. (a) Measured optical spectrum of a commercial bandpass filter (BPF); (b) Measured and calculated small signal responses of the BPF.

In this experiment, the small signal response of the AWGs cannot be reliable measured by the LCA due to the large fiber-chip coupling loss (~8 dB per facet). The O-O response is therefore extracted using an optical spectrum analyzer (OSA) which offers better sensitivity with no bandwidth limitation [33]. Because each measured AWG channel spectrum is slightly asymmetric as shown in Fig. 5(b), the average of both sides is used to calculate the small signal response. The AWG small signal response is well approximated by a two-pole low pass filter (LPF)

$$H(f) = \frac{1}{(1 + i\, f/f_{\rm LPF})^2}\,, \tag{5}$$

up to 45 GHz as shown in Fig. 5(c). Based on (5), the AWG dynamic model is implemented in Verilog-A using integral operators. During experiment, a transceiver channel is characterized

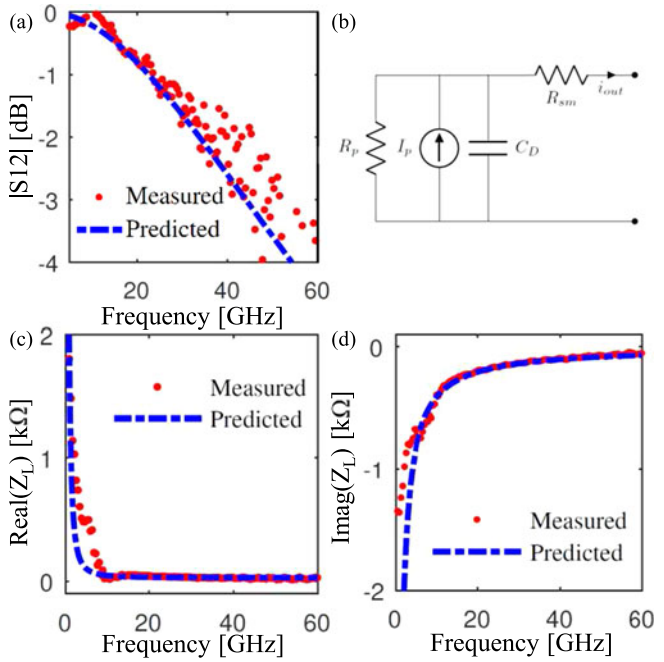

Fig. 7. (a) Magnitude of PD S_{12} (OE) response as a function of frequency. (b) Quasi static circuit model for PD. (c)(d) The real and imaginary part of the PD load impedance as functions of frequency. For this PD, $R_p = 10\,\mathrm{k}\Omega$, $C_D = 38\,\mathrm{fF}$, $R_{\mathrm{sm}} = 30\,\Omega$.

without activating other channels. To match the experimental setup, the AWG channel crosstalk is not included in the Verilog-A model. A more complete AWG model [34] implemented as a scattering matrix in photonics simulator will be adopted in future work to account for channel crosstalk as well as phase and amplitude errors.

E. PIN Photodetector

Waveguide photodiodes can achieve simultaneously high quantum efficiency and high speed [35]. On the heterogeneously integrated platform, PDs have seen a steady improvement in performance [36]. PIN type InGaAs PDs are designed and fabricated as receivers in our PIC. Responsivity (R_{sp}) over 1.1 A/W is observed among PD test structures. The electrical characteristics of the PD can be modeled by the quasi-static equivalent circuit illustrated in Fig. 7(b). The current source represents the photocurrent ($I_p = R_{\mathrm{sp}} P_O + I_{\mathrm{dark}}$) generated by the input optical power P_O and the dark current I_{dark}. Under reverse bias, the diode has a capacitance C_D and series resistance R_{sm}. The circuit is similar to that of the EAM. For this reason, the circuit parameters are extracted in the same way as for the EAM. Unlike the EAM, the AC photocurrent in the PD is the only source for both displacement current and output signal, so the PD bandwidth is subject to the transit time limitation [30]. However, the transit time limit for our waveguide photodiode with a 400-nm thick intrinsic region is above 75 GHz [35]. As a result, the bandwidth of the PD is RC-limited. The PD compact model is constructed by implementing the equivalent electric circuit as well as the light-current relationship. The accuracy of the model is again verified by the close agreement between the measured and calculated load impedance and S_{12} responses shown in Fig. 7.

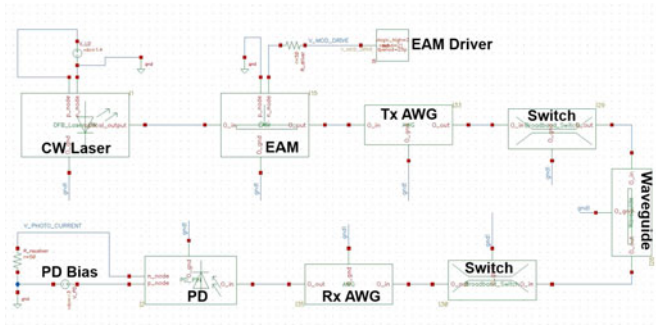

Fig. 8. Schematic view of the transceiver link in Virtuoso. The 50 Ω resistors in the EAM driver and after PD represent the internal resistance of the pattern generator and the oscilloscope.

III. Simulation and Analysis

Based on the individually validated device models above, the overall transceiver link performance can be simulated. The speed and energy consumption of the transceiver link will be evaluated. Also, two cases of using our models and simulation framework for design space exploration are presented, namely, optimizing PD design and EAM driving voltage to demonstrate the application and capability of our models.

A. Full Link Simulation and Analysis

An end-to-end single channel transceiver link is simulated based on our compact device models. Fig. 8 demonstrates the schematic view in Virtuoso environment, which follows the measurement setup. The EAM is driven by a random bit sequence source swinging between -1 V and -2 V. The PD is biased at -3 V. The broadband switches have a wavelength operation range from 1550 nm to 1570 nm (2.5 THz). For this reason, an insertion loss is introduced for the switch without imposing any bandwidth limitation on the link.

First, the dynamic performance of the full transceiver link is studied. The frequency response of the link can be obtained by multiplying the individual frequency responses of the bandwidth limiting components, namely the EAM, the PD and the AWGs. In Fig. 9, the simulated frequency response reasonably captures the link behavior indicated by the measurement data. Next, transient simulations are performed to obtain the eye diagrams of the received signal. In the experiment reported in [16], the data transmission test was applied with a 40 Gbps pattern generator and $2^7 - 1$ bits PRBS signal, which is reproduced in our simulation setup. The simulated eye diagram in Fig. 10(c) is in reasonable agreements with the measurement, shown in Fig. 10(a). The quantified eye characteristics are summarized in Table III. The discrepancies between the simulated eye and the measured eye can be explained by the additional noise introduced by the electronic components in the measurement setup. These electronic components such as function generator, transimpedance amplifier as well as coaxial cables and connectors are not included in the simulation.

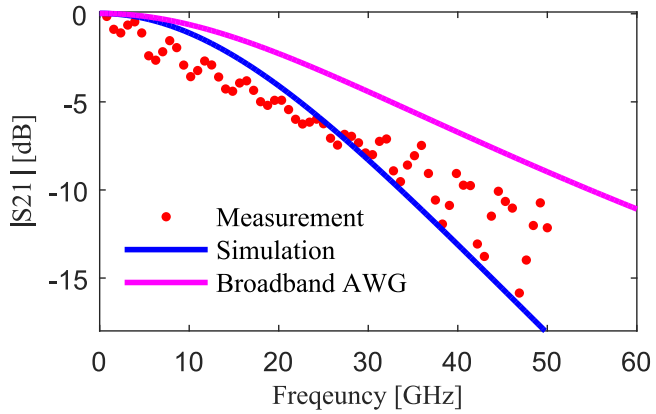

Fig. 9. Simulated and measured frequency responses of the single channel transceiver link. The pink line represents the predicted frequency response of the transceiver link integrated with broadband AWGs.

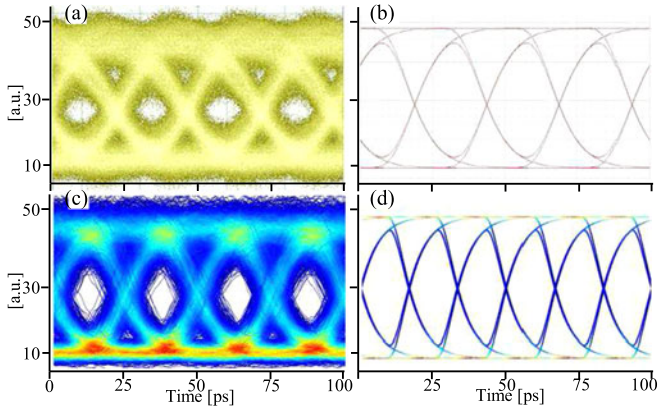

Fig. 10. (a) Measured eye diagram of the single transceiver link at 40 Gbps. (b) Noise-free full link eye diagram from Cadence Virtuoso simulation at 40 Gbps. (c) Full link eye diagram from Lumerical INTERCONNECT at 40 Gbps. The power spectral density (PSD) of the noise source at the laser and modulator are set to 1×10^{-17} W/Hz. The PD thermal noise variance is 3.328×10^{-22} A^2/Hz. (d) Simulated noise-free transceiver link eye diagram at 60 Gbps in INTERCONNECT with the AWGs removed. The software-calculated extinction ratio is the same as the noise-free eye diagram with AWGs at 40 Gbps.

TABLE III
EYE DIAGRAM CHARACTERISTICS

Data source	Eye width (ps)	Rise time (ps)	Fall time (ps)
Measurement in Fig. 10(a)	∼10	∼11	∼11.5
Simulation in Fig. 10(c)	10.1	10.8	11.2

If the ONoC is integrated with its driver electronics, the nominal resistance can be customized to be smaller than 50 Ω. In this case, the RC-limited bandwidth of EAM and PD will be improved, leaving the AWGs as the major bandwidth-limiting components. For this reason, the impact of the spectral filtering effect, introduced by the AWG transmission spectrum, on the overall speed of the transceiver link needs to be investigated. This is accomplished by removing the AWGs from the transceiver link in the simulation. The data rate is then gradually increased so that the software-calculated extinction ratio is the same as in a simulated full transceiver link. The extinction ratio is chosen as the figure of merit because it directly reflects the eye openness. Based on this procedure, the transceiver having sufficiently broadband AWGs is predicted to have the same eye openness at 60 Gbps, shown in Fig. 10(d), as the simulated eye with AWGs at 40 Gbps, shown in Fig. 10(b). Such improvement in the AWG performance will scale the transmission capability of the ONoC up to 3.84 Tbps.

TABLE IV
PD DESIGN SPACE AND SIMULATED OMA

PD #	Width (μm)	Length (μm)	Resp. (A/W)	Cap. (fF)	Res. (Ω)	BW (GHz)	OMA (μA)
1	4	30	0.45	38.9	38.9	46.0	29.3
2	2	50	0.48	38.6	52.0	40.4	30.6
3	2	75	0.56	54.8	36.0	33.8	34.4
4	2	100	0.66	71.5	29.4	28.0	38.3

The energy consumption of the transceiver link is calculated by adding up the power usage of individual active components. DC power is found by calculating the product of the bias voltage and bias current. The DFB laser and PD consume DC power only while the EAM consumes AC as well as DC power. The energy E dissipated in a EAM in one bit cycle is expressed as:

$$E = CV_{\mathrm{PP}}^2/4 + I_{\mathrm{avg}}V_{\mathrm{bias}}/B\,, \tag{6}$$

where C is the junction capacitance; V_{PP} is the peak-to-peak voltage swing; and B is the bit rate. For the EAM, C is ∼70 fF and the voltage swing is 1 V. The first and second summands in (6) correspond to the AC and DC power, respectively. For this EAM modulated at 40 Gbps, the AC power is 18 fJ/bit. The power consumption of the entire transceiver link is 678 fJ/bit, 90% of which is from the on-chip laser. To make the ONoC competitive as an off-chip interconnect, it is necessary to reduce the photonic device energy further to the order of tens of femtojoules per bit [1], [37]. Such a tight power budget for an on-chip transmitter calls for a different type of laser with lower threshold while still being temperature and surface-recombination insensitive when the device is made sufficiently small. Quantum dot lasers grown or bonded on Si have shown promising results in each aspect [38], [39].

B. Design Space Exploration of PD Design

The modeled photonic chip includes a large variety of PD test structures with different device lengths and widths, only a subset of which is used in the fabricated full transceiver links. Table IV shows the key parameters of several PD designs, where the PD #1 is used in the full transceiver link in Section III-A. The bandwidth (BW) is calculated by $(R + 50\,\Omega) \cdot C$, considering a 50-Ω receiver. The optical modulation amplitude (OMA) is calculated by $I_1 - I_0$, where I_1 and I_0 are current for detected 1 and 0 levels of the eye diagrams in link simulation. Device parameters are extracted at −3-V bias.

Due to the nature of the waveguide photodiode design, the responsivity increases while the bandwidth decreases with the device length. From Table IV, the PD #2–4 have a higher

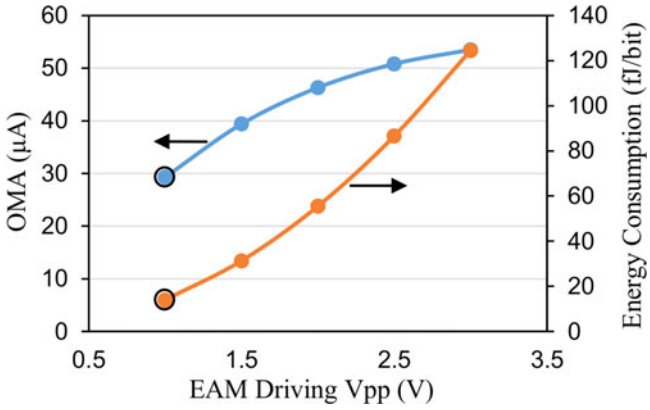

Fig. 11. The OMA and modulation energy consumption with respect to different EAM driving voltage. The black circles indicate the operating points of the EAMs in our ONoC.

responsivity but a lower bandwidth than the PD #1. Therefore, it is possible to replace the PD #1 with each of PD #2–4 to trade bandwidth for responsivity to obtain a higher optical modulation amplitude. Then PD #1 is swapped with each of PD #2–4 in the full link simulation to get the corresponding link eye diagram at 40 Gbps. From these eye diagrams, the OMA values are extracted as shown in the last column in Table IV. The simulation results show that PD #4 leads to the highest OMA mainly because of its high responsivity. A higher OMA will result in a better signal to noise ratio (SNR) and, in turn, a lower bit error rate (BER). This study of PD designs demonstrates that, with these models, the designers can now explore photonic device designs for system optimization.

C. Optimization of the EAM Driving Voltage

In the preceding link simulations, the driving voltage for EAM is set at 1 V_{pp}, which saves energy but compromises the OMA. Such phenomenon can be seen from the EAM transmission versus voltage curve in Fig. 4(a), where 1 V_{pp} swing is not enough to reach the maximum and minimum of optical transmission. The EAM driving voltage swing is then increased, and the eye-diagrams are re-simulated at 40 Gbps. The extracted OMA and modulation energy consumption are plotted in Fig. 11. Other device parameters and driving conditions are the same as those in Section III-A. The simulation results show that the OMA could be enhanced by increasing the EAM driving voltage swing at the cost of consuming greater transmitter power. A higher OMA reduces the requirement for the receiver sensitivity, which in turn reduce the receiver's power consumption [40]. Therefore, with these photonic models and simulation methodology, the transmitter and receiver could be co-optimized for minimizing the overall power consumption while meeting the transmission quality requirement.

IV. Conclusion

Accurate circuit-level models for Si photonic devices are developed based on their electrical and optical properties. These models have been validated in multiple aspects based on the data from fabricated devices. The models are described in standard hardware description language suitable for SPICE compatible simulators as well as in commercial photonic circuit simulators. In both cases, the simulation results of the full optical transceiver link has demonstrated reasonable agreement with the measurements. These simulation results provides insights to the link's overall performance in terms of both speed and energy efficiency. Most importantly, the models assist and guide future PIC design through design space exploration and optimization. Ultimately, this model and simulation methodology enables electro-optical co-simulation, allowing designers to co-optimize photonic devices with electronic circuits seamlessly.

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