

Large-Area Direct Hetero-Epitaxial Growth of 1550-nm InGaAsP Multi-Quantum-Well Structures on Patterned Exact-Oriented (001) Silicon Substrates by Metal Organic Chemical Vapor Deposition

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We employ a simple two-step growth technique to grow large-area 1550-nm laser structures by direct hetero-epitaxy of III–V compounds on patterned exact-oriented (001) silicon (Si) substrates by metal organic chemical vapor deposition. Densely-packed, highly uniform, flat and millimeter-long indium phosphide (InP) nanowires were grown from Si v-grooves separated by silicon dioxide (SiO₂) stripes with various widths and pitches. Following removal of the SiO₂ patterns, the InP nanowires were coalesced and, subsequently, 1550-nm laser structures were grown in a single overgrowth without performing any polishing for planarization. X-ray diffraction, photoluminescence, atomic force microscopy and transmission electron microscopy analyses were used to characterize the epitaxial material. PIN diodes were fabricated and diode-rectifying behavior was observed.

Key words: III-V growth on silicon, MOCVD, InGaAsP, thin films, hetero-epitaxy

INTRODUCTION

Direct hetero-epitaxy of III–V compounds on silicon (Si) is of great interest for the realization of monolithically integrated lasers in silicon photonics. Although flip-chip and wafer-bonding technologies are currently more mature,^{1,2} monolithic solutions are preferred for large-scale manufacturing. The large lattice mismatches between gallium arsenide (GaAs), indium phosphide (InP) and Si ($\varepsilon_{\rm GaAs/Si} = \sim 4\%, \varepsilon_{\rm InP/Si} = \sim 8\%$) and their different polarities and thermal expansion coefficients make the direct growth of GaAs/InP on Si extraordinarily challenging as this can result in a high density of defects from anti-phase boundaries, twins, stacking faults,

threading, and misfit dislocations. These can strongly degrade the quality of the hetero-epitaxy and ultimately limit the performance and reliability of fabricated devices.

Several solutions have been proposed to overcome these issues including thermal cycling,³ growth on off-cut Si (001) substrates,⁴ use of thick and complex buffer layers including InAs, AlAs, GaP, GaAs, InAlAs^{5–7} grown on Ge/Si⁸ and on GaP/Si (001) with an offcut < 0.5° ,⁹ and selective area growth¹⁰ often combined with aspect ratio trapping (ART).^{11–13} Many devices grown by molecular beam epitaxy on templates have already been demonstrated.^{14–16} By contrast, fewer device structures grown by metalorganic chemical vapor deposition (MOCVD) have been reported,^{17,18} particularly those demonstrating emissions at wavelengths of interest for tele- and data-communications (1550 nm and 1310 nm). Growth by MOCVD is desirable for the versatility

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of this technique including the ability for large-scale and high-yield growth of a broad range of materials for photonics and electronics applications.¹⁹

Here, we report on the direct hetero-epitaxy by MOCVD of high-uniformity and large-area 1550-nm PIN MQW and full laser structures on patterned exact-oriented (001) Si substrates. By incorporating an ART technique in a two-step growth process, smooth, highly crystalline, and millimeter-long InP nanowires were realized. Then, after coalescence and active region formation in the second step of the growth process, smooth surfaces were yielded on areas as large as $250 \times 250 \ \mu\text{m}^2$ without the need for any intermittent polishing step.

EXPERIMENTAL

Silicon dioxide (SiO_2) stripes 3 mm long, of different width and pitch size (in the range 200 nm up to 50 μ m) and oriented along the [110] direction were patterned on 4-inch (c. 10-cm) on-axis (001) Si wafers by Deep UV (DUV) lithography. The SiO2 film, 500 nm in thickness, was deposited by plasmaenhanced chemical vapor deposition. Conventional CF₄/CHF₃-based chemistry was utilized to etch the stripes by inductively-coupled plasma etching. The wafers were then diced to 2×2 cm² pieces. Following RCA-1 cleaning, samples were subjected to dilute buffered hydrofluoric (BHF) acid and then etched with dilute potassium hydroxide at 70°C to form v-grooves and expose the {111} surface of the Si substrate. Clean, smooth and straight surfaces along the grooves are desirable for growth quality and to limit the transfer of any imperfections into eventual growth films.²⁰ Immediately prior to loading into the MOCVD system, samples were briefly subjected again to BHF and DI H₂O rinsing and N₂dried.

For oxide desorption, samples were then annealed in the growth chamber in the presence of hydrogen at 825°C and at a pressure of 6.67 kPa for 25 min. Trimethylindium and trimethylgallium, tertiarybutyl arsine and tertiarybutyl phosphine were used as group III and V precursors during the entire growth, Diethylzinc and disilane as *p*- and *n*- dopant sources, respectively. An arsenic (As)-monolayer was deposited on the surface at a temperature of 550°C to facilitate the formation of a thin (~ 30 nm) GaAs)/InP low-temperature (LT) nucleation layer. In this surface reaction-limited regime, the LT layer is meant to accommodate most of the large lattice mismatch between Si and the subsequent III-V layers^{21,22} by producing a thin and conformal layer on Si, with extremely high selectivity ($\sim 100\%$) between Si and SiO₂. The LT GaAs layer was deposited at 410°C and 430°C with a V/III ratio of 6 and 12, respectively, and the LT InP nucleation layer was also deposited at 430°C with a V/III ratio of 628, because a high V/III ratio for InP has been suggested to favor the formation of InP islands at high density, in particular in very narrow trenches,

and consequently a full and uniform coverage of the trenches.²³ Afterwards, the reactor temperature was ramped up to 550° C to deposit a first high-temperature InP layer, followed by another high-temperature InP layer deposited at 600° C with a V/ III ratio of 40 and 89, respectively. The growth pressure was between 46 kPa and50 kPa for all layers.

The second part of this work was focused on the coalescence of such nanowires to allow for device growth and fabrication with planar techniques, similarly to previous reports on ${\rm GaAs}^{24}$ and ${\rm GaN}^{25}$ growth on Si. For that, the SiO₂ stripes were etched with BHF and the sample surface was then cleaned with oxygen plasma. This was followed by a brief exposure to BHF, DI $\mathrm{H}_2\mathrm{O}$ rinsing and N_2 drying immediately prior to loading the sample into the MOCVD system for overgrowth. Following coalescence of the nanowires, we grew PIN multi-quantum-well (MQW) and laser diode structures which consisted of 3- μ m *n*-type doped (~ 2 × 10¹⁸/cm³) InP:Si buffer layer, 400 nm In_{0.75}Ga_{0.25}As_{0.52}P_{0.48} waveguide (wg) layer, a 5-period, 6.5 nm/8 nm $In_{0.74}Ga_{0.26}As_{0.84}P_{0.16}/In_{0.73}Ga_{0.27}As_{0.52}P_{0.48} \quad MQW_{10}$ active region, ~ 1.6- μ m *p*-type doped (~ 2 × 10¹⁸/ cm³) InP:Zn and 100-nm p++ (~ 1 × 10¹⁹/cm³) InGaAs contact layer. Growth conditions and doping concentrations have not yet been optimized. Finally, diode structures were fabricated by standard UV photolithography and chlorine-based etching, 150/10,000 Å Ti/Au were deposited by electron beam evaporation and both used as p- and ncontacts.

RESULTS AND DISCUSSION

The film morphology was characterized by optical microscopy, atomic force microscopy (AFM), transmission electron microscopy (TEM) and scanning electron microscopy (SEM). Densely packed, nearly flawless, flat and millimeter-long InP nanowires of various widths and pitch sizes were observed over a large area, as shown in Fig. 1a and b. Nanowires whose nominal width and pitch size (i.e., trench plus oxide width) were, respectively, 550 nm and 750 nm (Fig. 1c) were noticed to have a better morphology than those having nominal width of 300 nm and pitch size of 400 nm (Fig. 1d). Trench/groove size is known to affect island coalescence, and their optimum ratio is currently under investigation. Generally, for the same growth conditions, narrower trenches lead to longer inter-island distance, making it more difficult to transition from 3D to 2D growth and ultimately leading to a discontinuous and poor morphology of the nanowires.²⁶ InP nanowires having a width of 500 nm and pitch size of 590 nm yielded very smooth top surfaces as indicated by AFM, which revealed a root-meansquare (RMS) roughness of 1.75 nm (Fig. 2a).

These nanowires also demonstrated a good height uniformity as illustrated in the SEM plan view Large-Area Direct Hetero-Epitaxial Growth of 1550-nm InGaAsP Multi-Quantum-Well Structures on Patterned Exact-Oriented (001) Silicon Substrates by Metal Organic Chemical Vapor Deposition



Fig. 1. (Color online) (a) Bright field optical and (b) SEM images of millimeter-long InP nanowires showing good uniformity over a large area, (c, d) SEM plan-view images showing difference in uniformity and smoothness of InP nanowires grown on two different trenches width and pitch size.



Fig. 2. (Color online) (a) AFM scan of InP nanowires, SEM (b) plan-view and (c) cross-section image of InP nanowires. (d) confocal 3D image of InP nanowires showing good uniformity in height over $30 \times 30 \text{ mm}^2$ large area. The small variation in color indicates small height variation.

(Fig. 2b) and in the FIB cross-section (Fig. 2c), and also confirmed by 3D confocal microscope imagining (Fig. 2d). X-ray diffraction spectra were also collected using a Panalytical MRD PRO high-resolution x-ray diffractometer with a Cuka1 (1.5405 Å) source operated at 40 kV voltage and 45 mA



Fig. 3. (Color online) (a) ω/2θ scan centered on InP and showing the InP and Si diffraction peak around (004) Bragg reflections, (b) reciprocal space map map of the PIN MQW structure around (004) Bragg reflections.

current. A triple axis configuration was used to acquire on-axis (004) $\omega/2\theta$ spectra, while a double axis, rocking curve, configuration was used for on-axis (004) omega scans. Figure 3a illustrates a $\omega/2\theta$ scan of the diffraction peak of the InP centered at 31.73°, along with the Si peak at 34.67°. The FWHM of the ω -rocking curve (not shown here) of these InP nanowires is 695 arcsec. This value is in the range of InP nanowires grown on Si²⁷ and SOI.²⁸

Such flat and long InP nanowires are promising for new classes of nano-electronic and photonic devices.²⁸⁻³⁰ However, this comes with difficulties when such nano-devices actually need to be fabricated at a large scale and low cost. Furthermore, growth of quaternary alloys like those used for telecom applications inside these nano-trenches or even directly on top of such narrow nanowires poses additional difficulties in controlling the growth rate, due to the loading effects^{31,32} and the alloys composition, because of the different gas-phase diffusion coefficient, D, and surface reaction rate constant, k_s , of the different precursors. These lead to a different incorporation in particular of In and Ga,³³ and it can result in uncontrollable change in PL emission and QW thickness along both the nanowire length and growth direction.^{27,3}

Thus, the nanowires were allowed to coalesce to achieve a smooth and thick InP "pseudo"-substrate. The thickness of this coalesced layer should be carefully optimized both in terms of material quality and, ultimately, final device performance. If the coalesced InP layer is too thin, although perhaps of high quality, high optical losses are expected due to the mode leaking from the InP active waveguide layer into the high refractive index and thick Si substrate. This behavior is summarized in Fig. 4, which illustrates the desired coupling efficiency dependency on the InP thickness for an input generated TE₀ mode for a laser diode structure fabricated on coalesced InP on Si. Simulations were performed using Lumerical,³⁵ a commercial 3D



Fig. 4. (Color online) Dependency of the coupling efficiency on the InP buffer layer thickness for an input TE₀ mode for a laser diode structure fabricated on coalesced InP on Si. Inset Simulations of TE₀ mode profile when the InP coalesced thickness is (a) 500 nm, (b) 700 nm, (c) 1.2 μ m. (d) Simulation of the TE₀ mode profile of the same structure grown on a native InP substrate.

finite-difference time-domain software tool. The TE₀ mode was first simulated for the InP laser structure on an InP substrate, and this mode was then launched into the InP laser on an InP/Si template. The coupling efficiency defines the amount of light launched that remains in the InP active waveguide layer after propagating over a significant distance. A lower coupling efficiency indicates that the launched mode undesirably couples to substrate modes. For an InP coalesced layer thickness $\geq 1.5 \ \mu m$ thick, a coupling efficiency of > 99% is achieved, which is desirable. The inset in Fig. 4 shows simulation results of the fundamental TE_0 mode profile for a structure with a coalesced InP thickness of (a) 500 nm (b) 700 nm, and (c) $1.2 \ \mu m$. The inset of Fig. 4d shows the simulated TE_0 mode profile for the same structure grown on a native InP substrate for comparison. For the InP

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Fig. 5. (Color online) (a) SEM top-view image of the final surface after regrowth without any intermediate CMP step, (b) bright rield TEM image of the MQW, (c) high-angle annular dark field scanning transmission electron microscopy image of the v-groove patterned on the Si and GaAs/InP seed layer.

coalesced thicknesses of 500 nm and 700 nm, the mode profile clearly shows field energy in the Si substrate. This is an indication that over some propagation distance, all of the optical energy generated in the InP active waveguide layer would couple to substrate modes in the Si. For our devices, we have grown $3-\mu m$ InP before the active layer. Electron channeling contrast imaging measures (not shown here) suggest that this InP "pseudosubstrate" has a threading dislocation density of 3.5×10^8 /cm². Figure 3b reports the reciprocal space map (RSM) around the (004) InP Bragg reflection of a PIN structure grown after InP nanowires coalescence and showing good alignment of the Si, InP, and the compressive strained InGaAsP MQW. The anisotropic elongation of the InP suggests mosaicity, which can be possibly attributed to the formation of defects in the thin low-temperature GaAs and InP layers.

As shown in the SEM image of Fig. 5a, the final regrown surface appears continuous and smooth. The measured RMS roughness was 5.7 nm over a scanned area of $5 \times 5 \ \mu m^2$. This is relatively flat considering that no polishing was utilized, and any planarization was due only to the growth itself. Most of the defects observed are likely due to threading dislocations, possibly not fully halted by the ART technique, in particular those propagating along the (111) direction, parallel to the trench direction.³⁶ The aspect ratio of the trench width to mask thickness was \sim 1, and it has been proposed to have it > 2 for the defects necking effect to work effectively and potentially halt all the threading dislocations arising from the mask openings. Additional defects, including stacking faults, may be introduced during the coalescence of the InP nanowires.³⁸ These are expected to be greatly



Fig. 6. (Color online) Photoluminescence of final laser structure showing 1567 nm emission after regrowth and (inset) of initial InP nanowires.



Fig. 7. (Color online) HV for a 900- μ m-long by 2.5- μ m-wide ridge fabricated on patterned (001) Si after InP nanowires regrow. Inset: SEM-focussed ion beam cross-section of one of the ridges fabricated on patterned (001) Si.

reduced by an optimized trench width and spacing and nanowire height and wedge–shaped surface. A further decrease in defects is expected by further improving the seed layer quality and the SiO₂ mask sidewalls, as these also affect the quality of the exposed (111) Si surface of the v-grooves, which in fact plays an important role in the defects necking.³⁹ A more complete defects generation mechanism and relative reduction study is ongoing.

Figure 5b and c show cross-section TEM images of the MQW region and area near the v-grooves, respectively. The MQW exhibits flat and sharp interfaces, and the density of defects is highest within the v-grooves. Figure 6 shows the results of room-temperature photoluminescence measurements for the MQW structure and for the InP nanowires (inset), the latter measured after only the first growth step. A strong PL emission was observed at $\lambda = 924$ nm, which corresponds to the fundamental InP bandgap, while the center wavelength of the PL emission for the MQW structure is 1567 nm and the FWHM is \sim 160 nm. Finally, the diodes fabricated after InP nanowires regrow have shown good rectifying behavior. Figure 7 illustrates a measurement of a 900- μ m-long by 2.5- μ m-wide ridge having a turn-on voltage of 1.2 V.

Future work will be focused on improving overall material quality and optimization of the fabrication process.

CONCLUSIONS

In conclusion, we have successfully demonstrated direct hetero-epitaxy of 1550-nm laser structures grown on patterned exact-oriented (001) Si substrates by MOCVD. Good uniformity over a large area was achieved by growing on coalesced, millimeter-long InP nanowires which were initially grown from Si v-grooves. Diodes were also fabricated and their measured IV characteristics clearly show diode behavior. These results are significant because they demonstrate the feasibility of monolithically-grown III–V lasers by MOCVD on a well-established (001) Si planar platform which is a key requirement for the integration of the III-V based materials on Si for the next generation of telecom applications.

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