Invited Paper

# Silicon photonic terabit/s network-on-chip for datacenter interconnection

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ABSTRACT

Silicon photonic integration is an enabling technology for power- and cost-effective optical interconnects in exascale performance computers and datacenters which require extremely low power consumption and dense integration for a higher interface bandwidth density. In this paper, we experimentally demonstrate a fully integrated optical transceiver network on a silicon substrate using heterogeneous integration. High performance on-chip lasers, modulators and photodetectors are enabled by transferring III-V materials to a pre-patterned silicon substrate. Wavelength division multiplexed transceivers with eight wavelength channels are monolithically-integrated on a single chip, forming an optical network-on-chip circuit with total transmission capacity up to 8×8×40 Gbps, and bandwidth density over 2 Tbps/cm. We show that the heterogeneous silicon integration provides the design flexibility and scalability for high-speed optical communication systems.

**Keywords**

Heterogeneous silicon integration; Network on chip; Optical interconnection.

## 1. Introduction

The demand of fast, reliable, and low-cost optical data links has led to research in developing the next generation of photonic integrated circuits (PICs) to improve the power efficiency, latency, and capacity. In past decade, the power required for photonic transmission in data centers and supercomputers has been dramatically reduced in energy per bit. The transmitter size per capacity has been reduced by a factor of 10-100, and in the same time the bandwidth capacity has been increased from 10 Gb/s to 400 Gb/s in short links. However, the typical energy consumption of 10-100 pJ/bit to date must shrink further by another 2 to 3 orders of magnitude within the next few years for practical optical interconnection applications [1, 2]. This demand can be achieved with complete integration with a high bandwidth density, low power module, and most importantly a low-cost package technique.

Silicon photonics has shown its great potential for monolithic integration with the well-developed complementary metal–oxide–semiconductor (CMOS) fabrication [3-7]. Benefiting from the low loss of Si and advanced process techniques, a variety of functional components, including low loss waveguides (WGs) [8-9], modulators [10-12] and photodetectors [13-15] have been developed on the silicon-on-insulator (SOI) platform. Monolithic integration of photonic components with the electrical driver and/or other logic circuits were demonstrated on silicon with a standard semiconductor foundry process [16-18]. As an example, reference [18] presented the first single-chip microprocessor with embedded optical interconnection between processor core and memory bank with on-chip modulators, photodetectors and off-chip light source. Such approach requires co-design and co-process of optical and electrical components, and in many cases compromises must be made between the two parts of the system. Therefore, it is better to optimize and fabricate the photonic chips and driver circuits individually, and then integrate both circuits together with 2.5D or 3D architecture in a compact chip package [19, 20]. Advanced signal multiplexing techniques are normally involved in the photonic circuit design to scale up the chip bandwidth. In particular, integrated wavelength division multiplexing (WDM) systems combined with single mode fiber shows great advantages compared with discrete links such as vertical cavity surface emitting laser (VCSEL) links in short distance communication [21-23].

However, the lack of a reliable silicon laser has been the major impediment due to the fundamental material limit of silicon, which has an indirect band-gap. Three approaches have been widely used to achieve an on-chip laser by introducing efficient light emission materials on silicon with three major approaches: (1) hybrid, (2) heteroepitaxy or (3) heterogeneous integration. The hybrid assembly approach couples the laser output from a III-V chip with gain section into the silicon chip laterally [24, 25] or vertically [20, 26]. This approach allows optimization and fabrication of the III-V and silicon chips individually, but it is mainly limited by the complications in light coupling and device packaging, as well as the extra fabrication cost of two separate chip fabrication. Direct epitaxial growth of III-V materials, especially quantum-dot (QDs) gain materials on silicon is a promising solution for high performance lasers with high volume throughput [27-31]. However, the lifetime and reliability of the heteroepitaxial lasers requires further improvement. Moreover, heteroepitaxial growth normally has a thick or dedicated buffer layer to annihilate the propagating dislocations from the heterogeneous interface, which makes it difficult to couple the laser output into the waveguide at the silicon layer. In this paper, we focus on the heterogeneous silicon integration (HSI) approach, which transfers the functional materials to silicon with a wafer bonding technique [32-37]. By using a selective die bonding method, which selectively places a number of small III-V chips to designated zones on a large silicon wafer, the total cost can be dramatically reduced, and multiple functionality can be realized by integrating different epitaxial structures on the single chip [38]. This platform is not limited to the integration of III-V materials, but can be

applied to a wide variety of material systems to integrate nonlinear and nonreciprocal materials for many different applications [39-42].

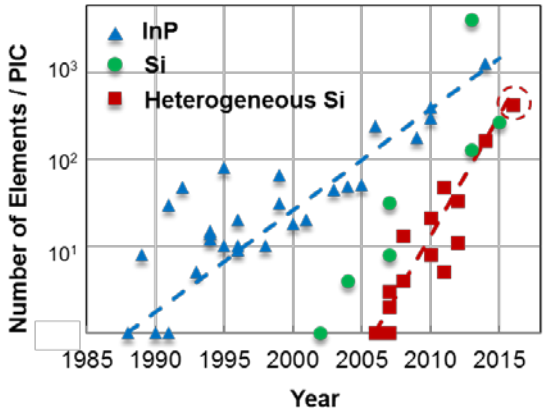


**Fig. 1.** Evolution of photonic integration in terms of number of devices on a single waveguide on chip. Silicon photonic (green circle) represents the "passive" integration without an on-chip laser; InP integration (blue triangle) and heterogeneous silicon integration (red square) have integrated active devices including lasers on-chip. The circled data point indicates the PIC reported in this work.

Fig. 1 shows the evolution of InP- and silicon- based photonic integration platform in terms of number of devices integrated on one chip, representing "Moore's Law" in the photonic integration field. With more and more photonic devices integrated on the single chip, both the complexity and functionalities of the PICs have been greatly improved in past three decades. Silicon photonic integration is catching up with InP-based III-V photonic integration. Benefitting from the compact component footprint and low loss waveguide, over 4000 devices were integrated in the large-scale silicon phase tuning array chip in 2013 [43]. Particularly, with an efficient on-chip laser solution, the HSI platform has been rapidly growing since its invention in 2006. This paper will summarize the design and demonstration of our recent advances on heterogeneous integrated optical network-on-chip (ONoC) circuit [44]. With eight transceiver nodes and over 400 photonic components in a single die, large communication capacity was achieved for the application of high-speed datacom interconnects in high performance computers (HPCs) and data centers. The remainder of this paper is organized as follows: Section 2 shows the architecture of the ring optical network. Section 3 discusses the photonic circuit design and fabrication process. Section 4 and 5 report the characterization of key components and the optical network circuit, respectively. Finally, section 6 summarizes this paper.

## 2. ONoC architecture

The ONoC topology defines the structure of the network and controls how data flows among the transceiver nodes in the network. A number of ONoC topologies have been reported [45-49], such as Corona [45], Firefly [46], ATAC [47], etc., typically designed for a multi-core system with 2-D or 3-D photonic integration. In the case of the Corona network, the WDM clusters are connected to bus waveguide with resonator structures [45]. As a wavelength-selective switch (WSS) component, the microring resonator picks up one channel of the WDM spectrum as either modulator/multiplexer (Mux) or photodetector/demultiplexer (DeMux). However, the bandwidth at each node is limited by the modulation speed and the optical bandwidth of the microrings.

In this paper, to overcome this bandwidth limit, we propose a ring network architecture based on broadband optical switches instead of WSS components. The network architecture has a ring topology with circular and close bus waveguide as the basis infrastructure, as schematically shown in Fig. 2. Multi-nodes of photonic WDM transceivers are attached to the bus through broadband optical routers/switches. The transmitter/receiver nodes have individual electrical/optical (E/O) interface to CMOS driver and the corresponding clusters. Two spare nodes in this chip are present with optical interface for coupling with single mode fibers. The broadband optical routers/switches control all the WDM channels simultaneously to scale up the total bandwidth at each node.

Such ring architecture defines a reconfigurable network that can be controlled by varying the working status of the optical routers, as illustrated in Fig. 3. With a normally-off switch design, the default mode is at self-communication or self-configuration status, where the transmitter is talking to its local receiver for self-testing or initialization (Fig. 3(a)). By fully turning on any two of the switches in the network, all WDM channels at one transmitter or from the off-chip optical interface can be routed to another node simultaneously, as a cluster-to-cluster or point-to-point mode (Fig. 3(b)). It can also work at a broadcasting mode as a 1×N network by partially turning on the switch array (Fig. 3(c)). This reconfigurable network architecture provides flexibility in system designs based on practical applications. It is to note that, all transceiver nodes share identical WDM channels, thus traffic conflicts need to be avoided by carefully controlling the switch array. The data stream can only flow in one direction on the bus waveguide, due to the directionality of the light coupling in the optical switches. There are two ways to scale up the number of clusters in this network: more clusters can be added to one bus loop considering a low insertion loss from the bus waveguide and switch bank; two or more bus loops can be cascaded through the optical input/output (I/O) ports to form a multi-ring architecture.

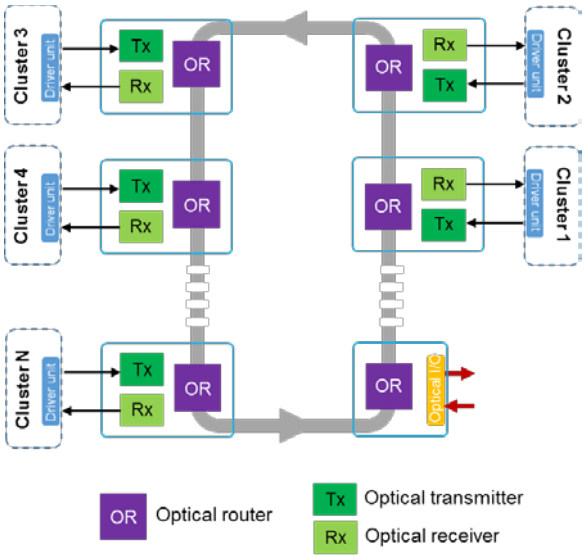


**Fig. 2.** Architecture overview of the ONoC circuit.

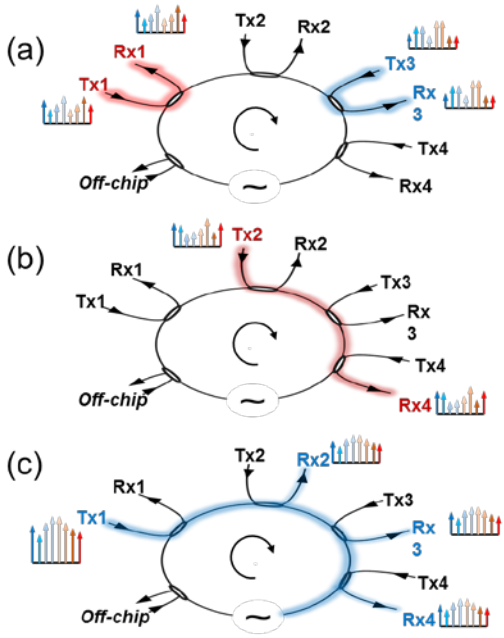


**Fig. 3.** Reconfiguration modes of ring network: (a) self-configuration, (b) cluster to cluster and (c) broadcasting mode.

### 3. Heterogeneous silicon integration

Most of the key elements for an on-off keying (OOK) optical link are available on the heterogeneous silicon integration platform, including low threshold current distributed feedback (DFB) lasers, high-speed Mach-Zehnder modulators and electroabsorption modulators (EAMs), high power semiconductor optical amplifiers (SOAs) and high-speed photodetectors (PDs) [50-55]. Fig. 4(a) schematically shows the layout of the WDM transceiver. The transmitter has 8 wavelength channels in the C/L band with 200 GHz spacing. Each channel has a continuous-wave (CW) DFB lasers as the single-color light source, a high-speed EAM for intensity modulation, and a monitoring PD (MPD) to in-situ monitor the laser output power and to provide feedback control. The corresponding 8-channel receiver has fast PDs (FPDs) with P-I-N structure and InGaAs absorptive layer. Part of the receivers consist of SOAs with same gain materials as the laser to amplify the received optical power and compensate any high optical loss from fiber coupling or transmission in long waveguide. 1×8 silicon array waveguide grating (AWG) are adopted as symmetric Mux/DeMux. The data upstream and downstream are controlled by a Mach-Zehnder interferometer (MZI) switch which covers the broad spectrum over 1.6 THz (8×200 GHz). Fig. 4(b) shows the schematic and cross-sections structure of the heterogeneously integrated devices used in the transceivers. All the device epitaxial layer structures are carefully designed, so that they are compatible with same device fabrication. The DFB/SOA/MPD epi consists of 3 InAlGaAs quantum wells (QWs) with photoluminescence (PL) center wavelength at 1545 nm; the EAM epi has 12 InAlGaAs QWs with PL wavelength at 1485 nm; the FPD epi has 400 nm InGaAs bulk layer as the light absorber.

They share the same contact layers: InP for n-type contact and InGaAs for p type contact, so same contact metallization can be applied with one deposition. The same InP bonding interface with super lattice (SLs) are used for the selective bonding process.

On the other hand, those different types of devices structures are optimized individually. Lasers and SOAs have wide mesas with 4 μm wide current channel defined by $H^+$ implant. Lasers have a 400 μm long cavity and SOAs have 1.5 mm. A short (20 μm) taper is used to couple the light from silicon waveguide to III-V/Si heterogeneous waveguide. EAMs have a narrower mesa defined by dry etch to reduce parasitic capacitance, and a longer taper (60 μm) for low insertion loss. The PDs also have a compact mesa design for low capacitance, but wider mesa and silicon waveguide to improve the responsivity. Instead of heterogeneous tapers, PDs have adiabatic silicon tapers at input and 7° slanted III-V interface to eliminate unnecessary reflections back to the input waveguide.

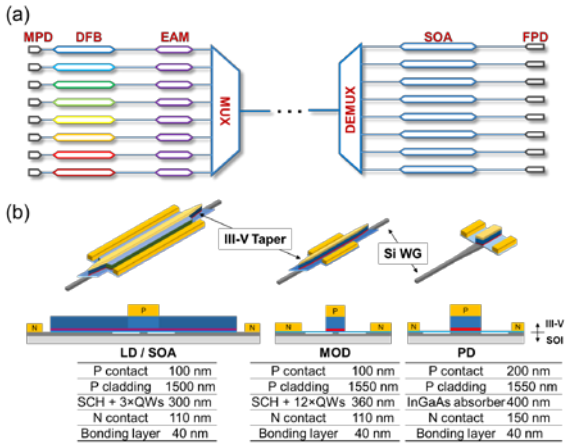


**Fig. 4.** (a) The WDM transceiver architecture in the ONoC circuit, and (b) the device structure, cross-sections and epi stack of the heterogeneous laser /amplifier, modulator, and photodetectors, respectively.

The ONoC circuit fabrication has two major parts: silicon (passive) process and III-V (active) process. The silicon process defines the grating, waveguide, (De)Mux, switch and all other silicon components on the silicon-on-insulator (SOI) substrate with 500 nm thick device layer and 1 μm buried oxide (BOX) layer. As the first step, first-order Bragg grating sections in DFB cavities were defined with a JEOL JBX-6300FS E-beam lithography (EBL) system and etched with a reactive ion etching (RIE) tool. The Bragg grating pitches were finely tuned to control the wavelengths to the eight WDM channels. A quarter-wavelength phase-shifted section was at the center of the laser cavity. Waveguides, including ridge waveguide (partially etched), stripe waveguide (fully etched) as well as outgassing channels (fully etched) were patterned with an ASML 248-nm deep-ultraviolet (DUV) lithographic stepper. Fig. 5 shows the cross-sectional diagram of the SOI substrate after the passive process, and scanning electron microscope (SEM) images of the Bragg gratings on silicon waveguide and directional coupler with ridge waveguide. The etch depth of grating and ridge waveguide are 30 nm and 200 nm, respectively. Multimode (2 μm) ridge waveguides are used between transceiver nodes for low propagation loss, and they adiabatically taper down to single mode (600 nm) waveguide at bending to avoid large leakage.

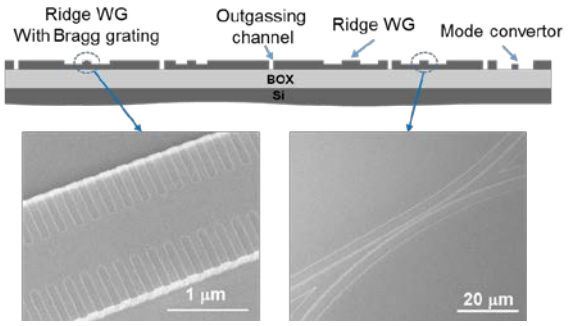


**Fig. 5.** Diagram of SOI substrate after process, and the SEM images of Bragg gratings on silicon ridge WG and directional coupler.

The III-V processes were performed after the selective die bonding, as shown in Fig. 6. After thorough clean and oxygen plasma treatment on both III-V chip and SOI, the bonding process was operated in a Finetech pick-and-place tool with below 10-μm precision. The gap between III-V bonded samples was controlled below 100 μm, and then a thin layer of silicon dioxide was deposited to protect the exposed silicon waveguide inside the gaps. After III-V substrate removal, the mesas of laser/modulator/photodetector were etched with Methane/$H_2$/Ar RIE etch, followed by selective wet-etch to expose the bottom n-InP contact layer. A thick silicon dioxide layer was deposited after n-type metallization. After Ti/Pt heater/tuner and p-type metallization, the sample was implanted with protons to define the 4 μm current channel in the laser and SOAs, as well as to isolate the EAM cavity with the long tapers. Pd/Ti/Pd/Au and Pd/Ge/Pd/Au metal stacks were used as p- and n- type contacts, respectively. The sample was planarized with 3 μm polymer (Benzocyclobutene, or BCB used in this work) before final metallization to further reduce the parasitic capacitance from the substrate.

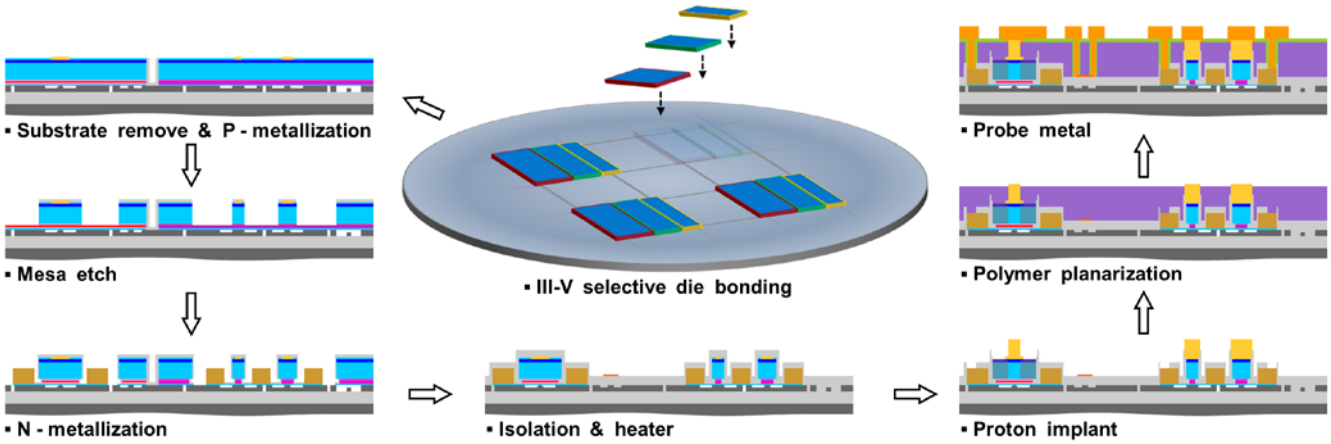


**Fig. 6.** Schematic of selective die bonding on SOI and fabrication steps of III-V/Si after bonding.

Fig. 7(a) shows a microscope image of the photonic chip after III-V bonding. A 100-mm diameter SOI wafer was used due to the tool limit. Three pieces of III-V epi bonded in parallel in each quarter, covering a whole die with about 19×19 $mm^2$. The transceiver circuit locates in the middle of the die, with a size about 11×16 $mm^2$. Fig. 7(b-d) shows SEM images of the heterogeneous laser, photodetector and modulator after mesa etch and metallization. Because of the good resolution of DUV lithography, sharp adiabatic III-V tapers with 300 nm tip width were achieved, which is preferred for low transition loss and low power reflection. Fig. 7(e) shows the opened via on modulator mesa and n-metal after BCB planarization. Over 400 functional photonic components, including both passive and active devices, were interconnected with silicon waveguide into an integrated network system, as shown in the stitching microscope image in Fig. 7(f). The footprint of each transmitter or receiver node is roughly 1×6 $mm^2$, mainly limited by the size of the AWGs. The switch array is located at the right side of the chip, highlighted by the red dash box, with metal pads compatible with a 16-pin probe card. The blue boxes in Fig. 7(f) indicate the bonding positions of III-V epi. After the process the chip was diced into dies with facets polished for fiber coupling and characterization. The process yield of the individual photonic components was evaluated by testing the monitoring devices. The process yield of passive components was 100%, and the overall yield was about 90% counting both active and passive elements. The high yield was benefitting from a series of tolerant device designs, such as wavelength-insensitive and broad band designs; the failed devices was mainly due to process imperfections, such as bonding defects that resulted from the imperfect process environment.

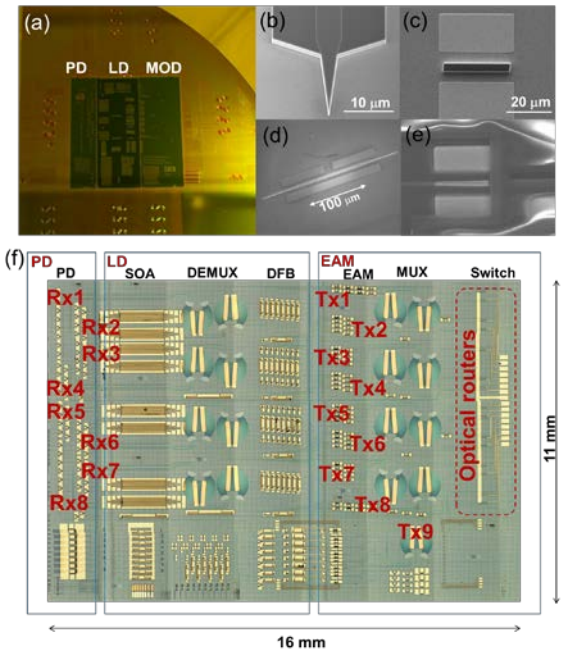


**Fig. 7.** (a) Microscope image of the photonic chip after multiple die bonding and device mesa etch; and SEM images of (b) laser mesa with 20 μm taper; (c) FPD mesa with n-contact metal; (d) EAM after mesa etch with 100 μm cavity and 60 μm tapers; (e) deep via in the thick polymer after surface planarization; (f) microscope image of the photonic transceiver circuit.

## 4. Device design and performance

### 4.1 Broadband optical switch

A broadband optical router and switch is of great interest in an alignment-free optical network or WDM system. Microelectromechanical based optical switches are normally broadband, but their large footprint make it difficult to be integrated on chip [56]; Resonator based switches have small size, but they normally have narrow bandwidth [57,58]. Broadband optical switches are reported with multimode interference coupler or broadband 3-dB couplers based MZI switches [59, 60]. However, they are normally very sensitive to fabrication variations. In this work, we propose a novel adiabatic coupler MZI (ACMZI) switch, which adopts the adiabatic coupler as the 3-dB power combiner/splitter in a MZI structure, so that the switch can work for a wide wavelength range.

In an adiabatic coupler, the two unbalanced arms are brought close gradually to avoid abrupt mode perturbation, and then change the waveguide width slowly enough with a constant gap width. During this transition the fundamental mode on each arm will adiabatically change to an even/odd mode and then optical power is evenly split to two symmetric outputs [61]. In this design, the input ridge waveguide widths are chosen to be 700 nm and 500 nm, while the output waveguide is 600 nm. The coupling gap is 300 nm. Fig. 8 shows the simulated light propagation with fundamental transverse electric (TE) mode at 1550 nm wavelength. It can be seen that an even mode is activated when the light inputs from the wider arm, and odd mode is activated when the light inputs from the narrow arm, both resulting in an even power split.

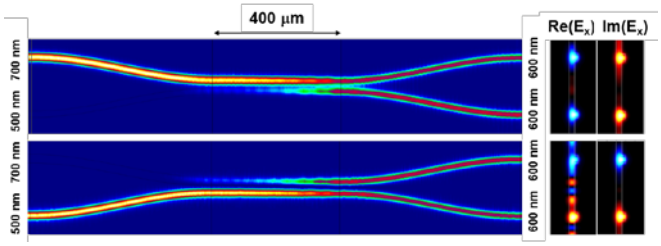


**Fig. 8.** Simulations of light propagation in an adiabatic coupler

Fig. 9(a) shows the structure of the MZI switch with adiabatic couplers [62]. Two 3-dB adiabatic couplers are connected back to back to form a symmetric interferometer structure. A thermal phase tuner on one arm is to change the phase difference between two arms and to control the power split ratio. As introduced in the process section, the ridge waveguide was partially etched with 200 nm ridge height and 300 nm slab thickness. 1 μm $SiO_2$ layer was deposited on the coupler, isolating the silicon waveguide from the top Ti/Pt heater metal. 2 μm wide deep trenches were etched on both sides of the waveguide to improve the thermal efficiency of the phase tuner. The performance of AC-MZI switch is shown in Fig. 9(b). It shows an on-off extinction ratio (ER) larger than 16 dB across over 80 nm wavelength range on both coupling and through ports. Fig. 9(c) shows the tuning response of the AC-MZI switch in time domain under a square wave signal on the phase tuner. It has about 18 ms rise time which corresponds to a 30-kHz bandwidth, which is fundamentally limited by the low efficiency of the indirect thermal tuning through a thick oxide spacer layer.

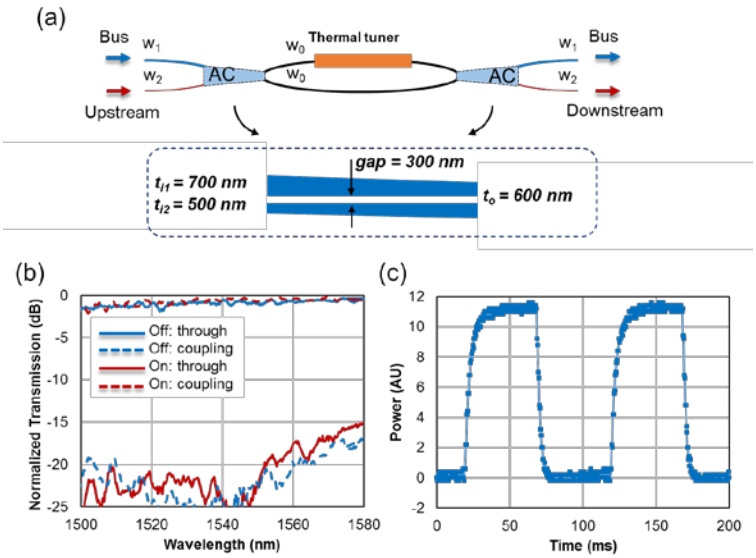


**Fig. 9.** (a) Structure of the AC-MZI switch; (b) normalized transmission of AC-MZI switch at on and off status; and (c) its response to a 10-kHz square wave voltage driving on the phase tuner.

### 4.2 (De)Mux

AWGs are widely used as the (De)Mux in a WDM system due to their dense channel spacing, low cross talk and compatibility to integrated circuits [63-65]. A symmetric AWG design is used in this work, as the SEM images show in Fig. 10(a). It consists of three major parts: I/O waveguides, star-couplers with free propagation region (FPR), and the phase waveguide array. Fig. 10(c) labels the parameters used in this work, with the design values listed in Table 1. The array waveguide width is set to be 1.2 μm, which is slightly multimode, for low loss and low crosstalk [66]. The 1×8 AWG has a footprint about 1.2 $mm^2$. A parabolic taper is used at the I/O waveguide to improve the channel uniformity, as shown in Fig. 10(b) [67]. In order to reduce the total insertion loss of the large component, all the waveguides are partially etched; minimum 200 μm bend radii was used for low leakage loss; the gap between neighboring array waveguides was 200 nm, limited by the lithographic resolution.

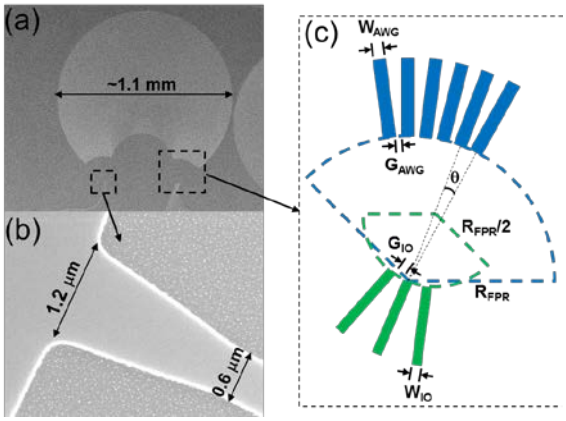


**Fig. 10.** SEM images of the (a)AWG design and (b) the I/O waveguide with parabolic taper; (c) the AWG design used in this work.

**Table. 1.** Design parameters of the 1×8 AWG

| | | |
|---|---|---|
| Array WG | $N_{AWG}$ | 127 |
| | ΔL | 17.471 μm |
| | $W_{AWG}$ | 1.2 μm |
| | $G_{AWG}$ | 200 nm |
| FPR | $R_{FPR}$ | 159.035 μm |
| I/O WG | $N_{IO}$ | 1×8 |
| | $W_{IO}$ | 1.2 μm |
| | $G_{IO}$ | 1.2 μm |
| | Taper_L | 2 μm |

The normalized transmission spectrum of the 1×8 AWG is shown in Fig. 11. A low insertion loss was achieved below 1.5 dB at the center channel, and the non-uniformity among the eight channels is about 1 dB. The channel crosstalk was as low as -28 dB. The average optical bandwidth of single channel is 0.62 nm, or 75 GHz in the frequency domain.

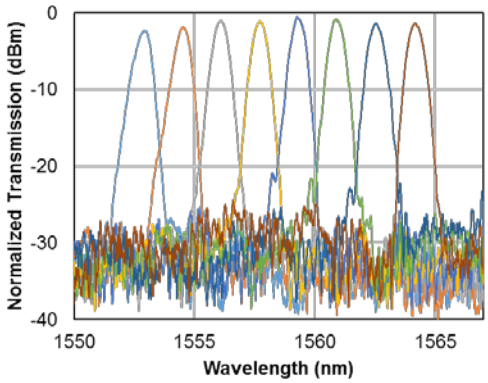


**Fig. 11.** Normalized transmission spectrum of the 1×8 AWG.

4.3 Heterogeneous DFB laser

The heterogeneous DFB laser was used as the laser source due to its low threshold current and single mode operation. In this work, the laser cavity length is 400 μm, which is longer than previous work to improve the device thermal impedance and series resistance [50]. The epitaxial layer design with 3 QWs is for lower transparency current density and lower threshold current density. A weak Bragg grating is required for such a long cavity. For this purpose, an edge Bragg grating was used instead of etched grating across the whole waveguide. The etched corrugations are defined at the edge of the waveguide, as shown in Fig. 5. The grating width $W_g$, is a new degree of freedom in design to finely tune the overlap between the grating tooth with guided optical field. Here, we used 30 nm

grating etch-depth and 400 nm grating width on the 1 μm silicon waveguide. The quarter-wavelength shifted Bragg gratings is carefully aligned with the silicon waveguide layer, which is critical to achieved desired grating strength and center wavelength.

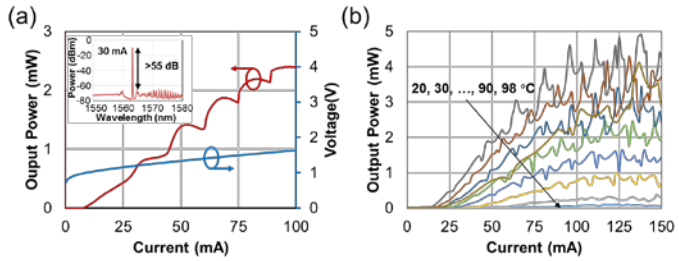


**Fig. 12.** (a) L-I-V curves of 400 μm heterogeneous DFB laser. Inset is the lasing spectrum at 30 mA current injection. (b) The CW operation of a 400 μm long heterogeneous DFB laser at high stage temperature up to 98 °C.

Fig. 12(a) shows light-current-voltage (L-I-V) characteristics of the heterogeneous DFB laser with 400 μm cavity under CW operation. The threshold current was measured to be 7.5 mA, corresponding to a threshold current density of 470 A/cm$^2$ at 20 °C. This shows an over 50% improvement compared with the previous 200 μm cavity DFB with 7-QWs [50]. The inset lasing spectrum in Fig. 12(a) indicates a single wavelength emission with a side mode suppression ratio (SMSR) over 55 dB. The kinks at the L-I curves relate to longitude mode hopping. This DFB laser on silicon kept CW lasing at high ambient temperature up to 98 °C, as shown in Fig. 12(b).

4.4 Heterogeneous EAM

Electroabsorption modulated lasers (EMLs) are widely utilized in commercial optical transponders, with their advance in broad-band, small footprint, large extinction ratio and high-speed modulation [68-70]. With a strong quantum confined Stark effect, the III-V quantum-wells structures can manipulate the absorption edge with the external electric filed. EAMs with lumped electrodes are used in this photonic circuit design [52]. Similar to integrated lasers we just discussed, the EAMs have a heterogeneous III-V/Si waveguide as the absorptive section between the adiabatic tapers, as shown in Fig. 4(b). However, the III-V epi consists of a thick active region with 12 QWs. 2.5 μm mesa width and 750 nm Si waveguide width are used to enhance the mode confinement factor in the QWs. The absorptive section is 75 or 100 μm long, which is a tradeoff between insertion loss and modulation depth.

Fig. 13(a) shows the transmission performance of the 100 μm long EAM at varying reverse bias from 0 to 6 V. The optical input is at TE polarization. Over 6 dB per 1 Vpp extinction ratio can be achieved across 1550-1570 nm with a low DC bias voltage below 3 V. The small signal frequency response of the heterogeneous EAM was measured in a lightwave component analyzer (LCA), as the result shown in Fig. 13(b). Over 24 GHz bandwidth is achieved on the EAM with a 75×2.5 μm$^2$ cavity. The inset shows a clear open eye diagram at 25 Gbps operation.

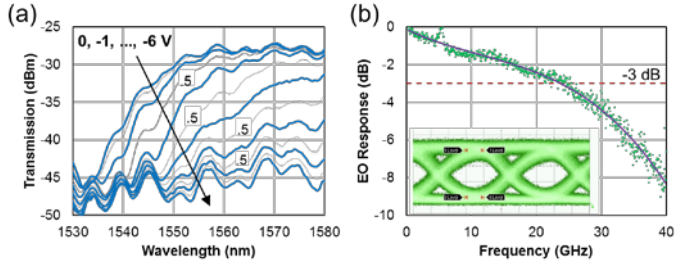


**Fig. 13.** (a) Power transmission of 100×2.5 μm$^2$ EAM versus reverse bias from 0 to 6 V (0.5 V interval); (b) EO response of EAM with 75 μm cavity and 2.5 μm mesa width at 1560 nm wavelength and 2V reverse bias. Inset: eye diagram under 25 Gbps operation with 1560 nm input wavelength and 3.3 V reverse bias.

4.5 Heterogeneous photodetector

The photodetector is another critical component in the transceiver network. A waveguide photodetector is used in this design, with a vertical PIN structure and 400 nm InGaAs intrinsic layer as the absorber [71, 72]. The input silicon waveguide is flared out to multimode waveguide with the same width of the III-V mesa. The PD cavity has a 4 μm wide and 30 μm long, as shown in the inset of Fig. 14(a). A low dark current of 10 nA at 2 V reverse voltage was achieved, shown in Fig. 14(a), benefitting from the optimized mesa dry etch and sidewall passivation process. The OE frequency response of the heterogeneous PD in Fig. 14(b) shows 3-dB bandwidth of 20 GHz. The internal responsivity of the photodetectors is measured at 1550 nm wavelength with TE polarization. The responsivity of the photodetectors with 30×4 μm$^2$ mesa was 0.45, and a higher responsivity can be achieved with a longer/wider cavity. The efficiency of the waveguide photodetectors can be improved with further mode engineering, such as to squeeze the mode into the absorber layer by tapering down the silicon waveguide.

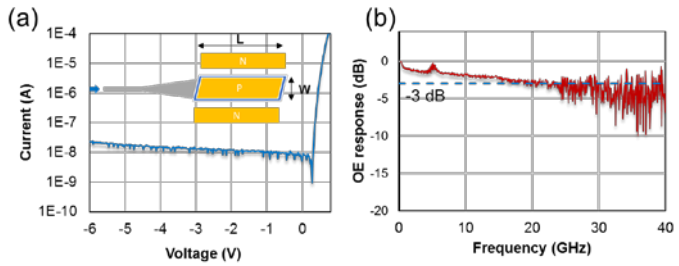


**Fig. 14.** (a) I-V curve of heterogeneous PD with 4×30 μm$^2$ and its top-view diagram in inset, and (b) its normalized small signal frequency response.

4.6 Inverse taper for fiber coupling

Coupling loss between silicon waveguide and optical fiber is one of the major sources of total optical loss in an optical link. Vertical fiber coupling with a grating coupler (GC) has coupling loss as low as 1.5 dB per coupling with dedicated multi-level designs [73, 74]. However, a low reflection and low loss GC design is still missing for the 500 nm SOI platform. Instead, edge butt coupling is commonly used, suffering from difficult alignment due to the large mode mismatch between waveguide and fibers. Other optimizing techniques, such as a waveguide mode convertor design [75-77], are not compatible with the thick device layer. To solve this problem, we designed a three-sectional mode convertor for a low loss fiber coupling. As shown in Fig. 15(a), the mode converter consists of three sections: (a) transition from partially-etched ridge waveguide to fully-etched stripe waveguide, (b) transition from stripe waveguide with 500 nm height to 300 nm height, and (c) an inverse taper with 300 nm height. This 300 nm tall strip waveguide is necessary for the inverse taper to "squeeze" the TE mode into the $SiO_2$ cladding at the taper tip, to achieve a low effective index and better overlap with fiber mode, as shown in the inset in Fig. 15(a). Therefore, neither extreme narrow taper tip nor EBL process is required in the process. In this work, 150 to 200 nm inverse taper tip widths were achieved with DUV lithography. The inverse taper 8-degree tilted from the normal direction from the facet to reduce the reflection. Fig. 15(b) shows experimental results of coupling efficiency and reflection with different inverse taper length and tip width. The minimum coupling loss was 4.7 dB per coupling when the taper tip width was 225 nm. The minimum reflection is about -20 dB at a taper tip width of 200 nm. The coupling loss can be further reduced with improved lithographic process and with a thicker BOX layer in the SOI substrate.

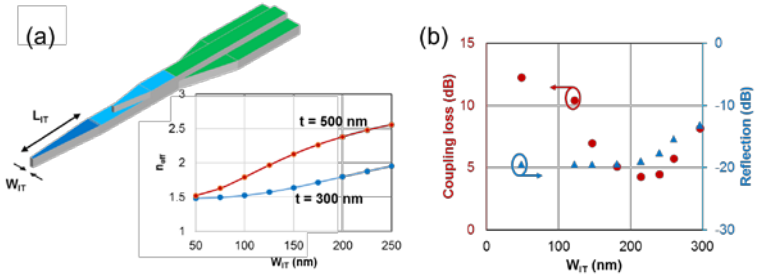


**Fig. 15.** (a) Diagram of the mode convertor on 500 nm SOI. Inset shows the effective index of the inverse taper changing with waveguide width; (b) measured fiber coupling loss and power reflection with the mode convertor.

**5. On-chip interconnection**

The diagram in Fig. 16 shows the setup for on-chip communication with the heterogeneously integrated ONoC circuit. Due to lack of an appropriate driver circuit, only one channel was tested at a time. The switch array was driven by a multi-pin probecard to route the data flow among transceivers. GSG radio frequency (RF) probes with 50 Ω impedance are used to directly drive the modulators and photodetectors, and needle probes are for DC bias of laser, SOA, monitor PD, etc. Broadband RF power amplifiers are used to boost the RF signal on modulator and the received signal from PD, and high-speed bias-tees to provide DC reverse bias on the modulator and PD. Small signal measurements are performed in a 67 GHz LCA, and the optical data transmission tests are performed with a high-speed digital communication analyzer (DCA). A 40 Gbps RF pattern generator is to provide pseudorandom binary sequence (PRBS) signal as the input signal. The DCA and pattern generator are synchronized with a frequency generator as the clock signal. Single mode fiber with 2 μm lensed tip is aligned with the silicon inverse taper at the facet for optical I/O coupling.

All the eight WDM channels of the AWG can be tuned simultaneously by the differential heater array on the array waveguides, as shown in Fig. 17(a) and (b). However, this tuning method is power intensive with an efficiency of 50 GHz/W, which is due to the inefficient thermal tuner design in this work. An alternative approach to align the laser wavelength with the AWG channel is to change the laser wavelength by adjusting the injection current, as shown in Fig. 17(c). With increasing the injection current from 20 mA to 200 mA, the lasing wavelength continuously scans over 3 nm. With manually tuning the wavelength of laser and AWG appropriately, eight DFB lasers with wavelength aligned to the corresponding AWG channels are shown in Fig. 17(d). The missing channel was caused by a defective device on the chip. The normalized transmission spectrum in Fig. 17(b) and (d) is from two back-to-back 1×8 AWGs on one waveguide, representing an ultra-low total insertion loss below 3 dB through two AWGs in transmitters and receivers.

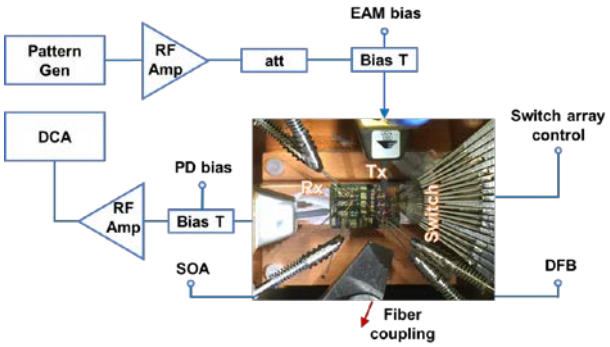


**Fig. 16.** Testing setup of the chip-level communication of the ONoC circuit.

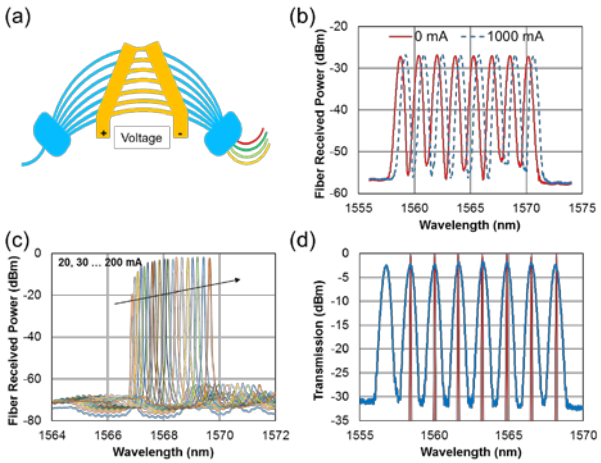


**Fig. 17.** (a) Schematic diagram of AWG with differential thermal tuner; (b) transmission spectrum of two cascaded back to back AWGs before and after thermal tuning; (c) output spectrum of 400 μm DFB laser with different injection current levels; and (d) the normalized wavelength of laser array aligned with the AWG channels.

It's worth noting that the RF signal with high speed data degenerates after the AWG. Due to the optical spectrum filtering effect, as illustrated in Fig. 18(a), when a non-return-to-zero (NRZ) signal with carrier frequency ($f_c$) and modulation frequency ($f_m$) passes a AWG channel with narrow optical bandwidth, both sidebands of the NRZ signal are truncated by the Gaussian-like optical filter, so that its response at higher frequency is depressed at the same time. With the AWG transmission shown in Fig. 11, its optical spectrum filtering effect has a 3-dB bandwidth of 26.5 GHz, as shown in Fig. 18(b). Consequently, at zero-detuning working status, a data-rate dependent power penalty of 0.25 dB and 0.52 dB for 25 Gbps and 50 Gbps data rate, respectively, can be expected [78].

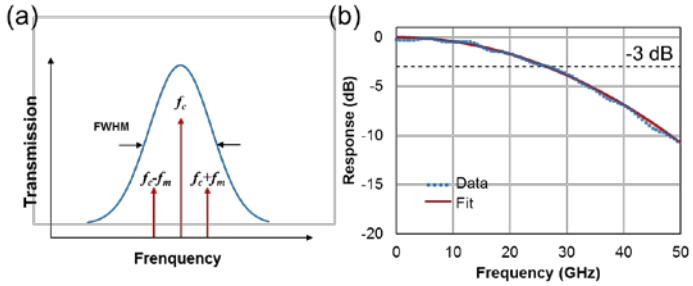


**Fig. 18.** (a) Spectrum filtering effect of an AWG channel as an optical band pass filter, the red arrows indicating the NRZ modulation signal; (b) calculated frequency response of an AWG optical channel.

The small signal frequency response of the modulator with corresponding photodetector in the receiver is shown in Fig. 19(a). A 6-dB bandwidth of 24 GHz was observed in the EAM-PD link. RF power reflections are seen due to the impedance mismatch between the 50 Ω probes and the high-impedance devices under reverse bias. The data transmission test with $2^7$-1 PRBS signal with the setup shown is shown in Fig. 16. A data rate up to 40 Gbps per channel performance is shown in Fig. 19(b), with the vertical scale of 50 mV/div in the eye diagrams. The unsymmetrical eye patterns are due to the clock distortion from the pattern generator. Clear eyes can be seen up to 40 Gbps operation, which is limited by the microwave amplifiers. The result shows a potential ultra-large capacity of the transceiver network, with 320 (8×40) Gbps per transceiver node, and 2.56 Tbps (8×320 Gbps) for the whole photonic circuit.

Further improvements are expected with integration of the photonic transceiver circuit with impedance matched CMOS driver circuit for low bit error rate operations.

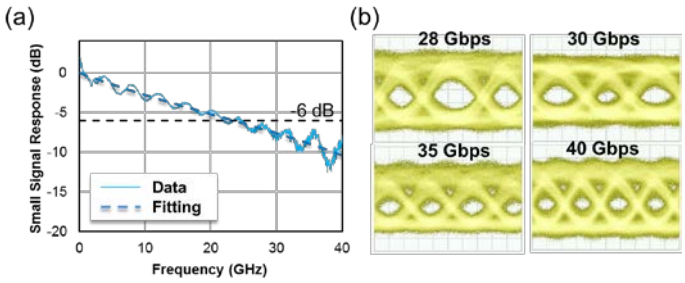


**Fig. 19.** (a) Small signal frequency response of the on-chip WDM channel; (b) Eye diagrams of on-chip communication from one WDM channel with varying data rate.

In this demonstration of on-chip interconnections, the photonic circuit's power consumption is dominated by the lasers. The DC power consumption of the DFB laser shown in the data link in Fig. 19(b) is about 1.5 pJ/bit with 70 mA current injection under a 40 Gbps data rate. A dynamic laser power tuning, with flexible laser control according to the link data rate, will be an effective way to save the energy consumption on the laser source. The power efficiency of laser wavelength tuning can be further reduced by incorporating a metal-oxide-semiconductor capacitor at the bonding interface [79]. The high-impedance modulator and photodetectors have about two orders of magnitudes lower power consumption compared with lasers. The total energy efficiency can be improved by integrating the photonic with electrical circuit to remove the 50 Ω transmission lines. However, the power that drains into the high-speed CMOS driver circuits is likely to take a large proportion of the total energy cost of a fully photonic-electronic integrated transceiver.

## 6. Summary

In this paper, we propose and demonstrate a novel heterogeneously integrated ONoC circuit for high-speed optical interconnections over short distances. Over 400 photonic components, including 300 active devices were heterogeneously integrated onto a single die on silicon substrate. The WDM photonic transmitter network achieves 8×40 Gbps at each node, and 2.5 Tbps total capacity with a high bandwidth density over 2 Tbps/cm. This can be further scaled up, and the integration level is largely limited by the interface of the electrical driver for 2-D integration, e.g. with wire-bonding approach. We believe that the ultra-dense photonic integration that follows the photonic "Moore's Law" will dominate the future high-speed data transmission with 3-D integrations with electrical circuits, e.g. with flip-chip bonding approach or through silicon via approach [19, 20].

We have shown the capability of the heterogeneous integration to integrate different types of photonic devices on silicon, promising for future low-cost and large-bandwidth chip-level optical interconnects. Selective die bonding technology and design of heterogeneous III-V/Si waveguide play important roles in this newly developed platform. Fortunately, most design rules and fabrication techniques can be transplanted from the pure III-V and Si CMOS platforms. As the next step, reliable process design kits of heterogeneous integration circuit with co-design of electrical circuit are being developed, which will accelerate the application of this platform to large scale photonic integration in near future.


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