Perspective: The future of quantum dot photonic integrated circuits

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Direct epitaxial integration of III-V materials on Si offers substantial manufacturing cost and scalability advantages over heterogeneous integration. The challenge is that epitaxial growth introduces high densities of crystalline defects that limit device performance and lifetime. Quantum dot lasers, amplifiers, modulators, and photodetectors epitaxially grown on Si are showing promise for achieving low-cost, scalable integration with silicon photonics. The unique electrical confinement properties of quantum dots provide reduced sensitivity to the crystalline defects that result from III-V/Si growth, while their unique gain dynamics show promise for improved performance and new functionalities relative to their quantum well counterparts in many devices. Clear advantages for using quantum dot active layers for lasers and amplifiers on and off Si have already been demonstrated, and results for quantum dot based photodetectors and modulators look promising. Laser performance on Si is improving rapidly with continuous-wave threshold currents below 1 mA, injection efficiencies of 87%, and output powers of 175 mW at 20 °C. 1500-h reliability tests at 35 °C showed an extrapolated mean-time-to-failure of more than ten million hours. This represents a significant stride toward efficient, scalable, and reliable III-V lasers on on-axis Si substrates for photonic integrate circuits that are fully compatible with complementary metal-oxide-semiconductor (CMOS) foundries. © *2018 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/).* https://doi.org/10.1063/1.5021345

I. INTRODUCTION

For decades, the silicon microelectronics industry has developed at an exponential pace improving performance, functionality, and integration density of electronic integrated circuits. Over the last fifty years, the integration density of transistors has gone from a few hundred per square millimeter to over 100 000 000 mm^{-2} in Intel's latest 10 nm technology node.[1] In parallel to this downscaling of components, a massive manufacturing infrastructure ecosystem has been developed capable of churning out tens of millions of wafers per year at the 300-mm wafer scale. This unprecedented level of commercial development has yielded low cost, high performance electronic devices that have revolutionized human society around the globe.

Meanwhile, the invention of the laser in 1960 at Hughes Research Laboratories and the eventual demonstration of room temperature (RT), continuous wave lasing in a semiconductor by Alferov,[2] following simultaneous key proposals by Kroemer[3] and Alferov[4] regarding the use of double heterostructures, ushered in a similarly impactful technological paradigm shift ultimately leading to the fields of photonics, optical communications, and the Internet. Photonic technologies have enabled new methods of materials processing and characterization, sensing and analysis of gasses and liquids, high bandwidth data transmission interconnecting the entire planet, and numerous other technologies that have transformed our daily lives. Yet despite these rapid advances, photonic devices have remained bulky, expensive, and modular in nature, in stark contrast to the advancements in high-density

integration in Si-based electronics. To address this discrepancy, silicon photonics was proposed whereby established complementary metal-oxide-semiconductor (CMOS) manufacturing processes and materials would be utilized to create photonic components with high integration densities. Such a platform leverages the already developed and highly optimized processing techniques and the economy of scale uniquely afforded by decades of silicon microelectronics development.

The CMOS platform provides a nearly ideal design space for photonic integrated circuits (PICs) due to the high-quality interfaces and refractive index contrasts that can be achieved between Si, Ge, SiO_2, Si_3N_4, and other dielectrics. Using various combinations of these materials with silicon-on-insulator (SOI) substrates, waveguides can be designed to cover optical wavelengths from the ultraviolet to infrared.[3–9] The challenge then becomes how to integrate the other components necessary to form useful PICs with complex functionality. Specifically, how does one obtain lasers, modulators, photodetectors (PDs), and non-reciprocal components such as isolators and circulators? Engineered devices made from Si and Ge can cover modulation and detection for wavelengths around the near-infrared[10] but are not suitable outside that range. Additionally, the indirect bandgaps of Si and Ge make them unsuitable for high performance lasers or amplifiers with the only demonstrated laser in this material system having orders of magnitude a higher threshold current density at 300 kA/cm^2 [11] than what is achieved in direct-gap III-V materials integrated with Si, as will be detailed below.

Overcoming the inherent limitations of Group IV materials for gain, efficient modulation, and detection at wavelengths outside the near-infrared requires incorporating III-V materials with the silicon photonics platform. Until recently the entirety of work done on III-V integration with Si has fallen into two categories that have evolved in terminology to be designated either "hybrid" or "heterogeneous." Going back in the literature, the terminology is interchanged, but now it is commonly accepted that hybrid integration refers to co-packaged III-V and Si devices on native substrates (more specifically SOI for Si) while heterogeneous integration refers to III-V materials bonded to an SOI substrate. In the case of hybrid integration,[12] the light is butt-coupled between III-V and Si chips requiring extremely precise alignment that complicates packaging and arguably limits scalability. Meanwhile in heterogeneous integration, light is evanescently coupled vertically into a Si waveguide from the III-V active material (see Fig. 1).

This approach, first demonstrated at UCSB in 2006,[13] simplifies packaging by monolithically integrating all components and transfers the alignment complexity to the semiconductor processing side of things where established lithography techniques trivialize the issue. A detailed review of the current state-of-the-art in heterogeneous integration is presented in Ref. 14. Demonstrated performance shows that heterogeneous devices can rival, and occasionally exceed, native substrate devices and can exceed what is achievable purely with Si and Ge. Additionally, the PIC complexity of heterogeneous devices has rapidly grown to rival that of PICs on native substrates with over 400 components on a single waveguide in recent results.[15] Historical integration densities of PICs that include lasers are shown in Fig. 2. The heterogeneous approach has been widely adopted in industry by Juniper Networks,[16] Hewlett Packard Enterprise,[17] and Intel.[18] Intel is currently in volume production of optical transceivers using heterogeneous integration.

Currently the biggest driver in further developing silicon photonics is for datacenter and high-performance computing applications. Optical data transfer can be performed at much higher data rates
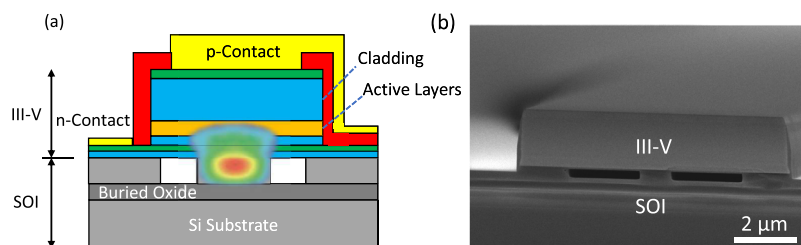

FIG. 1. (a) A schematic diagram of a heterogeneously integrated III-V laser on Si including the evanescent optical mode. (b) Micrograph of an etched III-V laser ridge bonded to a patterned SOI substrate.
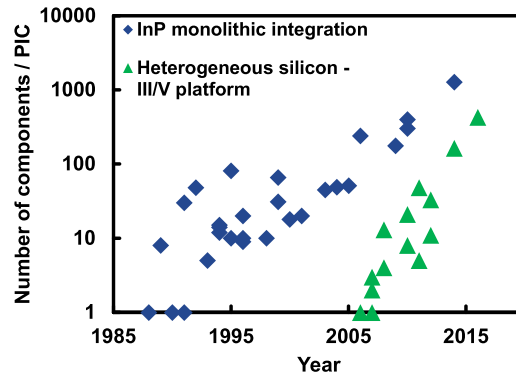
FIG. 2. Component counts in a single photonic integrated circuit are shown for PICs on native InP (blue diamonds) and for heterogeneously integrated PICs with lasers on Si (green triangles).

with much lower energy consumption than can be done with electronics and is needed to overcome the performance bottleneck presented by electronic interconnects within datacenters and supercomputers. Optical transmission has already been adopted for decades in long-haul communications and much more recently for shorter links down to the individual boards within a server rack, mostly through native substrate vertical-cavity surface-emitting laser (VCSEL) solutions, but further downscaling to within the board and eventually to on-chip interconnects has proved challenging. Integrating photonics at these length scales requires small-footprint and low energy devices that are tolerant of the high temperatures sustained near the electronic processors. Designing photonic devices that meet all of these criteria is challenging as sidewall scattering and recombination hinder performance in small devices in addition to the high temperature requirements. Additionally, an in-plane laser cavity is desired for integration with additional on-chip photonic components for increased functionality. While datacenters are the principle driver for these changes, smaller footprints and higher integration densities will be a boon for any PIC application.

In order to achieve broader commercial viability of PICs, the high costs of heterogeneous integration must be addressed. For heterogeneous integration, all III-V devices are grown first on a native substrate. Then the device is bonded to Si, and the III-V substrate is removed and discarded (or reused). Relative to Si substrates, III-V substrates are orders of magnitude more expensive in addition to only being available at much smaller wafer sizes that limit scalability. See Table I for a comparison of III-V wafer costs and sizes with Si. If the III-V substrate cost could be avoided, the cost per PIC would go down significantly (by as much as 50%). The only way to do this is by moving to an epitaxial III-V/Si process for photonic integration. Such an approach offers several possible embodiments: (1) growth on Si followed by wafer bonding and Si substrate removal, (2) integrating as-grown III-V components with the Si device layer of an SOI substrate, and (3) using as-grown III-V layers for the entirety of the PIC with Si serving only as a low-cost substrate to facilitate scalable manufacturing. Each approach has its own benefits and drawbacks and will be detailed below. A detailed techno-economic analysis of the benefits of epitaxial integration is the subject of Ref. 19.

In order to realize the benefits of an all-epitaxial process, the challenges associated with mismatched epitaxy must be overcome. Relative to Si, non-nitride III-V materials have larger lattice constants and higher coefficients of thermal expansion (see Table II) which, for unoptimized growth conditions, result in high densities ($\sim 10^9$ cm^{-2}) of crystalline defects including primarily threading

TABLE I. Comparison of the price and wafer diameter for various III-V substrates and Si and SOI substrates.

	InAs	InP	GaAs	SOI	Si
Substrate cost ($/cm^2)	18.25	4.55	1.65	1.30	0.20
Maximum size (mm)	76	150	200	450	450

TABLE II. Comparison of the lattice constants and the coefficient of thermal expansion (CTE) mismatch for common III-V semiconductors with Si.[23]

	Si	GaAs	InP	GaSb	AlSb
Lattice constant (Å)	5.431	5.653	5.869	6.096	6.136
% mismatch w/Si (%)	0	4.09	8.06	12.2	13.0
CTE mismatch (%)	0	119	76.9	198	62.3

dislocations (TDs) and antiphase domains. Fortunately, through careful optimization of growth conditions and utilization of dislocation filtering layers and techniques,[19–22] the defect density can be reduced by a few orders of magnitude enabling near native substrate level performance.

To truly achieve native substrate performance and reliability, quantum dot (QD) active regions must be adopted over quantum wells (QWs). Quantum dots represent zero-dimensional, particle-in-a-box-like quantum confined structures that can be formed through a self-assembly process using InAs on (In, Ga, Al)(As, P) layers. Their artificial-atom-like properties make them ideal for low threshold, high temperature lasers, high performance semiconductor optical amplifiers (SOAs), low dark current photodetectors, and potentially high efficiency quantum confined Stark effect modulators. They also have unique dynamic properties that enable low feedback sensitivity and narrow linewidth lasing, but, most importantly, their in-plane carrier confinement dramatically reduces in-plane carrier migration to heteroepitaxial defects. These attributes and more are covered in the remainder of this paper.

The remainder of this perspective will be organized as follows. First, the benefits, challenges, and proposed solutions of epitaxial integration will be detailed. Then, the specific motivations for switching to quantum dot-based active regions for photonic devices will be covered, showcasing results on native substrates and Si. Applications targeting the datacom and telecom wavelength bands around 1.31 μm and 1.55 μm will be emphasized since they currently dominate ongoing research in photonic integration.

II. HETEROEPITAXIAL GROWTH AS AN INTEGRATION PLATFORM

A. The challenges

In order to realize the economic benefits of an all-epitaxial integration scheme, the performance discrepancy between grown and bonded devices must be resolved. Epitaxial III-V on Si devices have historically shown diminished performance relative to their counterparts grown on native substrates due to high densities of crystalline defects. With the notable exception of GaP, relative to Si, all III-V materials have a substantial mismatch in their crystalline lattice constant, and all III-Vs show substantial mismatch in their coefficients of thermal expansion (CTEs). Additionally, there is a third mismatch in that III-V materials are polar compounds and Group IV materials are nonpolar. This can lead to antiphase boundaries (APBs) between two regions where Group III and Group V material sublattices are misaligned such as across single atomic steps. Each of these mismatches must be overcome to achieve reasonable device performance. Figure 3 shows representative images of dislocations and antiphase domains taken using a transmission electron microscope (TEM).

The lattice constant mismatch leads to substantial stress accumulation in the first few pseudomorphic layers of material that are grown, which leads to relaxation above a critical thickness. This relaxation comes about through the generation of misfit dislocations which are essentially lines of aberrant bonding running along the mismatched interface. Since no dislocation can terminate within a crystal for energetic reasons, the misfit dislocations must either reach the edge of the wafer or turn up toward the growth interface to form threading dislocations (TDs). If growth is being done in a region where the distance to a sample edge is much larger than the distance to the epi surface (for example, in planar growth across an entire substrate), then the misfits will preferentially form TDs. Dislocations have associated trap states that act as nonradiative recombination centers and tend to getter an atmosphere of point defects in their vicinity that promote further recombination and gradual device
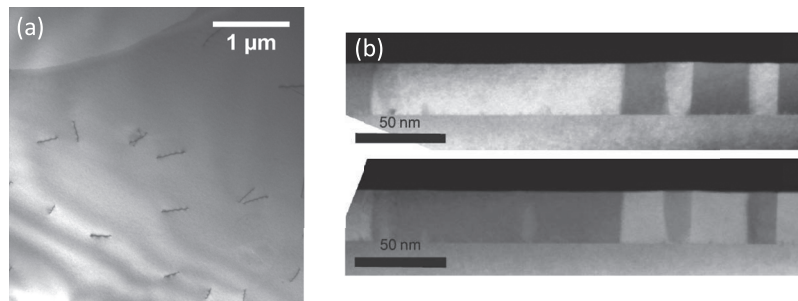
FIG. 3. (a) Plan-view transmission electron microscope image of GaAs on Si showing threading dislocations intersecting the surface. (b) Cross-sectional transmission electron microscope image of antiphase domains in GaP on Si. Adapted and reprinted with permission from Németh *et al.*, "Heteroepitaxy of GaP on Si: Correlation of morphology, anti-phase-domain structure and MOVPE growth conditions," J. Cryst. Growth **310**, 1595–1601 (2008). Copyright 2008 Elsevier.[24]

degradation through recombination enhanced dislocation climb,[25,26] whereby the total dislocation length within a region of high recombination (high minority carrier population) grows steadily. As a result, III-V photonic devices grown on Si tend to have lower internal efficiencies and shorter device lifetimes. The bulk of effort that has been put into III-V/Si growth has been in dealing with TDs. The most promising techniques are presented below along with the results for the optoelectronic devices they have facilitated.

The CTE mismatch becomes a problem during the cool-down from growth temperature. This problem is well known to the bonding community and led to the development of low temperature bonding techniques to prevent bonded films from cracking or delaminating.[27] In epitaxial growth, the highest temperature steps likely to be reached for III-V materials are ~600 °C. Upon cooling to room temperature, following growth of a film that is a few microns thick, a residual strain of a few percent can be expected. This strain has two primary effects. If nucleation centers are present on the wafer, such as surface contaminants, growth defects, or the clips from poorly designed sample holders, then cracks will form in the III-V film that will destroy the device yield. Fortunately, the cracking problem is one that can be solved through relatively simple procedures in the engineering of sample holders and sample preparation prior to growth. Additionally, III-V growth can be done selectively through masking to allow some thermal stress to relax. In GaAs grown on Si, the theoretical thickness threshold for cracking is ~5 μm, but with a lack of nucleation centers, experimental values put the cracking threshold at 6-7 μm.[28] In addition to cracking, the residual stress drives degradation of III-V devices by creating an additional driving force for dislocation growth.[26]

The issue of antiphase boundaries (APBs) was largely solved decades ago by utilizing miscut Si substrates that preferentially form double atomic steps on the surface.[29] In III-V/Si epitaxy, the Group V species always nucleates preferentially on the Si surface and terminates at one monolayer. As a result, APBs only form at single atomic steps on the Si surface, and if single-steps are absent, then so are the APBs. However, the problem with using miscut Si is that the holy grail for photonic integration is CMOS compatibility, and miscut Si is not CMOS compatible. The need for an APB-free CMOS compatible Si substrate is what has driven recent work in III-V/Si epitaxy.

B. The solutions

Given that lasers were the primary missing components in the silicon photonics platform, the bulk of III-V/Si heteroepitaxy research has been focused on generating efficient lasers. The first laser ever reported on Si was an AlGaAs double heterostructure laser that operated in pulsed mode at 77 K with a threshold current density of 10.8 kA/cm^2 and a differential quantum efficiency of 1.2% in 1984.[30] The best results for a double heterostructure laser were achieved in 1988 for an InGaAsP/InP device with a threshold current density of <4 kA/cm^2 and less than 5% increase in current after 5 h at constant power aging.[31] After 19 years of further research, room temperature (RT), continuous wave operation was achieved in a QW laser with threshold current densities of 269 A/cm^2 along with a device lifetime of 4 h.[32] To reach these performance levels, Groenert *et al.* used a heavily optimized Ge/GeSi/Si buffer with a TD density of 2×10^6 cm^{-2} grown on miscut

Si to avoid antiphase domains.[33] To the best of our knowledge, no epitaxial QW laser on Si has ever exceeded this performance benchmark. Meanwhile, the first QD laser on Si was grown in 1999 using In_4Ga_6As QDs and lased under pulsed conditions at 80 K with a threshold current density[34] of 3.85 kA/cm^2. Within six years, quantum dot lasers were also being operated CW on Si at RT and were showing threshold current densities of 1.5 kA/cm^2 despite reported dislocation densities[35] of 2-5 × 10^7 cm^{-2}. Then, in 2012, the previous QW records were shattered by QD lasers with RT CW threshold current densities of 163 A/cm^2 and CW lasing up to 30 °C with reported dislocation densities[36] of 5 × 10^6 cm^{-2}. In 2014, narrow ridge QD lasers were produced setting records for the absolute threshold current at 16 mA, output power at 176 mW, and continuous wave lasing up to 119 °C (exceeding even heterogeneous device performance) despite dislocation densities[37] of 2 × 10^8 cm^{-2}. These devices were directly compared with simultaneously fabricated QW lasers with an identical TD density showing that QW devices were incapable of lasing at all at these TD densities.[38] Further testing of the same devices showed extrapolated lifetimes of 4600 h at aging conditions of 30 °C and more than twice the threshold.[39] These performance results and later results by Chen *et al.* in 2016 showing 62.5 A/cm^2 current densities and extrapolated lifetimes >100 000 h at relaxed conditions[40] began to make the case that QD lasers grown on Si can be a commercial technology. The only problem is that none of these results made use of CMOS compatible on-axis (001) silicon substrates. The historical trends in threshold current density and device lifetime for these lasers and newer results described below are displayed in Fig. 4.

Within the past year, efforts have doubled down on developing CMOS compatible, epitaxial materials platforms on Si leading to impressive results in material quality and record setting device performance. Many strategies are being pursued by various groups. The first ever lasing results on on-axis Si were achieved simultaneously at the University of California, Santa Barbara by Liu *et al.*[41] and Norman *et al.*[42] using III-V/Si buffer templates developed by Huang *et al.* at Yale University[43] and Li *et al.* at the Hong Kong University of Science and Technology.[22] The approach by Huang *et al.* utilized a 45 nm pseudomorphic GaP layer grown directly on Si by metal-organic chemical vapor deposition (MOCVD) that was pioneered by NAsP$_{III/V}$, GmbH. NAsP$_{III/V}$ utilizes a series of carefully optimized surface treatments including Si homoepitaxy to grow antiphase domain free GaP directly on on-axis Si with no additional defect formation due to the small mismatch between GaP and Si.[44] Using such a template for subsequent mismatched growth of GaAs is simpler than direct Si growth because only the TDs must be contended with and GaAs nucleates more favorably on GaP. The first results on this template yielded TD densities of 2 × 10^8 cm^{-2}. Further refinement of the GaAs/GaP growth conditions by Jung *et al.*[21] and the inclusion of thermal cycle annealing and dislocation filter layers pushed the TD density down to 7 × 10^6 cm^{-2}. A second, equally promising approach is the procedure developed by Li *et al.* at HKUST which utilizes a CMOS compatible crystallographic etch to pattern v-shaped trenches in an on-axis Si substrate, aspect ratio trapping to limit defect propagation, and coalescence of an overgrown GaAs layer to provide bulk
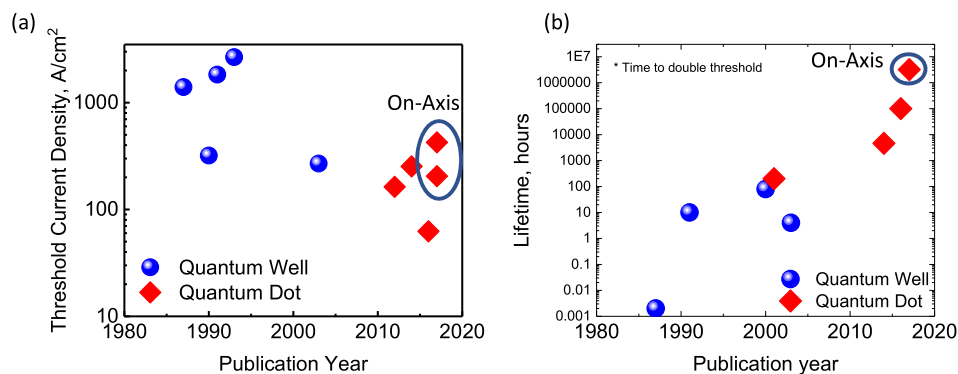

FIG. 4. (a) Threshold current density and (b) device lifetime (either extrapolated or measured) for lasers on Si operating in the continuous wave mode. The distinction is noted between historical results on miscut Si substrates and recent results on CMOS compatible on-axis (001) Si.
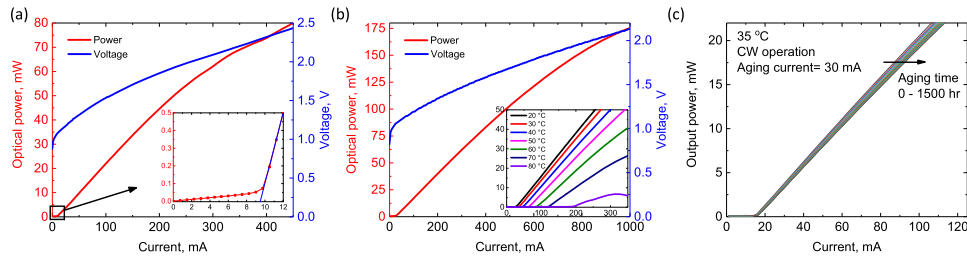
FIG. 5. Highlighted results for as-cleaved Fabry–Pérot lasers on on-axis (001) Si substrates showcasing (a) record low threshold currents of <10 mA (from Ref. 50), (b) record single-facet output powers of 175 mW and continuous wave lasing up to 80 °C (from Ref. 50), and (c) LI curves as a function of continuous aging time at twice the threshold and 35 °C from zero to 1500 h aging (from Ref. 51).

templates.[45] The {111} v-groove surface suppresses the formation of antiphase domains and limits TD propagation as demonstrated in the pioneering work at IMEC by Paladugu *et al.*[46] Coalesced films of GaAs-on-v-groove-Si (GoVS)[42] yielded TD densities of 7×10^7 cm^{-2} and stand to be improved significantly with the inclusion of additional dislocation filtering layers and thermal cycle annealing. Efforts are also underway to grow GaAs directly on planar Si by way of an AlAs nucleation layer by Chen *et al.* at University College London resulting in electrically injected lasing, but defect densities have not been reported.[47] Additional work is ongoing to produce as-grown laser cavities using III-V from a single trench,[48,49] which has yielded optically pumped devices operating at room temperature.[49]

Of the previous approaches to CMOS compatible Si integration, the GaP/Si and GoVS templates are most mature and have yielded the most promising device results with performance exceeding that obtained on miscut Si and rivaling or exceeding even what has been achieved through heterogeneous integration. On the GaP/Si templates, Fabry–Pérot lasers have been grown that far exceed the performance of identical structures grown on miscut Si templates. We have achieved CW RT threshold currents as low as 9.5 mA, single-facet output powers of 175 mW, ground state lasing up to 80 °C, and wall-plug-efficiencies as high as 38.4%, and extrapolated lifetimes in excess of 10 000 000 h for aging at 35 °C and twice the threshold current density, all obtained with as-cleaved facets.[50,51] Highlights are shown in Fig. 5.

These devices are currently undergoing aging at elevated temperatures and current densities to directly evaluate their suitability in realistic datacenter and high performance computing (HPC) environments. Meanwhile, using the GoVS template, we have achieved electrically injected lasing in micron-scale ring resonator cavities showing threshold currents in the sub-milliamp regime (Fig. 6) for rings of 5 μm radius and 3 μm width which shows the tolerance of QD active regions to sidewall recombination in small cavities. These devices also showed CW lasing up to 100 °C.[52]

Epitaxial integration could take one of several embodiments. One approach pursued by IMEC uses aspect ratio trapping in nanoscale trenches to eliminate crystalline defects within a couple hundred nanometers of growth.[49] Such an approach could be integrated with SOI [Fig. 7(a)] and is promising in that the active layers can be grown within reasonable coupling distances of the
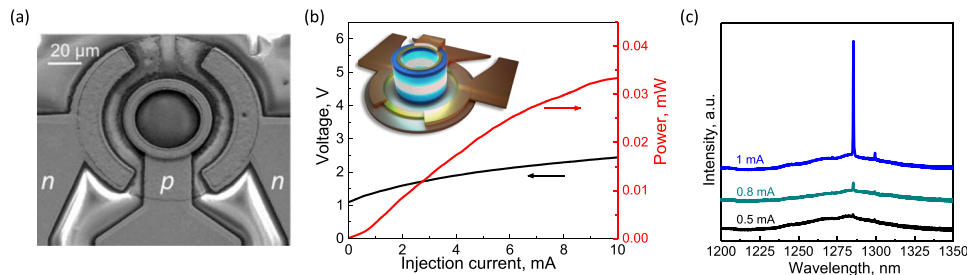

FIG. 6. (a) Scanning electron micrograph of a microring device. (b) Power-current-voltage curves for a sub-milliamp threshold laser with inset illustration. (c) Optical spectra showing the lasing mode for various pump currents. (Adapted from Ref. 52.)
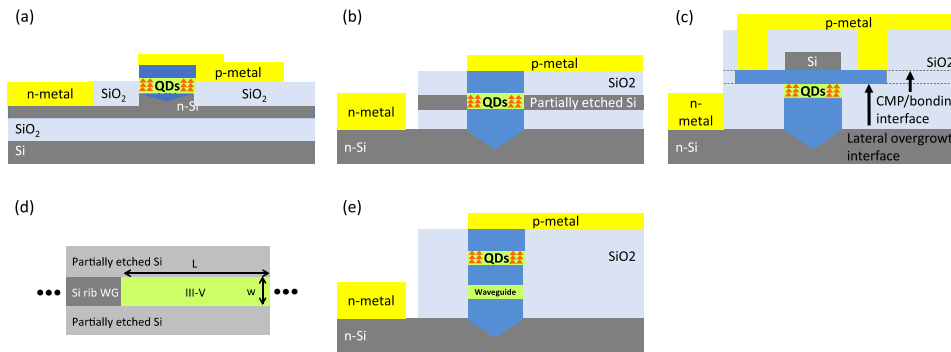
FIG. 7. Schematic illustrations of potential III-V/Si integration schemes including embodiments using a silicon waveguide: (a) direct growth on SOI, (b) growth on patterned SOI from the handle wafer with butt-coupling to a Si device layer waveguide, and (c) growth on Si with a bonded Si waveguide on top of the III-V epi. (d) Top-down schematic of structures [(a)–(c)] showing III-V and Si waveguides. (e) An all III-V integration scheme where a separate waveguide layer is grown in the III-V layers for evanescent coupling.

underlying Si and in that the optical cavity is formed as-grown rather than being etched which may lead to improved passivation and reduced optical scattering. The problem with such an approach is that electrical injection of such structures is challenging and will likely have to be done through the highly defective III-V/Si interface which could generate a large resistance. Alternatively, standard III-V laser epi structures with thick buffers and contact layers could be grown on SOI with electrical injection all in the III-V layers and tapers or grating couplers could be used to inject the light into the underlying Si waveguides. Tapers are commonly used for heterogeneous integration to force the optical mode into the Si, and recently a slotted waveguide was used to incline emitted light from a laser at 54.6° with a low divergence angle of 1.7° which could be directed on a vertical coupler in the Si substrate for waveguide integration.[53] Another approach is to follow the established methods of heterogeneous integration and bond III-V epi grown on Si to patterned SOI substrates. Such an approach gains the economic benefits of eliminating the III-V substrate cost but retains the manufacturing complexity associated with wafer or die bonding. A simpler but analogous method would be to deposit amorphous Si[54] or simply bond a Si wafer to the top of the III-V epi and process it into waveguides [Fig. 7(c)]. This approach would use evanescent coupling in the upward direction analogous to the coupling scheme in current bonded lasers. The bonding in this case would be a bit simpler than bonding dies of III-V epi since it could easily be done at the wafer scale requiring minimal alignment. A fourth approach could involve the direct growth of III-V material from the handle wafer of an SOI substrate with the device active layers aligned to the device layer silicon [Fig. 7(b)]. The device layer would then be processed into standard silicon photonic components optimized around the SOI platform, and the III-V material would be butt-coupled to a waveguide. The principle challenge with this approach is that the III-V must completely fill the space up to the waveguide as the coupling efficiency drops rapidly with gaps even as small as 500 nm.[55] We discuss this embodiment in more detail in Ref. 38. A final proposed approach would be to simply perform all functions in the III-V epi layers either through evanescent coupling to a waveguide layer [Fig. 7(e)], regrowth, or intermixing. This embodiment would purely adopt Si as a cheap scalable substrate and leverage the suite of techniques and processes already commercialized in InP PICs for active and passive functions.[56] Such an approach achieves all the advantages of III-V PICs over heterogeneous integration, eliminates the III-V substrate cost, and improves the thermal impedance of devices due to silicon's higher thermal conductivity than III-Vs.[57]

III. THE PROMISE OF QUANTUM DOTS

In solid-state materials, a quantum dot (QD) is a small, three-dimensional inclusion of a narrower bandgap material within a wider bandgap matrix. At quantum length scales, the 3D confinement potential of the inclusion leads to discrete energy levels analogous to the textbook case of a particle-in-a-box. The discretization leads to localized, atom-like properties with size and confinement dependent energy

levels. For optoelectronic applications, the most well-developed QD material system is In(Ga)As within either a matrix of (Al, Ga)As materials or in a matrix of (In, Al, Ga)(As, P) materials targeting the InP lattice constant. The importance of distinguishing these two materials systems derives from the mechanism of QD formation during crystal growth. In the most common approach, quantum dots form via the Stranski-Krastanov growth mode.[58] In this growth mode, surface energetics initially favor a planar growth of the QD material, but with increasing thickness, the surface energy is counterbalanced by building strain energy from the mismatched lattice constants. The strain energy ultimately drives the re-organization of the QD material into 3D islands through a self-assembly process allowing for more efficient strain relaxation. The exact atomistic details of this growth mode are not completely understood, but a detailed review of current understanding can be found in Refs. 59 and 60. Figure 8 shows a transmission electron microscope (TEM) image of buried InAs QD layers in a multi-stack structure used to make lasers. Quantum dots have also been demonstrated in other solid-state materials systems for various applications including Ge/Si,[61] and III-Sb materials for mid-IR applications,[62] but these systems have yet to show the commercially relevant performance levels achieved regularly in the In(Ga)As on GaAs and InP systems.

Due to the self-assembled nature of QD growth, the ultimate properties of the material are highly dependent on kinetic restraints during growth. Properties such as the areal QD density, size homogeneity, ground state transition energy, energy level separation, and number of confined states can all be tuned to some degree and optimized for a target application by changing growth temperature, growth rate, V/III ratio, and sequences (e.g., growth interrupts or capping procedure). This fine tuning is on top of the tunability achieved by changing the composition of the QDs themselves and the surrounding cladding material. Figure 9 shows the photoluminescence spectra of (a) InAs QDs on GaAs, (b) InAs QDs on 2 nm $In_{.15}Ga_{.85}As$ on GaAs, and (c) InAlGaAs on InP. Corresponding atomic force microscope images of uncapped quantum dots are shown in Figs. 9(d)–9(f).

By leveraging the localized nature of each dot, the atom-like discrete density of states, and the broad range of tunability through growth conditions and epi design, many new opportunities are granted for improved performance in all varieties of optoelectronic devices. In Secs. III A–III G, the possible improvements afforded by QD active regions as opposed to QW or bulk based devices will be detailed in terms of specific devices desirable in PICs. Additionally, and possibly more importantly, the role played by the in-plane carrier confinement in enabling epitaxial integration will be detailed.

A. Lasers

Lasers are by far the most explored device in QD optoelectronics. The idea of a quantum dot laser was first proposed by Arakawa and Sakaki in 1982,[63] but it was not until 1992 that such a laser was experimentally demonstrated.[64] Following the first demonstration, the growth conditions and laser designs were rapidly improved[58] leading to QD lasers outperforming their QW counterparts by the year 2000.[65]
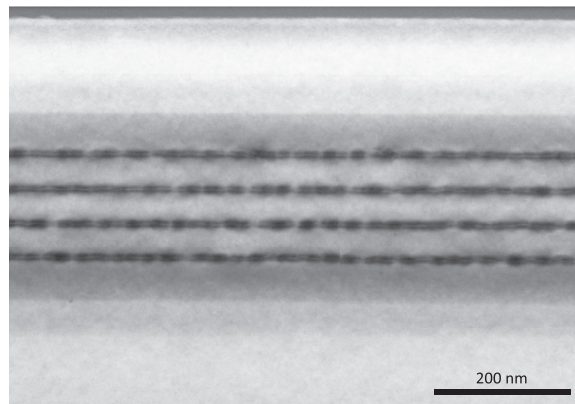

200 nm

FIG. 8. Transmission electron microscope image of four layers of InAs quantum dots.
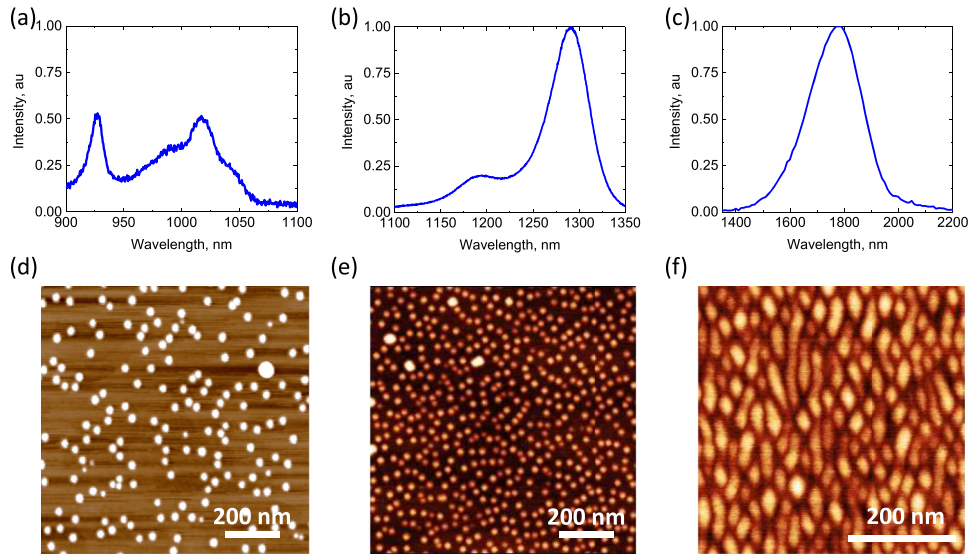
FIG. 9. (Top) Photoluminescence spectra and (bottom) atomic force microscopy images of InAs quantum dots grown at different conditions are shown to emphasize the range of material tunability that is achievable.

The discrete density of states of QDs is the key characteristic allowing for their improved performance in terms of lower threshold, higher temperature operation, and higher characteristic temperature, T_0. The concept is analogous to that which led to the development of QW lasers over bulk materials. As the density of states is further discretized, the subbands collapse into delta-function-like energy levels with atom-like degeneracy, meaning that for the case of a quantum dot in the ground state, there is a maximum occupancy of two electrons, as dictated by the Pauli exclusion principle. Relative to higher dimensional structures, this means that there will be less Fermi level pinning at the band edge, and thus, it will be easier to achieve population inversion. Population inversion is a necessary criterion to the onset of lasing as it sets the transparency condition where stimulated emission exactly cancels stimulated absorption.[66] The transparency current can be thought of as the current necessary to achieve lasing in an idealized, lossless laser cavity. As such, it represents a floor on the lowest achievable threshold current limiting the achievable energy efficiency of a laser.

Another important characteristic of QD lasers that will enable improved energy efficiency is that they have reduced sensitivity to sidewall recombination.[52] Each QD effectively acts as a trap for charge carriers moving in plane thus effectively reducing the in-plane diffusion length. Experimental analysis of the ambipolar diffusion length in QD lasers has found that it can be less than 1 μm but is dependent on the injection level, rising to a maximum of ~1.5 μm, due to the weaker confinement in the excited states of the QD.[67] Typical diffusion lengths in QWs are in the range of several microns, so by switching to a QD active region, devices can be fabricated at smaller scales to achieve lower threshold currents and better energy efficiency. Figure 10 shows the threshold current vs ridge width for deeply etched Fabry–Pérot lasers with a 7 QD layer active region and for deeply etched micron-scale ring structures.[52] It can be clearly seen that even at the smallest dimensions the threshold currents are still decreasing with cavity width indicating the low impact of sidewall recombination. In addition to efficiency improvements, such downscaling will also lead to improved integration density for increased PIC functionality and performance.

The high temperature performance of QD lasers comes about from the inability of the carrier population to thermally broaden into higher states. In the case of InAs QDs, the typical separation between the ground state and first excited state within the conduction band is 70 meV with state-of-the-art devices at 80 meV or higher,[68] both far exceeding kT at room temperature. There are two primary figures of merit for describing a laser's performance at elevated temperatures. One is simply the maximum temperature where lasing is sustained, and the other is the characteristic temperature, T_0, which is a measure of how much a laser's threshold current, I_{th}, changes with temperature as
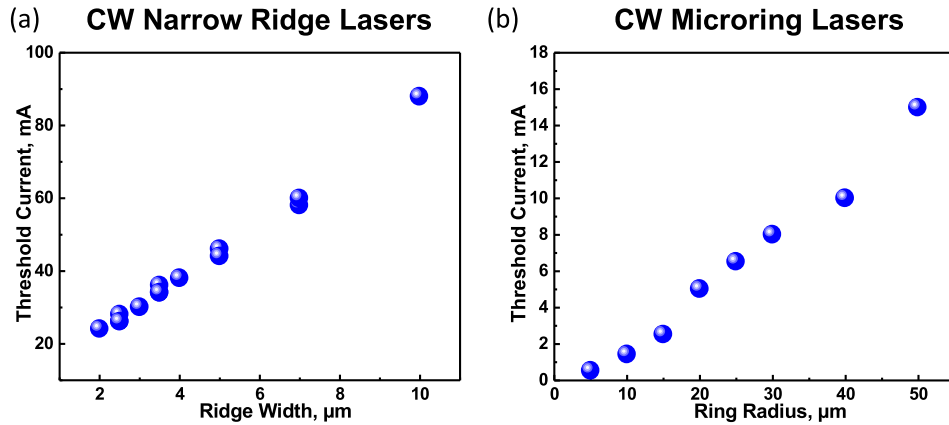
FIG. 10. (a) Threshold current for narrow ridge quantum dot lasers grown on GaAs showing a linear decrease in threshold with decreasing ridge width. (b) Threshold current for microring lasers grown on Si (from Ref. 52) showing decreasing threshold with ring radius.

defined by

$$I_{th} = I_0 e^{T/T_0}$$

with larger values of T_0 indicating more stable laser operation with changing temperature. Temperature stability is highly desirable for datacenter and HPC applications as it reduces the overhead needed to adjust laser drive currents due to temperature fluctuations on-chip. While infinite characteristic temperatures were theorized and realized over a limited range of temperatures (5-70 °C),[69] truly temperature invariant operation has never been realized due to the unfavorable offsets in the valence band that limit hole confinement and yield hole energy level spacings of only a few meV.[70] Nevertheless, QD lasers outperform their QW counterparts in T_0 and have far exceeded previous records for high temperature CW operation with commercially available native substrate lasers operating up to 220 °C[68] and heterogeneously integrated lasers operating up to 100 °C.[71]

The dynamic properties of QD lasers also deviate from their QW counterparts in beneficial ways with the most notable being the theoretical possibility of negative or zero values of the linewidth enhancement factor, α. The linewidth enhancement factor (LEF) describes the ratio of changes in the real part of the complex refractive index, $\tilde{n} = n + jn_i$, to changes in the imaginary part,[66]

$$\alpha = -\frac{dn/dN}{dn_i/dN}.$$

To understand the origin of the reduced LEF, one must explicitly consider many-body effects and the interaction between states within the QD and in the wetting layer in addition to the effects of inhomogeneous broadening on the complex susceptibility.[72] Smaller values of the LEF result in narrower laser linewidths, higher feedback tolerance, and higher output powers. Typical vales of the LEF are from 4 to 6 for QWs while near zero values having been experimentally observed in QDs.[73–75] Results from our previously described quantum dot lasers on Si in Ref. 50 show LEFs as low as 0.25 as measured by sub-threshold amplified spontaneous emission (Fig. 11). Care must be taken, however, in the chosen regime of operation because if the laser is biased such that the excited state becomes significantly populated, the LEF diverges and giant values up to 60 have been observed.[76,77]

The connection between the LEF and the laser linewidth is straightforward. The above-threshold linewidth can be expressed as[66]

$$\Delta\nu = \frac{\left(\Gamma g_{th} v_g\right)^2 \eta_0}{4\pi P_0} h\nu n_{sp}(1 + \alpha^2),$$

where Γg_{th} is the threshold modal gain, v_g is the group velocity, η_0 and P_0 are, respectively, the single facet optical efficiency and output power, $h\nu$ is the photon energy, and n_{sp} is the population inversion factor. From this equation, it is apparent that the linewidth scales with $(1 + \alpha^2)$ meaning
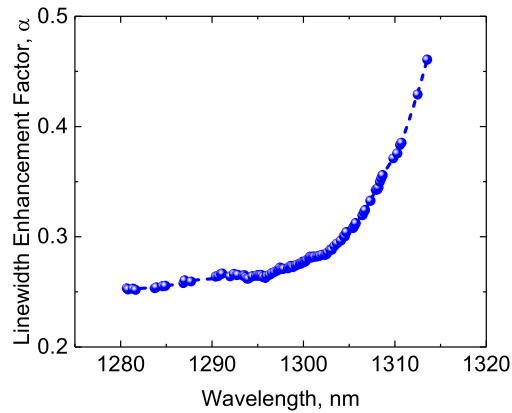
FIG. 11. The below-threshold linewidth enhancement factor, α, is plotted as a function of wavelength for a quantum dot laser on Si showing values well below 1 across the gain spectrum.

that even small reductions in the absolute vale of the LEF will lead to significant reductions in laser linewidth. Furthermore, QD lasers could also have higher output powers yielding additional linewidth improvement.

The possibility of higher output powers in QD lasers comes from their resistance to filamentation. Filamentation is a phenomenon in lasers with positive LEFs and high output powers where the optical mode will begin to deplete carriers in the central region of the waveguide which causes a local increase in the refractive index resulting in self-focusing of the laser beam leading to further carrier depletion and more intense focusing.[72] Ultimately the result of filamentation is that there is an upper limit on increasing a laser's output power by increasing its width. The lower LEF of QD lasers indicates that the local changes in refractive index should be smaller and thus lead to lower filamentation, and if negative LEFs are achieved, then antiguiding would be expected yielding more dramatic improvements in achieving high output powers.[72] Reduced and completely suppressed filamentation in QD lasers has been experimentally demonstrated.[78,79]

The advantages of a low LEF also extend to feedback susceptibility and noise. In any integrated photonic system, and particularly in those using low loss waveguides, undesired reflections will be generated and fed back into the laser cavity. Such feedback can have a destabilizing effect inducing multimode operation or even total coherence collapse depending on the strength of the feedback relative to a critical level defined as[66]

$$f_{crit} = \frac{\tau_L^2 \left(K f_r^2 + \gamma_0 \right)^2}{16 |C_e|^2} \left(\frac{1 + \alpha^2}{\alpha^4} \right),$$

where τ_L is the roundtrip cavity delay, $\left(K f_r^2 + \gamma_0 \right)$ is the damping rate defined by the K-factor and damping offset, γ_0, f_r is the relaxation oscillation resonance frequency, and $|C_e| = \frac{1-R}{2\sqrt{R}}$ is the cavity coupling strength. In addition to the improvements in the LEF, QD lasers also show higher damping rates than QW lasers due primarily to significantly larger K-factors (1 ns for QDs[80] and 0.265 ns for QWs[66]). Experimentally, QD lasers have shown 20-30 dB higher thresholds for coherence collapse than QWs with a threshold of −8 dB having been reported.[81,82] In addition to coherence collapse, optical feedback can induce relative intensity noise (RIN) that degrades the signal-to-noise ratio and will increase the bit-error rate in a PIC.[66] RIN scales with the damping rate, and so the higher K-factor in QDs relative to QWs should lead to reduced sensitivity as was confirmed in direct comparisons where the QD lasers showed 15-20 dB lower sensitivity.[82,83]

B. Semiconductor optical amplifiers

The benefits of switching to QD-based gain media for amplification are multifold and related to the gain and carrier dynamics within the active region and the isolated, independent nature of each individual QD emitter relative to the larger ensemble. The previously described static improvement in achievable output powers due to reduced filamentation in QD lasers translates in an obvious way to

allowing for higher gains, but more subtle improvements exist relating to performance under different modulation formats, simultaneous multi-channel amplification, and nonlinear effects. For a detailed review, see Refs. 84 and 86. Additionally, the inhomogeneous broadening due to QD size fluctuations can be tuned to achieve large gain bandwidths with up to 90 nm having been demonstrated in the E- and S-bands.[87]

The carrier dynamics of QD gain media are very different from their QW counterparts in that the carrier density in the active states is low due to the atom-like nature of the QDs while the carrier density in the separate-confinement heterostructure (SCH) outside the dots is orders of magnitude higher at operating biases. This separation of the carrier density in energy space decouples the gain recovery in QDs from the much slower reservoir repopulation and allows for gain recovery on the picosecond or even femtosecond time scales.[83,88] In QW materials, the carrier reservoir and the gain peak overlap leading typically nanosecond time scales for gain recovery due to the slow process of carrier injection.[88] The decoupling between gain and reservoir carrier densities means that the refractive index can be modulated through direct modulation of the SOA without affecting the amplitude of amplification[89] which has implications for designing efficient, compact optical networks around differential-phase-shift keying (DPSK).[90] Error-free transmission at 25 Gbit/s with an input power level of −5 dBm has been demonstrated.[89]

The independent nature of individual QDs means that the amplification by dots of different transition energies will not be coupled. In QWs, the phenomenon of cross-gain modulation (XGM) is well documented and results from amplification at one wavelength depleting carriers and reducing the amplification at a separate wavelength. In a QD gain medium, simultaneous amplification of multiple signals can be obtained because dots that are resonant with one wavelength will not be resonant with the additional amplified wavelengths to within the limits of the homogeneous broadening of individual dot transitions. Simultaneous amplification of four wavelength channels spaced on a 5-nm grid consisting of one 80 Gb/s return-to-zero (RZ) on-off keying (OOK) signal and three interfering 40 Gb/s non-return-to-zero (NRZ) OOK signals was demonstrated with error free transmission of all channels and <3 dB optical signal-to-noise ratio (OSNR) penalty at −6 dBm of input power.[90] This concept can be extended to apply even within a single subset of dots simultaneously operating from their ground and excited state transitions.[84]

C. Mode-locked lasers

The mechanisms that allow for improved mode-locked lasers (MLLs) when using QD active regions have already been detailed above. The aspects of the discrete density of states that lead to lower thresholds, higher powers, and higher temperature operation will all benefit MLLs in the same manner. Additionally, the gain dynamics that open so many interesting opportunities for QD semiconductor optical amplifiers also mean that the gain and absorber recovery times will be ultrashort for MLLs leading to sub-ps pulse widths. The lower LEF results in less chirping and shorter pulses. The shortest pulses ever demonstrated from an on-chip laser diode came from quantum dot lasers showing 390 fs pulses at 1.31 μm[91] and 312 fs pulses at 1.55 μm.[92] Quantum dot lasers also show reduced amplified spontaneous emission relative to QWs which leads to reduced jitter in MLLs[93] and has allowed for error free transmission at 10 Gb/s from several comb lines in a heterogeneously integrated device.[94] Furthermore, there have been multiple reports of spontaneous mode locking without separate active or passive mode locking sections[95,96] in QD lasers with relatively short pulses (490 fs) and stable mode locking occurring in Fabry–Pérot cavities.[96]

D. Modulators

Modulators based on QD active regions have not been heavily studied. Based on the increased confinement exhibited in QDs and their excitonic nature all the way up to room temperature,[97] one might expect to achieve high electro-optic coefficients and steep absorption edges due to the quantum confined Stark effect.[98] Measurements using InAs QDs for electro-optic modulation at 1515 nm showed a modulation efficiency of <1 V cm with an insertion loss of 3.1 dB/cm and for electro-absorption modulation at 1309 nm, an insertion loss of 30 dB/cm was obtained at 18 V reverse bias.[99] Optical modulation using QDs is an area that still needs more research to determine feasibility. One potential drawback is that the same decoupling between the gain and reservoir that is

so beneficial to amplifiers and MLLs may limit the performance of QD modulators since depleting carriers will require scattering out of the large energy level spacings and prior depletion of the carrier density reservoir. In a QW, these processes can happen simultaneously. One solution would be to add a coupled QW near the QD layers to promote tunneling as a pathway for carrier escape which has seen some success in improving performance of directly modulated QD lasers.[69]

E. Photodetectors

Quantum dot active layers offer promise as photodetectors (PDs) ranging from the near-IR communications bands to the mid-IR. In the near-IR on a native III-V substrate, InAs QDs have been used to fabricate high speed PDs with edge-illuminated responsivity as high as 0.5 A/W (0.6 A/W when accounting for coupling losses) for wavelengths spanning 1510-1630 nm with less than 1 nA of dark current up to −20 V bias and, when pushed into the avalanche regime, showed multiplication factors as high as 12 with 3 μA dark current and a 3-dB bandwidth of 20 GHz.[100] At 1.3 μm wavelengths, QD PDs grown on Si have shown an internal responsivity of 0.9 A/W and a dark current of less than 0.8 nA at −1 V (as shown in Fig. 12) bias with a capacitance-limited 3-dB bandwidth of 2.3 GHz.[101] For mid-IR applications, QDs are promising for their ability to detect at normal-incidence their low dark current and high temperature operation. See Ref. 102 for a detailed review of the history of the field and motivations. The low dark currents and high temperature operation are a direct result of the high energy level separations within the QDs that suppress thermionic emission.

F. Quantum computation

Silicon photonics already shows promise as a platform for quantum computation,[103] and quantum dots show promise as sources of entangled single photons compatible with proposed computation schemes.[104] Recently, there was even a demonstration of single photon filtering and multiplexing in a silicon photonic circuit with integrated InAsP quantum dots.[105] Such research is obviously still in the fundamental stages, but if QDs are already being integrated in Si photonics for classical applications with established processes, then it makes sense to grant them extra consideration in designing future quantum computation platforms.

G. Defect tolerance

Probably the most important advantage that QDs have over QWs is their tolerance to crystalline defects. This tolerance to crystalline defects is the sole factor that has even allowed heteroepitaxial growth to be considered as an integration platform. As previously described, heteroepitaxy generates large densities of threading dislocations that act as nonradiative recombination centers that grow with device operation. Due to the limited in-plane diffusion lengths described previously, QD materials are far less sensitive to the presence of these defects than are QWs. A detailed study of the effects on lasers using simultaneously processed QD and QW materials showed that while all the QW devices on Si
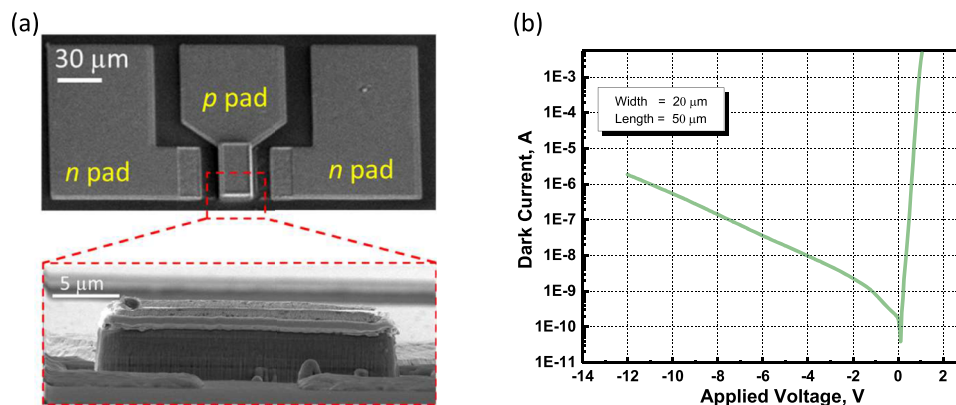

FIG. 12.   (a) Scanning electron micrograph of an edge-coupled quantum dot photodetector on Si. (b) Dark current as a function of applied bias. Adapted from Ref. 101.
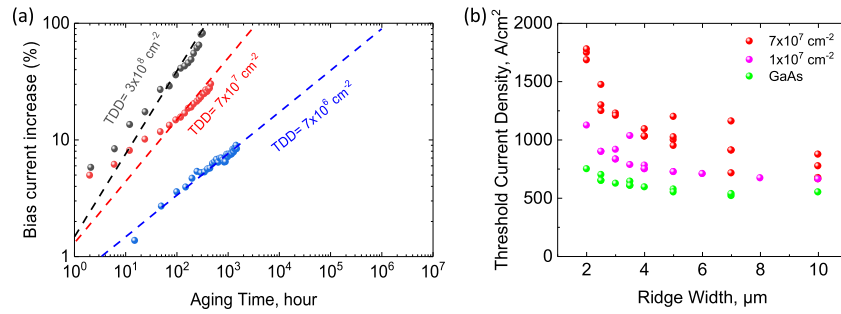
FIG. 13. (a) Extrapolated mean-time-to-failure for quantum dot lasers grown on Si with varying dislocation density.[109] (b) Threshold current normalized to the number of quantum dot layers for varying dislocation density.

failed to lase, the devices with QDs lased with low thresholds and high output powers.[38] Additionally, the photoluminescence of the as-grown material showed only a 20% reduction in intensity for the QDs as compared to a 90% reduction for QWs. The reduced sensitivity to defects has also allowed for commercially promising extrapolated lifetimes to be realized in epitaxial lasers at >10 000 000 h.[51] Figure 13(a) shows the extrapolated mean-time-to-failure, defined as a doubling of the threshold current, versus aging time for lasers with varying dislocation density. Figure 13(b) shows the static thresholds normalized to the number of quantum dot layers for devices grown on Si with varying dislocation density.

These benefits extend to other components besides lasers, with near-IR[101] and mid-IR[110] photodetectors having been demonstrated epitaxially on Si using QDs with performance levels comparable to native substrate devices. Heteroepitaxial growth is also not the sole source of defects in material. For space applications and metrology in certain environments, radiation damage can be a concern, and QD lasers have shown a high degree of tolerance to such damage.[111,112]

IV. CONCLUSIONS AND NEXT STEPS

At this point, III-V lasers with quantum dot active regions are showing promise for commercial viability. Lasers are arguably the most sensitive photonic component to material defects, and they have been demonstrated through epitaxial growth to match the performance of heterogeneously integrated devices in terms of static energy efficiency and output power. Their lifetimes are also entering the realm of commercial relevance with high power testing underway to prove their viability. The devices are being grown on pieces from industry standard 300 mm Si wafers, the same as would be used in commercial CMOS foundries or to make SOI wafers for silicon photonics. Further work remains to be done to reduce the dislocation density even further for improving device performance and to push the limits of the laser footprint. In order to achieve the goal of attojoule optoelectronics for on-chip interconnects, subwavelength components may be necessary[106] which would require the use of plasmonic cavities. Such structures have been demonstrated in VCSEL implementations[107,108] and could theoretically benefit similarly through the use of a quantum dot gain medium as have traditional semiconductor lasers.

So, what is missing? For one, the vast majority of research into epitaxial integration has focused on lasers. More work needs to be done to explore the possibilities of amplifiers, photodetectors, and modulators to prove their performance. Additionally, more work needs to be done to integrate quantum dot active regions with each of these components. We have outlined above the numerous advantages presented by QD active layers for devices beyond simple multi-mode ridge-waveguide Fabry–Pérot lasers, but many of these theoretical advantages still need to be experimentally demonstrated and optimized. Another missing piece is that current results and efforts all focus on photonic devices at 1310 nm and 1550 nm. There are many applications that could benefit from both longer and shorter wavelengths. Work is ongoing in this area but lags significantly behind the optical communications wavelengths. Notably, in the past year, the first results of CW operation of antimonide based lasers was demonstrated at room temperature on Si opening the door to longer wavelengths in the IR,[113] and

room temperature CW operation was also achieved in the ultraviolet spectrum using nanowires.[114] Additionally, the rise of self-driving cars is motivating the pursuit of lasers at eye-safe and atmospheric transparency wavelengths around 1230-1250 nm. In particular, LIDAR for self-driving cars will benefit from the narrow linewidths, low power consumption, low cost, and long device lifetimes afforded by epitaxial quantum dot devices on Si. Additionally, these desired wavelengths fall in the range that can easily be achieved using In(Ga)As quantum dots on GaAs. The final missing piece is determining the most suitable method for epitaxial integration. The buffer thicknesses in the previously reported results are all in excess of 2 μm[37,40–42,50–52] making coupling to any sort of waveguide structure on the Si substrate difficult, but the methods outlined above could present viable alternatives.

In summary, photonic integration has come a long way since the development of heterogeneous integration. Bonding III-V materials to silicon enabled new functionalities and commercial viability not previously attainable using purely III-V materials or Si and Ge. Innovations in the field have spawned companies and launched mass-production product lines for data center applications. Going forward, there are substantial opportunities to build upon what has been achieved through heterogeneous integration to both improve performance and reduce cost. Quantum dots present incredible new opportunities for performance improvements and high-density integration that will ultimately enable chip-scale photonic integration. These advantages can be obtained without changing the heterogeneous integration platform by simply changing out the bonded QW epitaxial material for QD structures. However, the future of low cost photonic integration must involve epitaxial integration. The cost of III-V substrates and limited scalability due to wafer sizes ensure that heterogeneous integration cannot compete with epitaxial integration when the performances are equal, and for lasers at least, they are already nearly there, already exceeding in many ways the static performance of bonded lasers and rapidly closing the gap in terms of reliability and more advanced functionality (ultra-narrow linewidth, tunability, high power, etc.). The key next step will be demonstrating the platform that allows for epitaxial integration with the functionality, complexity, and integration density currently being achieved in heterogeneous silicon photonics.

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