Photonic Integration With Epitaxial III–V on Silicon

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(Invited Paper)

***Abstract*—We present a brief overview of the various leading platforms for photonic integration. Subsequently, we consider the possibility of a photonic integrated circuit platform utilizing epitaxially grown III–V material on silicon—without the need for wafer bonding, or an externally coupled laser. Finally, a techno-economic analysis contrasting the aforementioned platforms will be presented.**

***Index Terms*—Integrated optoelectronics, quantum dots, wafer scale integration.**

I. Introduction

PHOTONIC integrated circuits (PICs) are expected to become a billion dollar market around 2020 as shown in Fig. 1, currently fueled primarily by telecom and datacom applications. Although PIC technology is primed to serve other growth markets such as automotive, consumer devices, and the internet of things (IoT), the cost of PIC technology must continue to fall to achieve broader commercial viability. Historically, the development of individual devices on various disparate material platforms preceded their co-integration on a common substrate or platform. As a result, there now exists several different platforms for photonic integration, each with their own trade offs in performance and cost. We will present a brief overview of the mainstream platforms, and subsequently examine the possibility of photonic integration with epitaxially grown III-V material on silicon. This approach will then be compared and contrasted with the commercially mature platforms for photonic integration in terms of cost and performance.

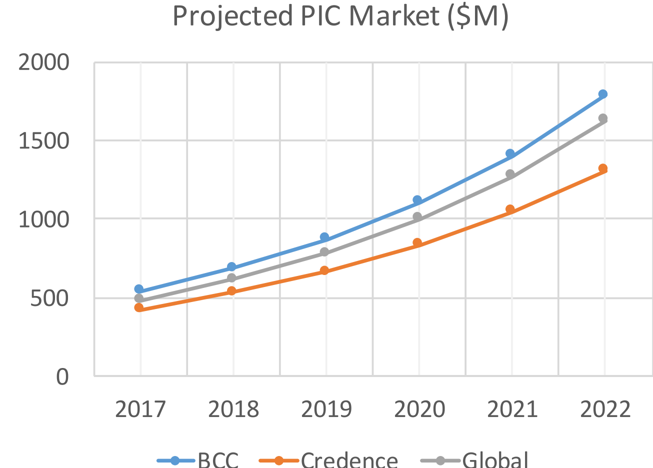

Fig. 1. Market size projects for Photonic Integrated Circuits (PICs) utilizing publicly available data from three separate sources: BCC Research, Credence Research, and Global Industry Analysts. All three are projecting a compound annual growth rate between 25–28%.

II. Commercial Platforms for Photonic Integration

In the sections below, we briefly review the leading platforms for photonic integration, and in each case will present a use case which exemplifies the unique advantage of each platform. This review is not meant to be exhaustive. There now exist many different material platforms for photonic integration, such as doped silica, chalcogenides, germanium on silicon, polymers, $LiNbO_3$, etc., each with their own unique strengths and shortcomings, and each meriting no less interest than the other. The scope of this text will focus on ones that are particularly well suited for application in the mainstream datacom and telecom wavelengths - which have been the primary application pull for photonic integrated circuits and will likely continue to serve this role in the near future. We will begin with the most mature platforms which are based on Si_3N_4, InP, monolithic silicon photonics, and heterogeneous integration, before examining the newly emergent one based on epitaxially grown III-V materials on silicon - hereafter also referred to as 'heteroepitaxial integration'. For ease of comparison, simplified cross-sectional representations of the key technological components, configurations, substrate choice, and substrate size for each platform are shown in Fig. 2 as a starting point of our discussion.

A. Si_3N_4

The silicon nitride platform is a purely passive platform which utilizes a waveguide core of Si_3N_4 typically clad by SiO_2 (see Fig. 2(a)). This combination of materials has a relatively low index contrast ($\Delta n \sim 0.55$), which reduces sensitivity to fabrication imperfections of its waveguides as well as scattering losses and reflections relative to the much higher index contrast of silicon/silica waveguides [1], [2]. Si_3N_4 as an integration platform is mostly known for its exceptional passive performance, with

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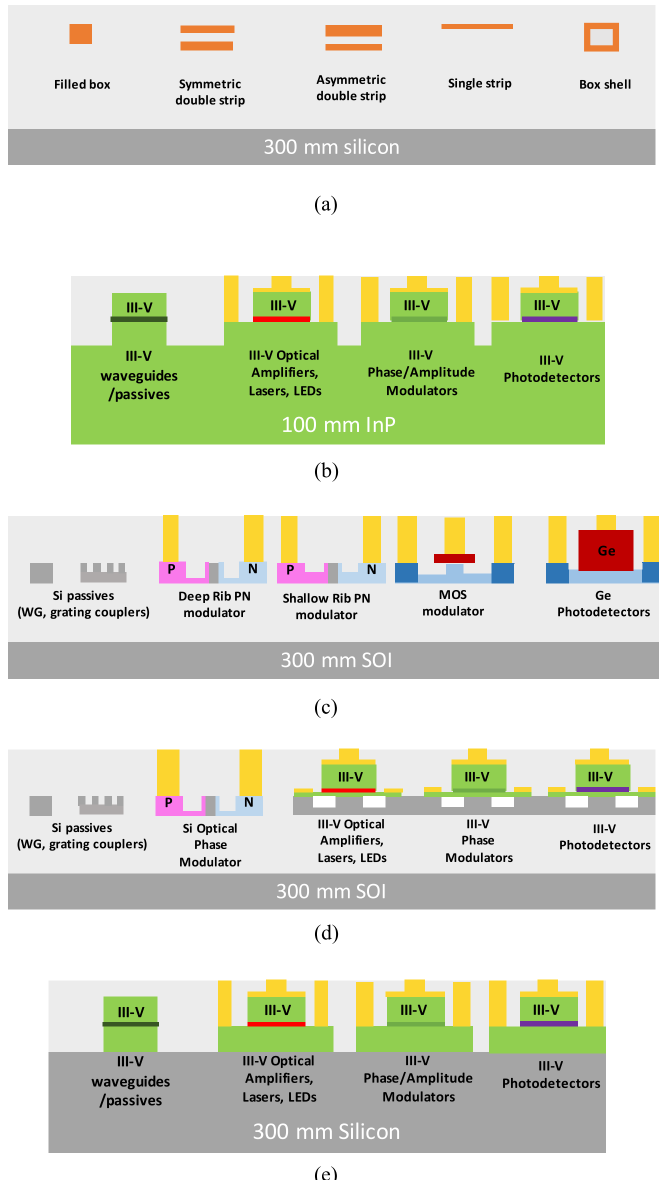


Fig. 2. Simplified representations of various platforms for photonic integration: (a) Si_3N_4 passive waveguides (TriPlex); (b) InP; (c) Monolithic silicon photonics; (d) Heterogeneous integration; (e) Epitaxial III-V on silicon (heteroepitaxial integration).

very low propagation loss down to 5×10^{-4} dB/cm [3]. This has enabled, for example, on-chip resonator Qs of 81 million [4]. One caveat to achieving such low losses is that it generally requires annealing over 1000 °C to drive out hydrogen, therefore limiting the integration capabilities of the platform [2]. This can be avoided if non-hydrogen sources are used for its fabrication (such as deuterium or chlorides).

The Si_3N_4 platform is also compatible with a wide span of wavelengths from the visible to the mid-infrared. Waveguides constructed on this platform can support a large, weakly guided mode with a significant fraction of power contained in the evanescent field (as compared to the smaller and highly confined modes in silicon waveguides with a much higher index contrast of $\Delta n \sim 2.05$). The aforementioned properties make the Si_3N_4 platform ideal for a variety of sensing applications [1]. The typically large mode sizes supported also makes it an attractive platform for spot-size-converters and fiber couplers [3]. These traits, along with the fact that spurious reflections are typically more than 10 dB lower in magnitude in Si_3N_4 based waveguides compared to their silicon-on-insulator (SOI) counterparts, makes Si_3N_4 an appealing platform for a photonic interposer. Photonic integrated circuits using Si_3N_4 are being offered by LioniX through its TriPleX platform [3] as well as LIGENTEC. A comprehensive review of the TriPleX platform can be found in [3], and an excellent overview of Si_3N_4 versus SOI can be found in [5].

B. InP

Photonic integration on InP, whereby InP and related ternary or quaternary epitaxial stacks are grown on a common InP substrate for the subsequent fabrication of optoelectronic devices, provides a platform for complete monolithic integration of passive and active functions (see Fig. 2(b)) [6]. Active and passive interfaces can be coupled with very low loss (as low as 0.1 dB) via vertical twin or single guide growths, quantum well intermixing, and/or butt-joint regrowth [6]. The most prominent foundry example is the joint European platform for InP-based components and circuits - or JePPIX. This consortium offers foundry services through Oclaro, the Fraunhofer Heinrich Hertz Institut (HHI) in Berlin, and the COBRA spinoff company SMART Photonics, located in Eindhoven. The JePPIX foundries have been actively offering multi-project wafer (MPW) runs.

Photonic integration on InP is a mature technology, and is the workhorse of traditional performance focused market segments such as long-haul and coherent communications. The distinguishing feature of InP PICs are exceptional performance of active components such as the photodetector, modulator, and in particular the laser which can be waveguide coupled to the rest of the PIC with very low loss. Infinera, Finisar, and Lumentum all offer products based on InP PICs within this space. The latest development from Infinera is a 14-channel coherent transmitter PIC with over 4.9 Tb/s of capacity [7]. For a comprehensive review of InP photonic integrated circuit technology, the reader is referred to excellent reviews elsewhere [6], [8].

C. Monolithic Silicon Photonics (with External Laser or no Laser)

Silicon-on-insulator or SOI is the natural platform for mainstream silicon photonics, whereby the majority of optical functions are derived from devices constructed from the silicon device layer, while selective area epitaxy of germanium is used for photodetection (see Fig. 2(c)). Germanium has been proposed as a possible light source for monolithic silicon photonics due to its availability in CMOS fabs today. While a germanium laser monolithically grown on silicon has been demonstrated, it is not technically viable for commercial use given that the required threshold current density is more than 1000× higher than III-V based lasers, and low operating power is a key requirement for most applications [9].

Many foundries today offer a relatively complete suite of technologies based on this platform, including the American Institute for Manufacturing Integrated Photonics in the U.S. (AIM Photonics), IMEC, GlobalFoundries, Institute of Microelectronics (IME), STMicroelectronics, Taiwan Semiconductor Manufacturing Company (TSMC), and TowerJazz, among others. However, an integrated on-chip laser is missing from these processes. Products based on this platform are being commercialized by companies such as Acacia, Luxtera, Cisco, and AIO Core, whereby an external III-V laser is coupled to the silicon photonic chip as the light source. This is viable when one or a few lasers are required, but becomes too expensive and yield limiting when an array of sources are needed such as in advanced wavelength division multiplexed (WDM) systems, which are increasingly required for datacom and telecom applications. The externally coupled laser is typically housed in a separate package from the silicon PIC, with coupling facilitated via external lenses or a fiber pigtail. Alternatively, the laser may be butt-coupled to the silicon PIC and light edge-coupled through spot size converters.

The high index contrast of the Si/SiO_2 system allows for tight waveguide bends and compact sized devices. However, this in turn means that unwanted reflections are also likely. Another hallmark of monolithic silicon photonics is the very high yield of a mature silicon based process, allowing for integration of a large number of devices with unprecedented complexity. An example which captures both of these points is the demonstration of a large scale two dimensional phased array via the integration of 4,096 optical nanoantennas, all within a footprint of 576 μm^2 [10]. For an excellent overview of photonic integrated circuit technology focusing on monolithic silicon photonics technologies, see [11].

D. Heterogeneously Integrated Silicon Photonics

Heterogeneous integration is the process of combining III-V functionality with monolithic silicon photonics via wafer-bonding of the two materials together (see Fig. 2(d)). With this approach, one can take advantage of the advanced silicon based processing in a monolithic silicon photonics process, but also utilize III-V materials for on-chip active optical functionalities such as gain, photodetection, and phase/amplitude modulation. As an added benefit, integration of multiple diverse materials on a single PIC connected by a common silicon waveguide is possible. A number of foundries such as CEA-LETI and IME are currently exploring this process. Intel has recently released products based on this technology, while Juniper Networks (through its acquisition of Aurrion) and Hewlett Packard Enterprise (HPE) are actively investing in the technology as well.

Heterogeneous integration presents opportunities for the realization of novel device architectures with enhanced performance that are otherwise unattainable using a pure monolithic platform alone. Some prominent examples of this are the achievement of ultra-narrow linewidths from a heterogeneously integrated III-V laser coupled to a high-Q silicon cavity [12], and integrated waveguide photodiodes with record output power and bandwidth achieved by engineering the hybrid III-V/silicon mode to smooth out the absorption profile [13]. Compared to monolithic III-V PICs or lasers, heterogeneously integrated active components have no significant incident photon density on exposed III-V facets or mirrors, minimizing III-V facet related degradation mechanisms and lending to improved reliability of the active devices. The most complex heterogeneously integrated photonic integrated circuit demonstrated is an $8 \times 8 \times 40$ Gbps network-on-chip with 2.56 Tbps of data capacity [14]. A recent review of heterogeneous integration can be found in [15].

III. Photonic Integration with Epitaxial III-V on Silicon

Epitaxial growth of III-V compound semiconductors such as GaAs and InP on silicon for the fabrication of photonic devices is a research area that has been pursued for many decades, motivated by the potential to integrate traditional CMOS logic with the superior RF and optical properties of III-Vs, and more recently by silicon photonics. This approach has also been referred to as 'heteroepitaxy' or 'direct (hetero-epitaxial) growth on silicon'. It bears mentioning that as of this writing, none of the commercial silicon photonics foundries offer a true integrated on-chip light source as part of their process. In this paper we give consideration to utilizing epitaxial growth of III-V materials on silicon as the basis for a monolithic photonic integration platform with complete on-chip active and passive functionalities - including the laser - which presents a compelling cost advantage compared to all of the aforementioned approaches.

There are two potential variations of this approach for the fabrication of PICs, which can be distinguished by the choice of passive circuitry to be used. One option is to couple light generated in a III-V section to passive photonic circuitry in silicon on an SOI substrate. This may be accomplished, for example, as an alternative version of heterogeneous integration by bonding III-V active material which has been grown on silicon instead of III-V substrates to SOI. Alternatively, one can pursue direct growth of III-V materials onto patterned SOI and integrating as-grown III-V components with the silicon device layer via selective area growth and buttcoupling. These two approaches have been detailed previously [16], [17], and will not be discussed in depth here.

For this paper, focus is given to an alternate approach whereby the entire PIC is self-contained within epitaxially deposited III-V layers on silicon (see Fig. 2(e)). In this case, III-V layers will be used for both active devices as well as passive circuitry (instead of silicon as in the former case). This would be analogous to the case of photonic integration on InP, with a major distinction being that the III-V layers are grown on a much cheaper and larger silicon substrate, whose main purpose is to facilitate scalable manufacturing with more modern and advanced processing, packaging and testing equipment. Multiple bandgaps may be obtained from selective area growth, regrowth steps or intermixing as is done in the case of photonic integration on InP.

Integrating III-V materials on silicon by epitaxial growth is an active area of research, pursued both within academia as well as commercially by AIM, IMEC, IBM, and NTT, among others. Performance and reliability issues have thus far

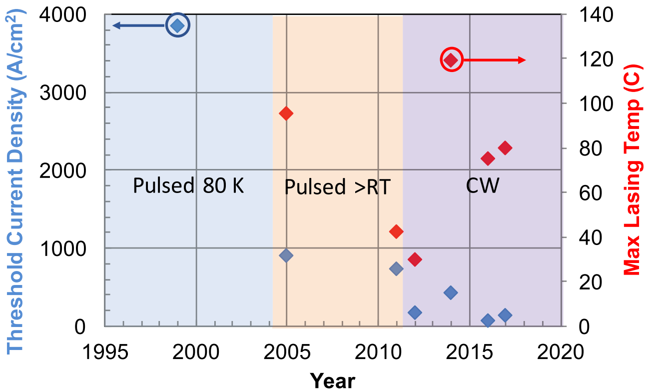


Fig. 3. Evolution of InAs/GaAs quantum dot lasers epitaxially grown on silicon in terms of threshold current density reduction and increase in maximum lasing temperature. University of Michigan was the first to report operation of a quantum dot laser grown on silicon lasing in pulsed operation at 80 K in 1999 [18]; UCSB reported the highest room temperature CW output power and lasing temperature to date in 2014 [19]; and UCL reported the lowest room temperature threshold current density in 2016 [20].

relegated the field to the continual improvement of material quality and individual device performance, without much discussion or consideration for the development of full photonic integrated circuits. However, a number of recent breakthroughs have significantly de-risked the technology from a performance standpoint, warranting discussion for more advanced photonic integration. These recent developments include incredible leaps in device performance and reliability of the light source, as well as demonstration of other optoelectronic devices from epitaxial III-V on silicon material, as described in the sections below.

A. Maturation of the Light Source

The laser is the most important component of a photonic integrated circuit, as it generates the light signal which is the basis for all photonic functionality. In optical transceivers, the power consumption of the laser comprises a significant fraction of the total transceiver power budget. Downstream system characteristics will place requirements on the necessary performance characteristics of the upstream light source, and conversely any inefficiencies or performance impairments of the laser will trickle downstream and must be dealt with or compensated for. Likewise in photonic sensors, the purity and strength of the laser signal used for sensing dictates the ultimate sensitivity of the system. Loosely speaking, for most datacom applications it is desirable for the laser to achieve efficient continuous wave operation at room temperature and above (up to 80 °C), with low thresholds (a few to tens of mA), and reasonable output powers (1–10 mW).

There are various approaches to monolithically grow light sources on silicon, however by far the most successful approach has been using III-V quantum dot lasers directly grown on silicon [17]. In recent years, the performance and reliability of quantum dot lasers epitaxially grown on silicon have begun to approach that of native substrate levels. Fig. 3 illustrates the progress in threshold current density reduction as well as maximum lasing temperature improvement over the years for Fabry-Perot type lasers with a quantum dot active region epitaxially grown on silicon. As is evident in the figure, the technology has made great strides from the first demonstration of cryogenic lasing in pulsed operation in 1999, to the first continuous wave (CW) operation demonstration in 2012, to rapid reductions in threshold current density and increases in maximum lasing temperature recently (~60 A/cm^2 and ~120 °C, respectively).

B. Demonstrating CMOS Compatibility

One criticism of the heterepitaxially integrated lasers described in the previous section was that it relied on the use of special silicon substrates that employed a slight miscut angle from the (001) orientation. The original reason for the use of miscut substrates is that the double-atomic steps induced from the miscut angle are favorable for the suppression of the formation of anti-phase domains resulting from the growth of the polar III-V material on the non-polar silicon surface. As traditional CMOS fabs all use on-axis (001) oriented wafers, use of the miscut silicon wafers was deemed to be incompatible with traditional CMOS processes. This has been proven to be a non-issue recently as the field has migrated to the use of CMOS compatible standard on-axis silicon substrates using novel methods to solve the anti-phase domain problem, obviating the need for miscut substrates. These approaches range from direct nucleation using conventional two-step growth methods [21], the use of a thin GaP buffer layer [22], and patterned growth on exposed {111} v-groove facets of silicon [23]. The most recent results from on-axis devices - employing an GaP interlayer - now show room temperature continuous wave threshold currents as low as 9.5 mA, single-facet output powers of 175 mW, ground state lasing up to 80 °C, and wall-plug-efficiencies as high as 38.4%, all obtained with as-cleaved facets [24]. Ultimately, this technology is agnostic to what the initial buffer approach is, and thus whichever approach yields the best material quality should be used.

C. Demonstrating Reliable Operation

Historically, GaAs based lasers have been susceptable to defect related failure modes. Indeed, initial demonstrations of heteroepitaxially integrated lasers showed very poor lifetimes, with the longest lasting no more than 200 hours [30]. Fig. 4 shows the rapid improvements in device lifetime which have been achieved since in recent years, with roughly 100x improvements in between each of the last two reports. A key observation is the fact that all of the best reported lifetimes employ quantum dot active regions. A sample of the most recent aging results at 35 °C and at twice the threshold current density (roughly 400–1000 A/cm^2 and ~3–6 mW of output power depending on device geometry) are shown in Fig. 5(a) [32]. The extrapolated mean time to failure, as defined by doubling of the threshold at the aging condition, are now in excess of 10,000,000 hours [31], [33]. Fig. 5(b) illustrates the rapid pace of improvement in lifetime obtained in the course of 1 year between three generations of devices: 4 orders of magnitude improvement in mean time to failure was realized via two orders of magnitude reduction in the defect density. Commercial use will require qualification at

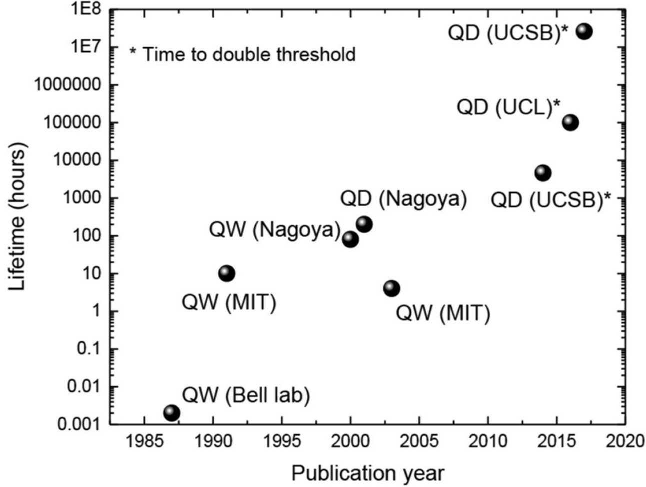


Fig. 4. Demonstration of the improvement in lifetime (time to doubling of lasing threshold or actual failure) of GaAs based lasers epitaxially grown on silicon. The most recent lifetime gains have been through a combination of using quantum dot active regions and defect engineering. References: 1987 [25], 1991 [26], 2000 [27], 2001 [28], 2003 [29], 2015 [30], 2016 [20], 2018 [31].

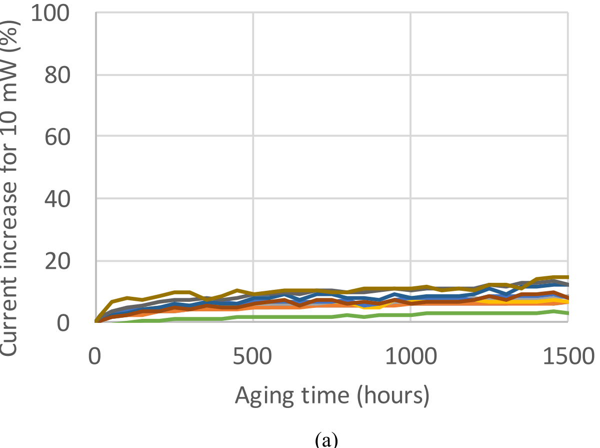
higher temperatures as well as applied current (densities) - e.g., 80 °C or above for datacom at current densities corresponding to 10–20 mW of on-chip power - and this is currently underway. Preliminary aging studies of InAs/GaAs quantum dot lasers grown on silicon at 60 °C and at twice the threshold current density (∼6–8 mW of output power) have yielded MTTFs on the order of 65,000 hours, a promising initial result [31].

We note that there have been previous reports of InP quantum well lasers grown on silicon with good lifetime [35], but they required III-V buffer thicknesses between 10–15 μms prior to the growth of the laser structure itself [36]. However, the prospect of improved reliability using InP based compounds epitaxially grown on silicon is worth investigating. We note, however, that in the case of GaAs based lasers epitaxially grown on silicon, the prevailing evidence as shown in Fig. 4 indicates that quantum well based active regions will simply not work, and that quantum dots are key to high efficiency and high lifetime lasers [17], [30].

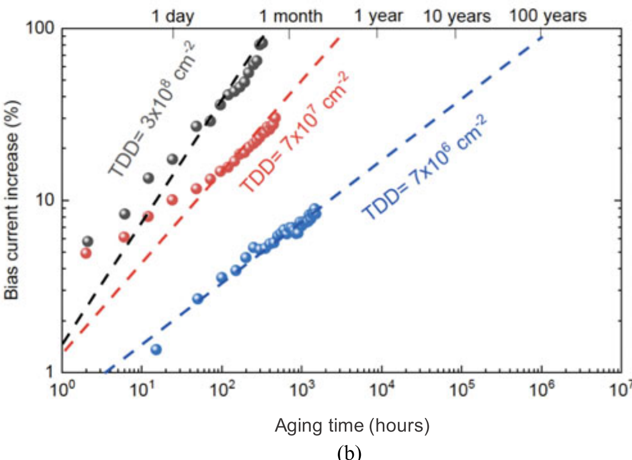
D. Other Ingredients for Photonic Integration

In addition to light generation, other components for signal shaping, regeneration, guiding, and detection will be needed to form the basis of a photonic integrated circuit. More sophisticated laser structures will also be needed. A brief overview of other such recently reported PIC ingredients fabricated from III-V material epitaxially grown on silicon is given below.

1) DFB and Microring Lasers: While the emphasis for epitaxial III-V on silicon research has thus far been on static performance of Fabry-Perot type lasers, their performance has sufficiently improved to warrant investigation into more advanced laser configurations, which will be needed for most practical applications. Recently, micro-ring configurations employing O-band quantum dot active material epitaxially grown on silicon have demonstrated sub milliamp room temperature continuous-wave thresholds and lasing up to 100 °C [37]. Such compact



(a)



(b)

Fig. 5. (a) 1500 hour constant current aging results at 35 °C and twice the threshold current of the latest heteroepitaxially integrated 1.3 μm InAs/GaAs quantum dot lasers on silicon [32], [33]. (b) Progress in lifetime improvement (4 orders of magnitude) within one year between three generations of devices due to defect reduction [31], [34]. Each data point is an ensemble average of the required bias current increase to maintain 10 mW of output power during aging (constant current stress at twice the threshold current at 35° (c) for a batch of similarly constructed devices.

geometries are ideal for high density and low-power photonic integration.

In a separate work, distributed feedback (DFB) quantum dot laser arrays directly grown on silicon were reported with side mode suppression ratios as high as 50 dB and spanning a wide wavelength range of 100 nm centered around 1.3 μm, relevant for WDM applications [38].

Finally, IMEC has reported optically pumped room temperature InP [39], [40] as well as InGaAs/GaAs [41] DFB laser arrays directly grown on (001) silicon. Notable to this work is the fact that the lasers were grown on 300 mm silicon substrates using the same selective area growth process which was used to produce III-V FinFETs on silicon, an important proof of concept for foundry compatibility and scalable manufacturing.

2) Quantum Dot Mode Locked Lasers: A single-section mode locked 1.3 μm InAs/GaAs quantum dot laser grown on silicon has been reported. The device achieved passive mode-locking under DC bias at 31 GHz with a pulse width of 490 fs

and a 3 dB RF linewidth of 100 kHz [42]. The single-section mode-locking is attractive for its simple operation compared to multi-section designs as well as lower overall cavity loss by virtue of eliminating the use of saturable absorbers.

3) Quantum Dot Photodetectors: Since quantum dot based lasers epitaxially grown on silicon appear to be the most viable light source for heteroepitaxial integration, being able to use the same material for photodetection is desirable. Heteroepitaxially integrated quantum dot waveguide photodetectors operating in the O-band have been reported with an internal responsivity of 0.9 A/W and dark current of less than 0.8 nA at −1 V (and 4.8 nA at −3 V) [43]. Most notably, a proof-of-principle on-chip photodetection was demonstrated by using a waveguide quantum dot photodetector to detect free-space coupled light from a nearby microring laser, both heteroepitaxially integrated on the same chip.

4) Bulk Photodetectors: Both p-i-n (PIN) and modified uni-traveling carrier (MUTC) surface normal photodiodes have been fabricated from InAlGaAs/InP material epitaxially grown on bulk silicon substrates. The reported devices have very low dark current of 10 nA at −3 V for 30 μm diameter device, corresponding to a dark current density of 1.3 mA/cm^2 [44]. The responsivity, 3-dB small signal bandwidth, output power, and third-order output intercept point (OIP3) were 0.76 A/W (at 1550 nm), 9 GHz, 2.6 dBm, and 15 dBm, respectively [45]. In another report, waveguide and normal incidence high speed InGaAs/InP photodetectors were selectively grown on the silicon handle wafer of a SOI substrate by MOCVD [46]. The measured 3-dB bandwidth were 15 and 14 GHz for the normal incidence and waveguide devices, respectively. Open eyes diagrams (non-return-to-zero) were also measured at 20 Gb/s for both device types biased at −5 V [46].

5) Modulators: In principle, both electro-absorption and electro-optic modulators can be fabricated using hetero-epitaxial integration as it makes full use of the properties of III-V semiconductors. Electro-optic phase and amplitude modulators have been recently demonstrated, fabricated from GaAs/AlGaAs layers epitaxially grown on silicon. Intensity modulators with 4-mm long electrodes have V-π of 3.59 V corresponding to 1.44 V-cm modulation efficiency [47]. The modulation efficiency reported is for 1.55 μm, but the device is just as capable of operating at 1.3 μm. For comparison, typical modulation efficiencies of silicon photonic carrier depletion modulators are around 2 V-cm [11], while native InP electro-optic modulators can be around 1 V-cm or less depending on design [6].

In an earlier work, an $In_{0.5}Ga_{0.5}As$/GaAs quantum dot laser co-integrated via free-space groove coupling with a regrown $In_{0.2}Ga_{0.8}As$/GaAs quantum well electro-absorption modulator on silicon have also been reported, with 45 and 100% modulation depth at −3 and −5 V biases, respectively [48]. These devices operated near 1 μm but the wavelength can be easily shifted to 1.3 μm during material growth.

E. Remaining Challenges

The prospects for photonic integration via epitaxial growth on silicon are bright, but much remains to be done to propel it to the market place. Here we identify a few key remaining challenges.

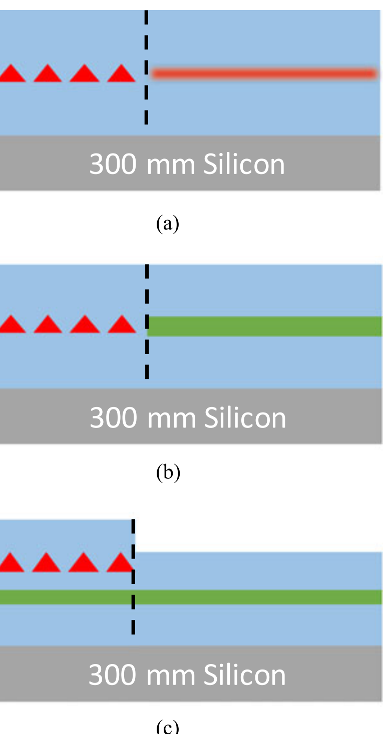


Fig. 6. A few examples of possible approaches to achieve active-passive integration (assuming a quantum dot light source): (a) quantum-dot intermixing; (b) etch and regrowth; (c) offset or dual quantum dot/wells.

1) Active-Passive Coupling and Co-Integration: The photonic components developed from epitaxially grown III-V on silicon highlighted above are for the most part all discrete devices, some with different active region material. Low loss active-passive coupling and advanced co-integration of multiple active devices (e.g., laser plus modulator and photodetector) remains to be demonstrated. This can be achieved by regrowth, intermixing, dual or offset quantum well/dots, evanescent vertical or lateral coupling, grating coupling, or any of the other techniques used for photonic integration on InP - as the main difference here is simply the choice of a substrate (InP versus silicon) [6], [49]. As was noted previously, this approach to photonic integration is relatively agnostic to what the initial buffer approach is for nucleating III-V on silicon (i.e., GaP, Ge, patterned growth, etc.), allowing whichever approach that yields the best material quality to be chosen as the starting point for a virtual substrate.

A few of the possible approaches for co-integration of multiple photonic components are illustrated in Fig. 6. Each of these approaches will have their own set of unique challenges: for example, uniformity of each process (intermixing vs regrowth); performing each process with a thermal budget that does not lead to significant dopant diffusion or degradation of the existing material/active region; high quality selective area growth without significant misalignment of the waveguides, gaps in-between, or nucleation of new defects. In some instances, lessons from photonic integration on InP may be leveraged (e.g., design

trade-offs of different integration schemes), while for others new techniques will need to be developed for challenges unique to this process (e.g., low temperature regrowth to preserve quantum dot quality).

2) Reliability: The required minimum reliability standards are somewhat specific to the application. For example, operating lifetime requirements in datacenters may be more relaxed compared to the needs of say automotive LIDAR due to differences in expected replacement cycles and ease of redundant provisioning to mitigate component failures on a system level. Ultimately, the more demanding applications that would require driving photonics to more intimate levels of integration with electronics would necessitate high performance and operating lifetimes at elevated temperatures where more failure modes may be activated and degradation is accelerated. However, a clear path towards reliable light sources is now in place, through a combination of defect reduction in the template, and device physics engineering. Other devices such as modulators and photodetectors will have a different set of reliability standards that need to be addressed, and specific reliability studies dedicated to each case should be conducted as well. However, degradation rates for devices that operate under reverse bias such as photodetectors and certain modulators are typically much slower compared to devices operating under forward bias such as lasers and amplifiers [50]. Reliable operation for such other devices should also be possible by leveraging the same defect reduction techniques for the template growth along with additional innovations specific to each device structure where necessary.

3) Wafer-Scale Growth and Yield: The true potential of photonic integration via epitaxial III-V on silicon is in the economies of scale from the cheap and large area 300 mm silicon substrates. However, the epitaxially grown III-V material is thermally mismatched with the silicon substrate, which could result in cracking, wafer bow, and other yield issues during blanket deposition. This can be mitigated through selective area growth (as demonstrated by IMEC) or thermal stress engineering. The demonstration of large area blanket GaN-on-Silicon growth for power electronics and LEDs proves that these issues are an exercise in engineering, and some of the lessons there can be leveraged: e.g., designing thermal-stress matched epilayers and other techniques for achieving low wafer-bow, crack-free grown on large area silicon substrates [51]).

A key advantage of silicon photonics is the excellent yields afforded by a mature silicon process - and this is an area where III-V processes have traditionally lagged behind. However Infinera has demonstrated that continuous yield improvement and manufacturing defect reduction for their III-V process follows a similar learning curve as for silicon electrical integrated circuits, with modern day wafer yields for InP PICs in the high 90%s [8]. Furthermore, processing yield tends to scale better with larger wafer size due to more precise wafer leveling and advanced lithography tools, which will be a key distinction between heteroepitaxial integration and photonic integration on InP. Therefore, there is no reason to believe that high manufacturing yields cannot be obtained for heteroepitaxial integration, although the aforementioned issues with wafer-scale growth and yield must first be overcome in order to take full advantage of the higher precision and throughput processing tools available for larger wafers.

TABLE I
SUBSTRATE MATERIALS REQUIRED FOR EACH INTEGRATION PLATFORM

	III-V	SOI	Si
InP	x		
Monolithic SiPh	x	x	
Heterogeneous Integration	x	x	
Heteroepitaxial Integration			x

TABLE II
SUBSTRATE SIZES AND COSTS

	GaAs	InP	SOI	Si
Typical diameter (mm)	150	150	300	300
Estimated cost ($/cm^2)	1.65	4.55	1.3	0.2

Adapted from [16].

IV. Techno-Economic Merit

In this section, we will draw techno-economic comparisons between monolithic silicon photonics with an external laser, heterogeneously integrated silicon photonics, InP photonic integrated circuits, and photonic integration employing epitaxial growth on silicon (assuming a quantum dot based light source). SiN PICs will be omitted due to it being mostly a passive platform without active functionality, though we should note it can be hybrid integrated with other platforms and technologies. Note that an accurate estimate of non-recurring engineering costs associated with each approach is difficult to estimate without the specifics of each business situation, and is omitted in the scope of this discussion. Therefore one should be aware of the volume dependent sensitivities over which such fixed costs will be amortized for each case. Our analysis will focus on the recurring costs in each case, and the comparisons will in general be valid for high volume markets over which fixed costs are sufficiently amortized.

A. Economics

We begin by examining the basic bill of materials for the four different approaches. Table I shows the required substrate materials for each approach. Immediately clear is the fact that both flavors of silicon photonics (monolithic with external laser as well as heterogeneous) still require the use of III-V substrates in the end to integrate the light source. Cross referencing with the substrate costs listed in Table II, we can see that epitaxial growth on silicon is easily the most economical among all four cases in terms of substrate cost.

Other considerations for manufacturing cost comparisons should include processing, packaging, and testing costs in addition to raw materials cost. Although generating a full process based cost model for each approach is beyond the scope of this text, we can still use relative comparisons to infer the cost difference between the various approaches. Generalized

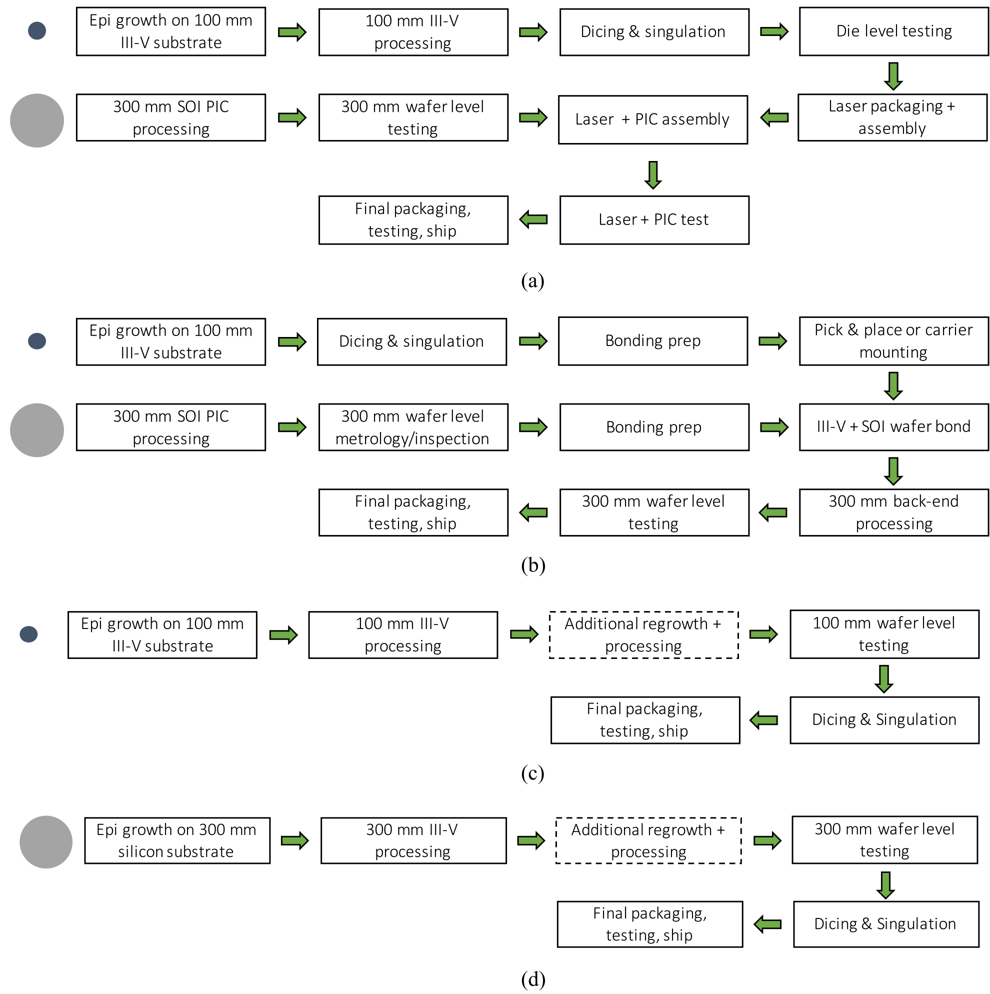


Fig. 7. Manufacturing flow diagrams for (a) Monolithic silicon photonics with an externally coupled lasers; (b) heterogeneously integrated silicon photonics; (c) InP PICs and (d) epitaxial III-V on silicon. The dark blue and grey circles indicate the relative wafer sizes of 100 InP and 300 mm SOI/silicon, respectively, and are meant to indicate the substrate size of the process.

manufacturing process flows for each of the four approaches are shown in Fig. 7(a)–(d) as a basis for comparison. A key distinction among each process is the relative wafer size - which are displayed next to each process as grey (300 mm SOI/silicon) or blue (100 mm III-V) circles with a 3:1 diameter ratio to serve as a guide for the eye.

Fig. 7(a) shows the manufacturing flow for a monolithic silicon photonics PIC with an externally coupled laser. A few key observations to note: utilizing an externally coupled laser for the monolithic silicon photonics process would necessarily absorb the entire cost of a separate III-V material growth and processing on the smaller and more expensive III-V substrate, dicing and singulation into individual devices/die, a testing/burn-in step for the lasers at the die level, and the extra packaging/assembly needed for hybrid integration with the SOI chip. In addition, it's likely that the laser will be sourced from an external vendor, which would introduce additional margin stacking costs on top of of the minimum cost of goods sold. For applications requiring multiple sources such as WDM, the cost and packaging for coupling multiple external lasers would become prohibitive.

Heterogeneous integration (Fig. 7(b)) eliminates some of the processing complexity and redundant testing by integrating the laser into the same wafer scale processing as the SOI, and obviating the need for die level testing and separate packaging of the stand-alone laser. However, it still requires the use of a III-V substrate for the original material growth, in addition to extra costs incurred for the bonding process (e.g., chiplet dicing, bonding, substrate liftoff/removal etc.). Heterogeneous integration also requires significant wastage of III-V materials as the diced pieces for bonding are often significantly larger than the required III-V device area due to limitations in minimize die size that is dependent on the substrate thickness and III-V boundary margin requirements for high-yield bonding.

As can be seen in Fig. 7(c), photonic integration on InP keeps the material growth and processing all in a single process on the same wafer, and employs wafer level testing. However, it is limited in process throughput by the relatively smaller substrate size. Photonic integration using epitaxially grown III-V on silicon leverages the best of both worlds by employing the streamlined process flow of an InP process, with the added benefit that it can leverage 300 mm tooling enabled by the larger

TABLE III
MANUFACTURING CONSIDERATIONS FOR PHOTONIC INTEGRATION

	Processing Throughput	Assembly Cost	Testing
InP	100 mm	N/A	Test laser + PIC at wafer level
Monolithic Silicon Photonics	100 mm III-V process, 300 mm SOI process	External laser packaging and coupling	Test laser at die level, test silicon PIC at wafer level, test laser + PIC at wafer level
Heterogeneous Integration	300 mm SOI process	N/A	Test laser + PIC at wafer level
Heteroepitaxial Integration	300 mm	N/A	Test laser + PIC at wafer level

TABLE IV
COMPARISON OF LIGHT SOURCE PERFORMANCE

	InP	Monolithic SiPh (External Laser)	Heterogeneous Integration	Epitaxial III-V on Si
RT stand-alone laser WPE (10-20 mW)	-	20-30%(estimated from [52])	-	38.4*% [24]
Active-passive coupling loss	0.1 dB (butt-joint regrowth) [6]	2-8 dB (off-chip to on-chip)	0.2-0.5 dB (taper losses) [53]	0.1-0.5 dB (assuming butt-joint regrowth)
On-chip WPE (10-20 mW)	∼15-20% (estimated from [52], [54])	3-17**	∼ 15%* [55]	∼34-37%**

*Double sided WPE from a FP laser; **Calculated using off-chip laser WPE and coupling loss.

and cheaper silicon substrate (Fig. 7(d)). These differences are summarized in Table III.

Therefore, we can conclude that the lowest cost approach to photonic integration is to combine III-V with silicon via epitaxial growth, eliminating the need for III-V substrates altogether and taking advantage of the processing, testing, and packaging equipment for 300 mm substrates. These sources for economic efficiency as compared to InP or monolithic + heterogeneous silicon photonics are summarized below:

- 300 mm (or larger) process
- simplified packaging (no external laser packaging: housing, isolator, lens, etc.)
- No III-V substrate required
- free up chip real estate dedicated to grating couplers or edge couplers for external laser coupling (e.g., fiber groove or spot size converter)
- eliminate margin stacking on all externally sourced components
- flip chip bonding and/or active alignment not required for light source integration (this includes process time for alignment itself as well as time for curing, setup/change-overs, tool maintenance, etc.)
- redundant testing of laser, separate silicon photonics chip, and the integrated package not required for light source integration.

B. *Performance*

Comparisons of device performance of between silicon photonics with InP can be found, for example in [11]. Here we will focus on the light source - the performance and method of integration of which is an important technological differentiator with important implications for system scaling. Coupling losses can significantly reduce the efficiency of the overall system and limit performance scaling - as they must be compensated by an increased power draw/consumption elsewhere in the system [52]. Table IV shows a comparison of light source schemes for the four different approaches described here. While using an externally coupled laser as is the case in monolithic silicon photonics allows one to choose the best performing laser, the much higher coupling losses (varying depending on coupling scheme such as edge vs. grating, and any excess loss due to mis-alignment or fabrication imperfection) compared to the other approaches are undesirable for efficient scaling of system performance.

Table IV also compares various reported room temperature wall plug efficiencies (WPE) for light sources of the various approaches. As WPE can vary depending on laser design as well as output power level, care was taken to make sure the numbers shown are all in the same range of output power levels between 10–20 mW. Also included are both stand-alone laser efficiencies as well as the effective on-chip WPE which takes into account coupling losses from the laser to a waveguide: using either reported values or calculated based on known stand-alone laser efficiency and the estimated coupling loss. As can be seen, reported WPEs of quantum dot lasers epitaxially grown on silicon are already rivaling performance of lasers on native substrates, and stand to be very competitive as an on-chip light source once low-loss active-passive coupling schemes are developed.

Another important consideration for the light source is the natural heat-sinking of its substrate. Table V shows a comparison of the thermal conductivity of the light source for the four approaches considered here (monolithic silicon photonics is assumed to have the same substrate as InP and are both grouped under the “native substrate” column). Bulk silicon substrates have almost twice the thermal conductivity as InP, implying improved natural heat sinking for lasers grown on silicon. Thermal simulations of laser structures on the three different substrates (InP, SOI, and silicon) were performed for varying mesa widths (26, 10, and 3 μm wide) and a 500 μm long cavity. In each case, the laser material stack and injected power level was the same (1 Watt), except in the case of epitaxial growth on silicon where

TABLE V
THERMAL CONSIDERATIONS FOR THE LIGHT SOURCE

	Heterogeneous Integration	Native (InP) substrate	Heteroepitaxial Integration
Substrate thermal conductivity ($\mathbf{Wm^{-1}K^{-1}}$)	- (SOI)	68 (InP)	131 (Si)
$\mathbf{Z_T}$ for 26 μm mesa (°K/W)	55	36	29
$\mathbf{Z_T}$ for 10 μm mesa (°K/W)	84	50	41
$\mathbf{Z_T}$ for 3 μm mesa (°K/W)	134	83	73

Substrate thermal conductivity as well as simulated thermal impedances (Z_T) of the same InP based separate confinement heterostructure laser material stack on the three different substrates here. In each case the laser cavity was 500 μm long, and 1 Watt of injected power in the laser active region was used. For epitaxial III-V on silicon, an additional 2 μm buffer was added between the laser stack and the substrate to reflect the need for dislocation buffers.

an additional 2 μm InP buffer was added to reflect the need for sufficient buffer thickness to achieve defect reduction, as well as to prevent mode leakage to the silicon substrate. In each case growth on silicon yields the lowest thermal impedance for the laser, as expected. Fig. 8(a)–(c) shows the cross-sectional temperature profile of the 26 μm case: showing an active region temperature difference of nearly 30 degrees compared to heterogeneous integration. The improved heatsinking is beneficial for both device efficiency as well as long-term reliability. Dislocations at the III-V/silicon interface generated due to the lattice mismatch may be expected to contribute to phonon scattering and reduce the local thermal conductivity. However, experimental measurements of the thermal conductivity of InP grown on silicon show that the thermal conductivity is unchanged from the bulk value for films with low defect density and/or sufficient thickness [56], which is corroborated by other theoretical studies [57], [58].

V. FORCES DRIVING ADOPTION

Following the techno-economic comparison in the previous section, we now examine both performance and economic trends for the evolution of photonic integrated circuits, which would drive the adoption of epitaxial III-V on silicon as an integration platform. The prevailing trend that drives the evolution of PICs is higher integration density, higher power efficiency, and smaller form factors. New markets with higher volumes are likely to emerge at the leading edge of the cSWaP curve where epitaxial III-V integration on silicon holds a significant advantage. In datacom and computercom, this is taking shape in the form of leveraging photonics for post-Moore performance scaling of electronic systems: driving photonics into the package in the near term, and generally more intimate integration (e.g., 3D stacking) with electronics to enable new high performance system architectures and functionalities in the long term. While datacenters and high-performance computing (HPC) are the primary application pull for this so far, lower cSWaP enabling higher integration densities without increases in the power

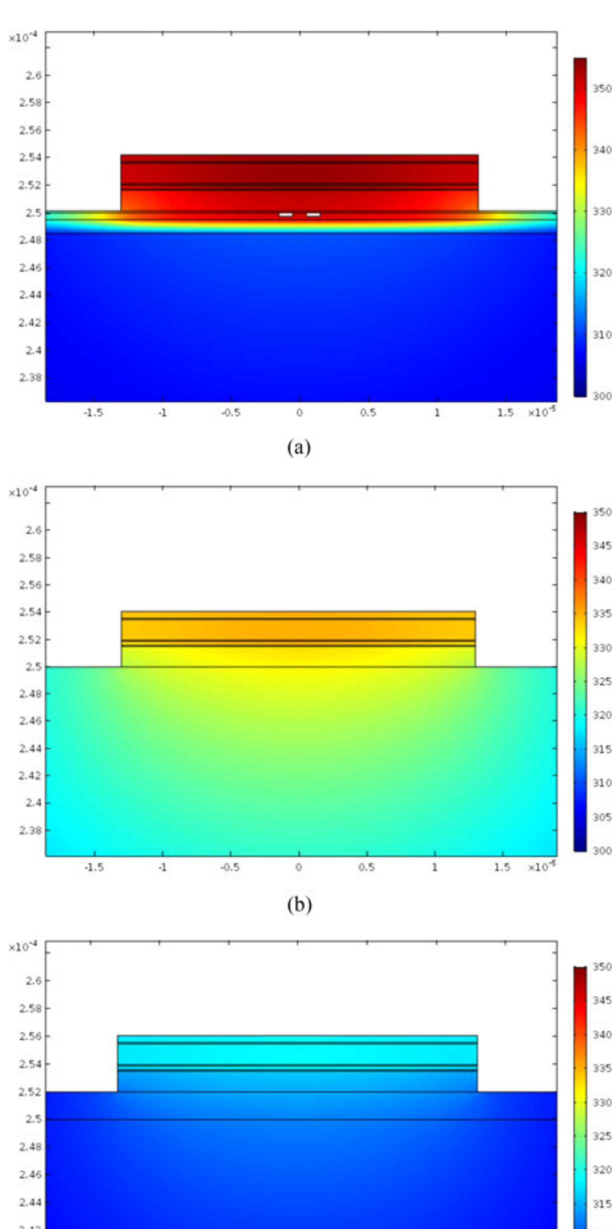


Fig. 8. 2D thermal profile simulations of lasers on (a) heterogeneously integrated on SOI; (b) grown on native InP substrate; (c) epitaxially grown on silicon (2 μm dislocation buffer added between substrate and laser to reflect reported laser structures). (All mesa widths here are 26 μm wide, 1 watt of injected power assumed, X and Y axis labeling in meters.) Lasers directly grown on silicon substrates with its superior thermal conductivity shows a clear advantage in natural heat-sinking.

envelope are a boon for any PIC application. In IoT and consumer sensors for example, enabling drastic form factor reductions to enable ubiquitous deployment while operating with a very small power draw from a fixed/limited DC power supply - all at low cost - is another trend driving the evolution of PICs. From a performance point of view, cSWaP scaling points to on-chip integrated lasers versus hybrid integration with an

external laser [52], as the coupling losses, extra footprint, and costs involved forms a self-imposed limit to its scaling potential. Among the platforms with on-chip laser capabilities, epitaxial growth on silicon offers the lowest cost.

The anticipated introduction of III-V materials into CMOS fabs is another factor that could expedite the adoption of this platform. There has been renewed interest by industry in using high mobility III-V compound semiconductors for post-Moore CMOS [59]. A number of foundries have already expressed anticipation for integrating III-V materials into their fabs for CMOS scaling, including AIM Photonics, STMicroelectronics, and IMEC. There is synergy to be leveraged for using the same tools and processes to create III-V photonic devices (epitaxially grown) on silicon. For example, IMEC recently demonstrated the world's first III-V FinFET on a 300 mm silicon substrate using selective area growth on pre-patterened (001) silicon [60]. As mentioned earlier, they were also able to leverage the same process to fabricate wafer scale integrated DFB lasers directly grown on (001) silicon [39]–[41], an important proof of concept. We further note that Intel's heterogeneous silicon photonic transceiver line is manufactured in a dedicated CMOS fab. Several other challenges remain to develop a wafer level process flow involving heteroepitaxial III-V integration in such fabs, however the aforementioned activities are a sign that industry is actively investigating in this area.

VI. Summary and Outlook

A number of breakthroughs have now made epitaxial growth of III-Vs on silicon an appealing platform for photonic integration from both a cost and performance standpoint. The same forces that drove the evolution of discrete optical modules to photonic integration on a single chip will continue to shape the evolution of photonic integrated circuits to meet the ever increasing demands on lower cost, size, weight, and power (cSWaP) while delivering equal or better performance than their predecessors. Photonic integration with epitaxial growth on silicon is now emerging as a strong candidate to meet those requirements.

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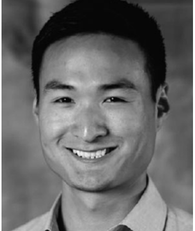

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