# Photonic Integrated Circuits Using Heterogeneous Integration on Silicon

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**ABSTRACT** | Heterogeneous silicon photonics using wafer bonding is reaching maturity with commercial products for the data center market being shipped in volume. Here we give an overview of recent research in the area showing record device performance by using the best of both worlds: III–V for light generation and Si for guiding the light. Utilizing the flexibility of the heterogeneous silicon platform, narrow-linewidth widely tunable lasers as well as fully integrated mode locked lasers with record pulse powers and pulse duration were demonstrated. The ability to perform multiple die bonding with optimized epitaxially grown layer stacks was used to realize high-performance photonic integrated circuits both for communications and sensing. In addition to III–V materials, nonreciprocal materials such as, for example, Ce:YIG can be bonded, providing additional functionality such as on-chip isolators and reconfigurable on-chip circulators. On-chip isolation will become necessary with the increase in complexity of photonic integrated chips as photonic components such as lasers are sensitive to feedback effects.

**KEYWORDS** | Heterogeneous silicon platform; integrated optoelectronics; optoelectronic devices; semiconductor lasers; silicon photonics

## I. INTRODUCTION

Photonics integrated circuits (PICs) can be realized in a number of platforms, but for efficient on-chip light generation a direct bandgap semiconductor is needed. Historically, the first PICs with lasers were realized on GaAs or InP substrates [1]. The performance of lasers on native III–V substrate is considered state of the art, but their high cost due to smaller wafer size and expensive substrates still presents a barrier to some markets.

More recently, optical components have been integrated on silicon (Si) substrates. In the past 15 years, a whole range of photonic components have been demonstrated, mostly using the silicon-on-insulator (SOI) platform. The SOI platform is especially suited for standard communication bands at 1.31 and 1.55 $\mu$m, as both silicon and its oxide $SiO_2$ are transparent and form high-index contrast, high-confinement waveguides ideally suited for highly integrated PICs. However, electrically pumped efficient sources on silicon remain a challenge due to the indirect bandgap of silicon. There have been some demonstrations with strained Ge, but the performance is very far from practical products and the standards set by III–V on Si [2]. Many current Si photonic PICs use hybrid approaches in which the Si PIC is coupled to III–V PIC which provides the optical gain for lasers [3]. Such an approach requires precise alignment and arguably has scaling limitations.

An alternative approach, most commonly called heterogeneous integration, bonds pieces of III–V material onto a patterned Si wafer and then processes them together using standard lithography tools. First demonstrated by the University of California at Santa Barbara (UCSB) in 2006 [4], such an approach is currently widely used by academia (e.g., UCSB [5], [6], Ghent University [7], [8]), research organizations (e.g., III–V lab [9]), and industry (e.g., Intel [10], Juniper Networks (former Aurrion) [11], HP Enterprise [12]) with first commercial products for data center market being shipped in volume [10]. The advantage of this approach is that the alignment tolerances are significantly reduced as devices are defined lithographically after bonding of unpatterned III–V dies. This process allows for efficient volume scaling. Furthermore, the use of complementary metal–oxide–semiconductor (CMOS)

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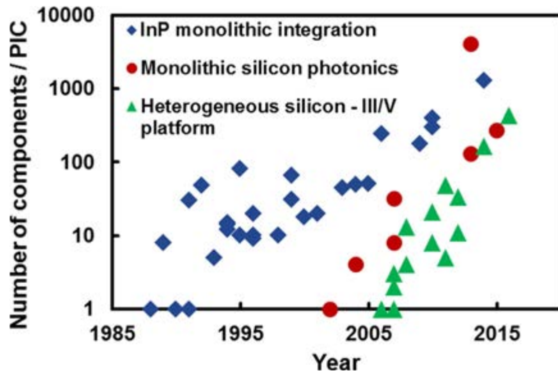


**Fig. 1.** *Evolution of photonic integration in terms of the number of devices in a single PIC. Silicon photonic integration (red circle) represents the "passive" integration without an on-chip laser solution; InP integration (blue squares) and heterogeneous silicon integration (green triangle) are solutions with on-chip lasers.*

processing infrastructure, perfected throughout the years and billions of dollars invested by semiconductor industry, allows for superior silicon waveguide quality with smaller feature sizes, smoother surfaces, and superior yield. This will become increasingly important as the complexity of PICs increases, as shown in Fig. 1.

The paper is organized as follows. In Section II, we introduce the heterogeneous silicon platform, and provide brief literature overview and examples of individual devices such as widely tunable lasers, mode-locked lasers, modulators, amplifiers, and photodetectors. The ability to bond multiple, smaller pieces of III–V allows for added flexibility by combining multiple optimized epitaxial layer stacks to realize complex systems on chip. We describe the capabilities of this approach in Section III, and provide examples such as microwave generators, interferometric gyroscope front-ends, beam scanners, and a network-on-chip with 2.56-Tb/s capacity. Bonding can be extended to other materials, which can be used to provide additional functionality such as isolators (Ce:YIG) and second harmonic generation ($LiNbO_3$). In Section IV, we report on on-chip isolators and circulators, both of which are reconfigurable. Finally, we summarize and give future outlook in Section V.

## II. HETEROGENEOUS SILICON PHOTONIC DEVICES

Heterogeneous silicon photonics[1] works to provide the best of both worlds: high-performance devices from optimized III–V materials and superior passive and waveguide technology of the SOI platform. Physically, the large mismatch in lattice constant and thermal expansion coefficient between the Si and III–V make monolithic integration very challenging, although a lot of progress has been reported as shown in [13]. Bonding removes, or at least relaxes, the lattice mismatch limitations to a very large degree although the thermal expansion coefficient mismatch still has to be taken care of. For this reason, the temperature during bonding and subsequent processing steps is typically limited to <300 °C. There are two main bonding approaches that have developed: covalent molecular direct bonding and adhesive bonding using polymers [14]. The former is pursued by UCSB, Intel, Juniper, HPE, and III–V labs among others, while the latter is pursued by Ghent University among others.

In a typical heterogeneous silicon process, waveguides and other devices are first defined in a SOI wafer using standard CMOS-compatible processes. Next, pieces of III–V material are bonded and processed as shown in Fig. 2. As the pieces are typically larger than a single device, the alignment tolerances are significantly relaxed. For high volume production, it is possible to simultaneously bond across a full Si wafer with the help of a carrier wafer for the III–V pieces. The processing then continues using alignment marks defined on the SOI wafer, and benefits from immersion DUV lithography commonly used in CMOS.

The SOI wafers are typically optimized for heterogeneous platform, and commonly have thicker Si device layer (400–500 nm) compared to the more commonly used 220-nm-thick silicon photonics platform. The reason is to facilitate more efficient coupling between active and passive regions [8]. Another change in heterogeneous silicon photonics is the reduction in buried oxide (BOX) thickness from the commonly used 2 to 1 $\mu$m, which improves thermal performance if laser is not flip-chip bonded. We have demonstrated up to 105 °C lasing, and

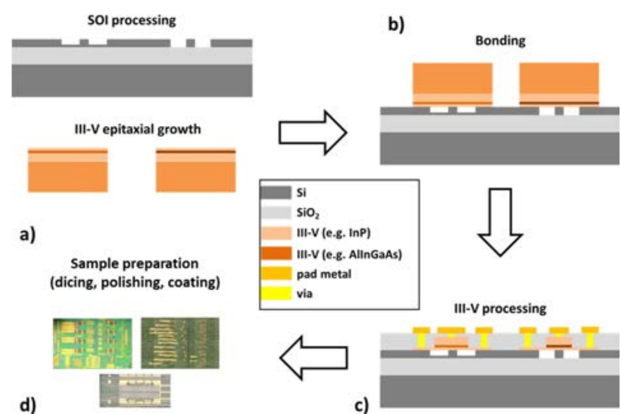


**Fig. 2.** *Simplified illustration of basic steps in a heterogeneous silicon photonics fabrication process. A typical full run has 15–20 lithography steps.*

[1]When the heterogeneous approach was first demonstrated, the nomenclature "hybrid III–V silicon evanescent laser" was used and often shortened to "hybrid silicon laser." In subsequent years, "heterogeneous" is more commonly used to describe this wafer scale approach to integration, and "hybrid" is more commonly used for bonding or soldering individual dies onto a common substrate.

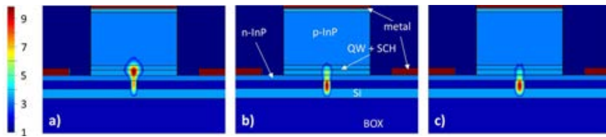


**Fig. 3.** *The fundamental TE mode in exemplary heterogeneous region as width of underlying shallow etched Si waveguide is changed. Corresponding Si waveguide widths are as follows: (a) 0.6 μm; (b) 0.8 μm; and (c) 1 μm. The color bar on the left corresponds to the index of refraction.*

commercial companies have shown up to 150 °C lasing, which shows that higher thermal impedance of BOX layer is not the limiting factor in potential laser integration with electronics.

A common question relates to the yield of heterogeneous devices. Generally, yield in both silicon and III–V processing is improved by the use of advanced lithography and processing tools. Wafer bonding yield is critically limited by vertically protruding defects on the III–V chip (which can be avoided with prior inspection), and by particulate contamination on both parts (Si and III–V), both of which can be further improved by transferring the process to more advanced growth reactors and cleanrooms. The silicon wafer is virtually free of surface defects.

For the covalent molecular direct bonding, a plasma activator is used to activate both the Si and InP wafer surfaces prior to bonding. The pieces are then placed in contact, which forms a spontaneous bond between the surfaces. This bond is strengthened by placing the wafer in a graphite clamp and annealing (typically at 300 °C for 1 h). Trapped water vapor at the bonded interface can form voids during the bonding anneal, so the surface of the silicon is commonly patterned with an outgassing structure [14].

The optical mode in the heterogeneous region extends in both the Si and III–V region, and the confinement can be controlled with the width of Si waveguide, i.e., lithography, which is a powerful tool to engineer the modal profile as shown in Fig. 3. The transition between heterogeneous region and passive Si waveguides is essential for high-performing devices: it should have low loss, low unintentional reflection, low transmission into higher order waveguide transverse modes (if supported), and high optical bandwidth (for certain class of devices). Design methodology and experimental characterization of a number of taper structures is presented in [15]–[18]. The transition may be accomplished in a number of ways, including a lateral directional coupler, vertical directional coupler, a grating-assisted codirectional coupler, or an adiabatic coupler. In our devices, we typically implement adiabatic tapers (shown in Fig. 4) as they do not have intrinsic parasitic reflections and can be designed to have extremely large wavelength bandwidth [16].

In the last ten years, many high-performing components realized in the heterogeneous silicon platform have been demonstrated, some of which outperform their native III–V counterparts. In the remainder of Section II, we present a brief overview of devices developed for standard telecommunication bands of 1.31 and 1.55μm. The heterogeneous platform has been extended, in recent years, beyond near-infrared telecommunication wavelengths to the mid-infrared (MIR) (2–20 μm) regime using a number of waveguide platforms (Si, $SiO_2$, SiN, Ge, etc.) and laser technologies such as InP Type-I and Type-II diodes; GaSb Type-I diodes and intreband cascade laser (ICL) structures; and InP, GaAs, and InAs quantum cascade laser (QCL) structures. These wavelengths hold potential for an extensive range of sensing applications. The topic lies outside the scope of this paper, but a good overview is presented in [19]. The heterogeneous approach can also be extended toward other waveguide systems, such as integration of active material on SiN waveguides that are transparent down to 0.4 μm as demonstrated in [20]. It should be pointed out that due to the sheer number of publications in the area, the overview is to be illustrative and not exhaustive.

## A. Single-Frequency Lasers

Since the first demonstration in 2008 [21], heterogeneous silicon single-frequency distributed feedback (DFB) lasers have been continuously improved [22]–[24] and now offer sub-10-mA thresholds, 5+ mW of output power, high temperature lasing up to 100 °C and high side-mode suppression ratio (SMSR) >55 dB. As the platform allows for the control of confinement in the quantum wells (QWs) and provides a low-loss waveguides, it opens up a new possibility in improving the coherence by providing a mechanism to separate the photon resonator (in Si) and highly absorbing active medium [25]. Initial demonstrations of heterogeneous DFB lasers with cavity quality factors in $10^6$ range showed Lorentzian linewidths as low as 18 kHz significantly outperforming native III–V DFB lasers. With further optimization, sub-kilohertz instantaneous linewidths were demonstrated [26]. Use of state-of-the-art DUV lithography also allows for direct definition of

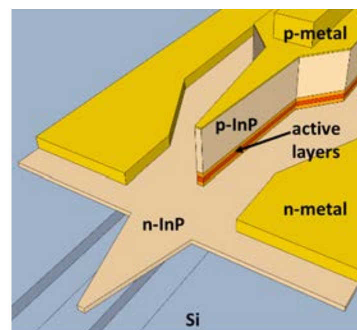


**Fig. 4.** *A 3-D mockup of the transition between heterogeneous and passive Si regions with dual layer tapers.*

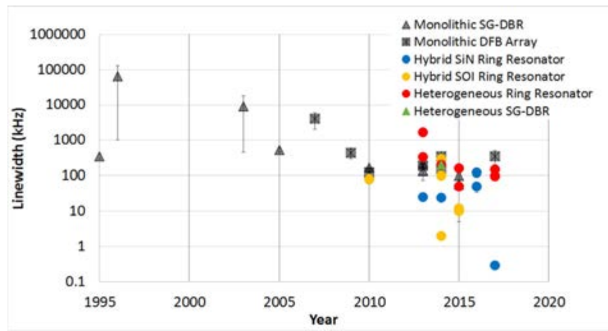


**Fig. 5.** *Linewidth of widely tunable integrated lasers versus time. We make a distinction between III–V-based monolithic lasers, hybrid lasers where individual III–V dies are bonded or soldered to a common substrate, and heterogeneous integrated lasers where larger pieces of the III–V gain material are bonded to silicon. (Sampled grating distributed bragg reflector (SG–DBR), distributed feedback (DFB), silicon-nitride (SiN), silicon-on-insulator (SOI).*

the grating, allowing such lasers to be mass produced on a 300+ mm wafer scale.

## B. Widely Tunable Lasers

Chip-scale widely tunable lasers are important for both communication and sensing applications, and they have a number of advantages such as size, weight, and cost compared to mechanically tuned counterparts. Furthermore, they allow for integration in more complex integrated photonic chips to realize added functionality. Wide tunability in chip-scale semiconductor lasers is commonly achieved by utilizing the Vernier effect. The effect has been utilized both with sampled Bragg grating (SG–DBR) reflectors and ring resonators, but the use of ring resonators tends to be more common in heterogeneous silicon devices [27]. Ring resonators, provided that the utilized waveguide platform offers sufficiently low propagation losses, have an advantage as the effective cavity length at ring resonance is significantly enhanced, directly reducing linewidth [28], [29].

Heterogeneously integrated tunable lasers have been demonstrated at both telecommunication bands (1.31 and 1.55 $\mu$m) with wide-tuning range (54 nm), high SMSR (>45 nm), up to 18 mW of on-chip power and integrated linewidths down to 50 kHz [9], [18], [30]–[34]. Linewidth is again superior compared to native III–V devices, as shown in Fig. 5 [27].

## C. Mode-Locked Lasers

The mode-locked lasers are a special class of lasers that produce a time series of short optical pulses at radio frequencies. Integrated mode-locked laser diodes, similarly to on-chip widely tunable lasers, have an advantage in their small size and capability for electrical pumping compared to bulk crystal and fiber lasers. Utilizing advantages of semiconductor manufacturing technology allows for mass production, and results with lower cost and potential for integration into larger integrated circuits, such as photonically enhanced analog-to-digital converters (ADCs).

There have been a number of demonstrations of heterogeneously integrated mode-locked lasers with improving performance [35]–[37]. Recently, 900-fs pulses were demonstrated, which is the shortest for a mode-locked laser on a silicon substrate with 98 mW of peak power [17]. The passively-mode-locked RF linewidth was 1.1 kHz, lowest ever demonstrated at 20 GHz. Two other sub-picosecond fully integrated mode-locked lasers [38], [39], both realized in the monolithic InP platform, utilized racetrack-style lasers which typically have poor output power due to the inability to control the lasing direction. The output power was not reported in either publication.

## D. Semiconductor Optical Amplifiers

As the complexity of PICs increases (see Fig. 1), the semiconductor optical amplifier (SOA) has become a critical component for many kinds of PICs to increase the output power and maintain signal levels as the signal propagates throughout a large number of optical components.

Since the first SOA on Si demonstration in 2007 providing 13 dB of on-chip gain and 11 dBm of output saturation power [40], the performance of heterogeneous SOAs was again continuously increased with subsequent demonstrations [16], [41]–[43]. Devices with up to 28 dB of on-chip gain [43] and output saturation powers of 16.8 dBm were recently demonstrated [16]. As the heterogeneous platform allows for continuous change of the confinement in the active region by changing the width of underlying Si waveguide (Fig. 3), it is possible to design a SOA with both high gain and the high output power.

## E. Modulators

Silicon photonics inherently provides many phase tuning mechanisms. The most common method of achieving phase and amplitude modulation in silicon devices is to exploit the plasma dispersion effect, in which the concentration of free charges in silicon changes the real and imaginary parts of the refractive index. This can be accomplished by using p-n and p-i-n junctions, or metal–oxide–semiconductor (MOS) junctions [44], [45]. Another method is thermal tuning, which is reasonably efficient due to large thermo–optic coefficient of silicon, but is too slow for data transfer applications and has generally large static power consumption. All these methods primarily change the phase, so a Mach–Zehnder interferometer or resonator structure (e.g., ring resonator) is employed to convert the phase modulation to amplitude modulation. With the introduction of germanium (Ge), small, efficient electroabsorption modulators utilizing the Franz–Keldysh effect are possible with low leakage currents (47 nA @ -2 V) and bandwidths exceeding 50 GHz [46], but in this demonstration, the operating wavelength was limited to 1610 nm

or longer due to the increase in insertion loss at shorter wavelengths. Optimization of the operating wavelength is possible by using SiGe, which shows 4.8-dB insertion loss at 1540 nm and up to 38-GHz bandwidth [47], but with larger leakage current in the microampere range.

The heterogeneous silicon platform allows for the use of III–V-material-based modulators. The use of III–V materials brings a number of advantages, such as large electron-induced refractive-index change, high electron mobility, and low carrier-plasma absorption, all of which are beneficial for overcoming the tradeoffs commonly encountered with modulators [48]. Furthermore, the state-of-the-art in QW design in III–V is currently superior to Ge/SiGe [49], [50] allowing for the utilization of quantum-confined Stark effect (QCSE) at arbitrary telecommunication wavelengths with devices fully integrated with standard SOI platforms. Bandwidths in excess of 67 GHz, and data transmissions at 56 Gb/s were demonstrated [51]–[53]. The QCSE is overall likely the strongest modulation mechanism [54]–[56], but very efficient modulators were also demonstrated in bulk III–V materials, especially if the SiSCAP type of structure is used. Performance of III–V/Si modulators surpassed the performance of Si MOS optical modulators in terms of phase modulation efficiency by a factor of 5 ($V_{\pi}\cdot\text{L} = 0.047$ V·cm), while at the same time providing lower insertion loss [48], [57].

### F. Photodetectors

Silicon, being transparent at standard communication wavelengths of 1.31 and 1.55 $\mu$m, cannot be used for detection at the same wavelengths. Detection, in silicon photonics, is commonly realized with the use of Ge. Ge-based waveguide detectors offer high bandwidths (45 or 67 GHz), good responsivities (0.8 or 0.74 A/W), and low dark currents in the nanoampere range [58], [59]. A problem is that the responsivities decrease as the wavelength of operation is increased beyond 1550 nm, leading to a direct tradeoff if Ge-based electroabsorption modulators are used as they tend to work better with lower insertion loss at longer wavelengths.

In the heterogeneous platform, detectors can be based on III–V material, often InGaAs that typically absorbs up to 1.7 $\mu$m with no drop in responsivity. The added flexibility of tailoring the Si waveguide width and the III–V mesa width allows for flattening the absorption profile and suppressing the localized saturation leading to record radio-frequency (RF) output power of 12 dBm at 40 GHz, which is the highest reported output power of high-speed waveguide photodiodes for any waveguide photodiode technology, including native InP and Ge/Si [60]. Performance has been further optimized leading to high bandwidths (65 GHz) and record high RF output powers at 70 GHz of –2 dBm with very low dark currents of 1 nA [61]. Bandwidths exceeding 67 GHz (limited by measurement equipment) have also been demonstrated with a high responsivity of 0.7 A/W [62].

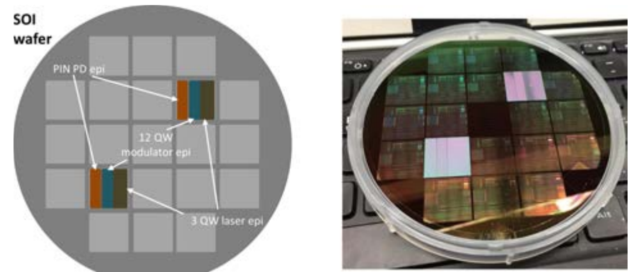


**Fig. 6.** *(Left) A schematic of a 4-in SOI wafer with multiple III–V epitaxial layers bonded on a single die. (Right) Photograph of a 4-in SOI wafer processed and bonded with III–V in the University of California Santa Barbara cleanroom.*

## III. SYSTEMS ON CHIP

A complex PIC might require a number of different, high-performing components. The underlying Si waveguides can provide routing, multiplexing/demultiplexing, filtering, splitting, and combining. With some extra processing (implants and Ge), silicon photonics can also provide modulation and detection, albeit with some limitations, as pointed out in the previous section. The ability to bond different epitaxially grown III–V thin films on a single die allows for optimization of individual device performance. A complex PIC device might make use of optimized laser gain material, bandgap shifted modulator material as well as optimized photodetector material, all on the same SOI die as shown in Fig. 6. The corresponding monolithic III–V PIC would require multiple regrowth steps. With proper design of the III–V layer stacks, simultaneous processing of all the different III–V layers after bonding is possible, reducing the number of processing steps, directly reducing cost and improving yield. The process also allows for fabrication of 1.31- and 1.55-$\mu$m devices on same wafer as demonstrated in [11].

This multiple-die bonding technology allows for state-of-the-art PICs for communications, signal generation, and sensing. We briefly describe a few key PIC demonstrations in the remainder of this section. Furthermore, the scalability of CMOS processing and high volume production can bring the cost down, allowing PICs to enter markets where pure III–V devices cannot compete due to price barriers.

### A. Microwave Generator

The broadband nature and low-loss capability of photonics has led to an ever-increasing interest in its use for the generation, processing, control, and distribution of microwave and millimeter-wave (mm-wave) signals for applications such as broadband wireless access networks, sensor networks, radar, satellite communitarians, instrumentation, and warfare systems [63]. One way to generate a microwave or mm-wave signal in the optical domain is based on optical heterodyning, in which two optical waves of different wavelengths are beat together on a

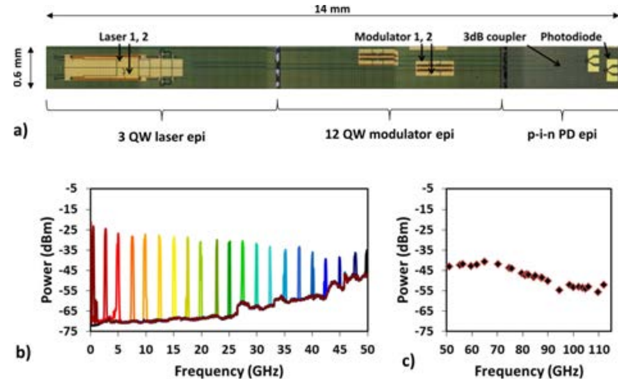


**Fig. 7.** *(a) Optical microscope image of the fully integrated photonic microwave generator chip and measured microwave signals (b) from 1 to 50 GHz on an ESA, and (c) from 50 to 112 GHz on an E-band power meter.*

photodetector. A chip-scale device providing that functionality has many advantages, most importantly size, weight, and cost. A fully integrated photonic microwave generator realized in the heterogeneous silicon platform combined waveguide photodiodes with a 3-dB bandwidth of 65 GHz and 0.4-A/W responsivity with lasers that tune over 42 nm and have 150-kHz linewidth. The microwave signal generated from beating two lasers together ranges from 1 to 112 GHz. The inclusion of modulators allows for direct signal generation at the microwave frequency, or for generation of sidebands for, e.g., measurement applications [64]. The total size of the chip was 14 mm $\times$ 0.6 mm as shown in Fig. 7, but the length could significantly be reduced with different routing, down to $\sim$3.5 mm. The laser would occupy $\sim$2.5 mm of length, modulators $\sim$0.7 mm of length, and photodetectors with pads $\sim$0.3 mm of length. The width of the chip would remain the same at 0.6 mm. This would bring down the total area to $\sim$2.1 mm$^2$ allowing for fabrication of more than 25 000 devices from a single 300-mm wafer.

## B. Interferometric Optical Gyroscope Driver

Interferometric fiber optic gyroscopes (IFOGs) were originally proposed in late 1960s and have been developed for decades. Today, IFOG is a mature technology which delivers high sensitivity, high stability, and reliability. A modern IFOG comprises five main components: a passive sensing fiber coil, a $LiNbO_3$ chip with modulators and beam combiners, a laser, photodetectors, and readout electronics [65]. Most of the modern IFOGs still use discrete optical components that are pigtailed and connected with the fiber coil to form a Sagnac reciprocal interferometer. Use of bulk components results in larger size and high cost, especially if multiple rotation axes or redundancy is implemented. Integration could reduce cost, weight, and size, and make the gyroscope more robust to vibrations and shock, opening new application opportunities.

Such a device was recently demonstrated in the heterogeneous silicon platform [66]. This was a first chip-scale fully integrated optical driver (IOD) that can interrogate a sensing coil and realize an IFOG. The chip comprises a light source (Fabry–Perot laser with broad optical spectrum which is beneficial for gyroscope operation), three photodiodes (7-GHz bandwidth, 0.7-A/W responsivity, 4-nA dark current), two phase modulators ($V_\pi$ = 4.2 V), and two broadband 3-dB splitters (>70-nm bandwidth) within an area of 4.5 mm$^2$, as shown in Fig. 8. A similar structure can be used in magnetometers and current sensors using special sensing waveguides or fibers [67], [68]. The size could also be further reduced with different routing, resulting in a large reduction in size, weight, and power consumption, compared to current bulk variants.

## C. Two-Dimensional Beam Scanner

Free-space beamsteering is important for light detection and ranging (LIDAR), free-space communications, and has potential applications for holographic displays and biomedical imaging. LIDAR employs a moving laser beam to sample the environment for optical "echoes" and rapidly collect high-resolution 3-D images. In recent years, the research has intensified as a need for cost-efficient, lightweight LIDARs may be necessary for autonomous driving.

Photonic integration allows for integration of a phased array beamsteering system on a chip [69], with much higher stability and performance and lower cost than has been previously possible. The heterogeneous silicon PIC consists of 164 optical components including lasers, amplifiers, photodiodes, phase tuners, grating couplers, splitters, and a photonic crystal lens in 69 mm$^2$, as shown

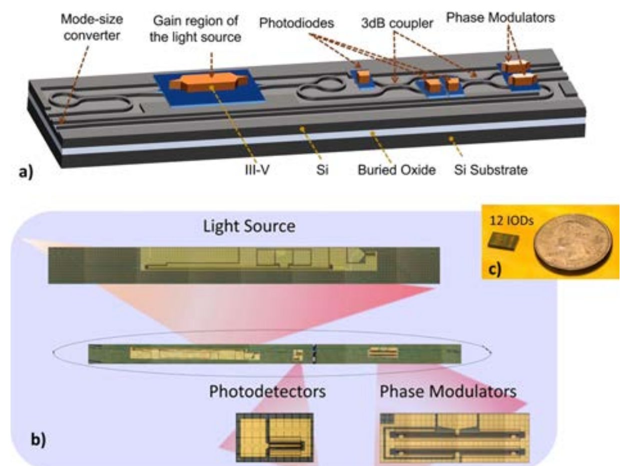


**Fig. 8.** *(a) Three-dimensional schematic of the integrated optical driver (IOD) for fiber optic gyroscopes. (b) Photo of a fabricated IOD chip with closeups of its components. (c) A set of 12 IOD devices next to a U.S. quarter coin for size comparison.*

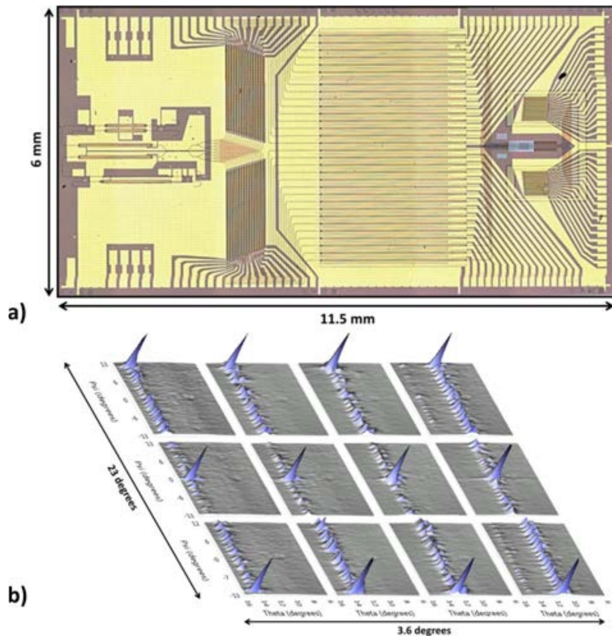


**Fig. 9.** *(a) Confocal microscope picture of the fully integrated beamsteering PIC. The chip size is 11.5 mm × 6 mm. (b) Two-dimensional beamsteering plots spanning 23° in $\psi$ and 3.6° in $\theta$ planes.*

in Fig. 9. All the active components (lasers, amplifiers, photodiodes, and phase shifters) are realized in heterogeneous silicon photonics. The beam scanner allows for steering over 23° × 3.6° with beam widths of 1° × 0.6° giving a total of 138 resolvable spots in the far field with 5.5-dB background suppression. As this is currently very active area of research, many improvements in performance are expected in near future.

### D. Network-on-Chip

As chip interconnects bit rates have increased, the power consumed by equalization and clock recovery and retiming has increased, and copper interconnects have become a bottleneck [70].

The limit to the total number of bits per second of information that can flow in a simple digital electrical interconnection is set only by the ratio of the length of the interconnection to the total cross-sectional dimension of the interconnect wiring—the "aspect ratio" of the interconnection. This limit is largely independent of the details of the design of the electrical lines, and because it is scale invariant, it cannot be changed by either growing or shrinking the system. Performance can be improved by using repeaters, advanced coding, and multilevel modulations, but these techniques also have limitations, one of which is the energy efficiency. Furthermore, the energy for communicating in electrical wires is essentially bounded by the energy required to charge up the appropriate line capacitance to the driving signal voltage [54].

The preferred solution to this problem is an optical interconnect, since it avoids the resistive loss. A processor using on-chip photonic devices to directly communicate with other chips using light was recently demonstrated [71], but in this demonstration the laser was external. An on-chip light source could provide overall system efficiency improvement as coupling losses are reduced and lasers can be switched off when the processor load is low [72].

An optical network-on-chip (NoC) that connects eight nodes, realized in the heterogeneous silicon platform, has been demonstrated [73] and is shown in Fig. 10. The NoC has eight nodes, each node having eight DWDM channels capable of ON–OFF keying (OOK) data transmission of up to 40 Gb/s, bringing the total on-chip capacity to 2.56 Tb/s. The chip comprises more than 400 functional components including lasers, modulators, amplifiers, detectors, switches, and arrayed-waveguide gratings in an area of 176 $mm^2$ and uses three different III–V layer stacks. A three-QW AlGaInAs stack with photoluminescence (PL) peak at 1545 nm provides gain for lasing (DFB lasers with 7.5-mA threshold current), amplification, and is used for monitor photodetectors on-chip. A 12-QW AlGaInAs stack with PL peak at 1485 nm is used for electroabsorption modulators. The bandgap offset is optimized for low insertion loss and high modulation efficiency with low drive voltage (6 dB extinction @ 1 $V_{pp}$ drive voltage). Finally, a p-i-n InGaAs detector is used for high-speed detectors providing >20-GHz bandwidth and low dark current (10 nA).

Due to probing limitations (device was not packaged), only individual channels were tested at a given time and the impact of channel crosstalk when all nodes are simultaneously communicating remains an open question. If crosstalk turns out to be an issue, it can be addressed by optimization of passive components and introduction of nonreciprocal materials as described in the following section.

Such a NoC is suitable for high speed, chip level optical interconnections and is the most complex heterogeneously integrated PIC to date in terms of component count.

## IV. HETEROGENEOUS INTEGRATION OF NONRECIPROCAL MATERIALS

Heterogeneous integration on silicon can accommodate not only III–V materials that provide gain, detection, and modulation, but can also include other materials bringing additional functionalities to the platform, such as nonreciprocity. Optical nonreciprocity is a phenomenon where light behaves differently depending on its propagation direction due to the asymmetric scattering matrix of the medium [74]. Many techniques for achieving optical nonreciprocity have been proposed using spatial–temporal modulation of the refractive index [75]–[77], or exploiting optical nonlinearities such as stimulated Brillouin

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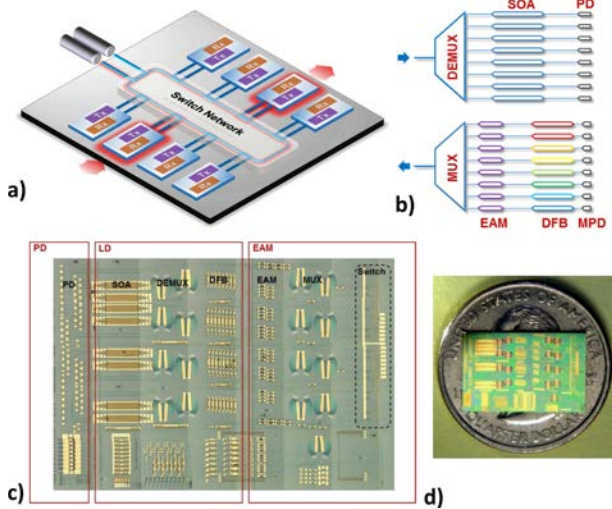


**Fig. 10.** *(a) Schematic of the optical NoC comprising eight nodes connected via ring bus architecture having one port for off-chip communication. (b) Each node comprises 8-channel WDM transceiver architecture. (c) Microscope image of the photonic transceiver circuit. The dimensions are 16 mm × 11 mm. Red rectangles mark the areas where different III–V layer stacks are bonded. (d) Size comparison between optical NoC and a U.S. quarter. (PD: high-speed photodiode; LD: laser diode; EAM: electroabsorption modulator; MPD: monitor photodiode; MUX/DEMUX: multiplexer/demultiplexer.)*

scattering [78], [79] and Kerr-like effects [80], among others. The latter method has come under scrutiny as the nonreciprocity can break down when forward and backward propagating light are simultaneously present in the device [81]. Broadly speaking, these approaches are attractive as they can be directly applied to silicon, but can be lossy, power hungry, or only operate for a specific wavelength and optical intensity.

On the other hand, magneto–optic (MO) phenomenon such as Faraday rotation is truly nonreciprocal and can be applied over a wide range of wavelength and intensity. The MO material becomes nonreciprocal when it is magnetized by a quasi-static magnetic field. In integrated photonics, synthetic garnets such as yttrium and terbium iron garnets (YIG, TIG) are commonly used due to their high Faraday rotation and optical transparency at telecom wavelengths [82]. Substituting cerium and bismuth to form Ce:YIG and Bi:YIG, respectively, have been shown to increase Faraday rotation even further, up to –4500 °/cm for Ce:YIG [83] and up to –11 000 °/cm for Bi:YIG [84]. Similar to III–V integration on silicon, the lattice and thermal mismatch create challenges for monolithic integration. Recent efforts to deposit garnets directly on silicon have been promising, with Faraday rotation approaching the performance of garnets grown on native substrates, although they often rely on techniques such as a seed layer and high temperature rapid thermal anneals (800 °C) that may be challenging to assimilate into a process flow involving III–V materials [85]–[87]. To date, the best performing nonreciprocal devices were fabricated by growing Ce:YIG on a lattice matched (Ca, Mg, Zr)-substituted gadolinium gallium garnet (SGGG) substrate, and then bonded on silicon waveguides. This ensures optimal Faraday rotation, and is compatible with III–V materials since anneals are performed at low temperature (<300 °C). Incorporating MO materials with silicon photonics enables the fabrication of devices such as isolators and circulators, providing more building blocks for complex PICs.

### A. Isolators

Optical isolators are often needed to prevent undesired reflections from reaching a laser cavity. MO-waveguide-based isolators generally use a different approach than their fiber-optic counterparts. Commercial isolators utilize a Faraday rotator to generate nonreciprocal polarization rotation when an external magnetic field is orientated parallel to the propagation direction of light. Polarization rotation in an integrated waveguide is difficult due to strong birefringence between transverse electric (TE) and transverse magnetic (TM) modes, although it has been demonstrated [88]. An alternate configuration can be used in which the magnetic field is perpendicular to the propagation direction, as depicted in Fig. 11 (Voigt configuration). Depending on whether the external magnetic field is in-plane or out-of-plane with respect to the chip, a nonreciprocal phase shift (NRPS) is present for TM and TE modes, respectively [89]. Both heterogeneous and monolithic integration are suitable for the TM case since the garnet is a cladding for the waveguide. An isolator operating for TE mode requires depositing garnet on the sidewall of the waveguide, or placing a TE–TM polarization converter prior to the isolator [90]–[92]. NRPS-based devices are fabrication tolerant and require a smaller magnetic field (50–100 Oe), since the in-plane direction is aligned to the soft axis of Ce:YIG.

Microring-based optical isolators have been demonstrated for the TM mode by bonding a Ce:YIG die directly on top of a silicon microring. A radially orientated magnetic field is needed to generate NRPS in the ring, which is done by placing a permanent magnet in the middle of the ring [93], or fabricating an electromagnet above the ring [94]. The latter approach is illustrated in Fig. 12. It is fully integrated, and switchable since the direction of the magnetic field is easily controlled. The NRPS in the ring

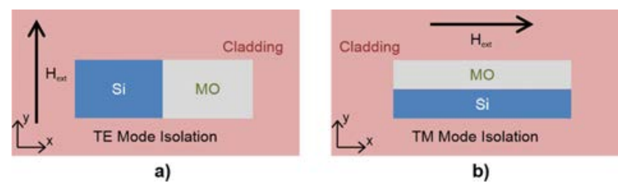


**Fig. 11.** *Cross-sectional schematic required for (a) TE and (b) TM mode isolation. In both cases, the magnetic field is perpendicular with respect to the propagation direction of light.*

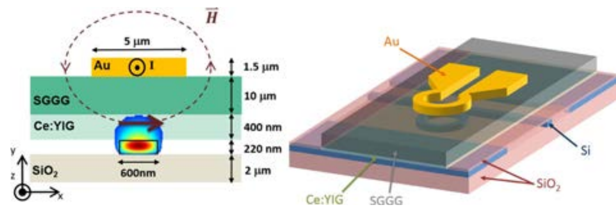


**Fig. 12.** *(a) Cross-sectional schematic and (b) perspective view of the ring-based isolator. Applying current through the electromagnet induces nonreciprocity in the ring and causes a resonance split.*

causes the clockwise (CW) and counterclockwise (CCW) propagation constants in the ring to be different, inducing a resonance split between forward and backward propagation [95]. Up to 32 dB of optical isolation was achieved using this design, with a footprint less than 0.01 $mm^2$ [96]. Multiple rings can be cascaded to achieve even higher isolation [94], although the isolation is limited to a single wavelength due to the narrowband characteristics of a ring resonator.

For applications such as sensors or WDM systems, broadband isolation may be needed, which was demonstrated using a Mach–Zehnder structure in which the Ce:YIG is bonded on the two arms of the silicon interferometer. The magnetic field in the two arms is equal but opposite in direction, creating a push–pull configuration, which shortens the length of the device. By tailoring the length and width of the silicon waveguides, broadband isolation [97] and athermal operation up to 60 °C is demonstrated [98]. If electromagnets are used to drive the two arms, the central operating wavelength of the isolator can be tuned across the entire S and C telecom bands, while maintaining 20 dB of isolation across 18 nm of optical bandwidth [99]. Future work to decrease the insertion loss of the integrated isolator (typically 7–10 dB) will bridge the gap in performance with their bulk counterparts. Thin-film, deposited permanent magnets will be used to reduce the size and eliminate any power consumption.

### B. Circulators

Optical circulators are an extension of isolators in the sense that backwards propagating light is rerouted to another port instead of being attenuated. They are necessary in applications where counterpropagating optical signals need to be separated, such as a bidirectional interconnect link [100], LIDAR or interferometric optical sensors [101]. Using a Ce:YIG clad add–drop microring, it is possible to realize a four-port circulator [88], [94]. Additional rings can be added to increase the port count. A six-port circulator was demonstrated with up to 14.4 dB of isolation and can be expanded to an arbitrary number of ports [102]. Coupled ring resonators can be used to further increase the isolation ratio.

Electromagnetically switching the radial field between pointing in and outwards with respect to the ring can reroute the optical pathways through the circulator. This was demonstrated in the six-port circulator in Fig. 13 with a time constant of 400 ps. In a device with N rings, it would possible to achieve $2^N$ different configurations with 2(N+1) port count.

MZI-based circulators have also been demonstrated, with a minimum isolation ratio of 28 dB among the ports [103]. Importantly, the design of the 2×2 couplers should be wavelength insensitive to achieve broadband operation of the circulator. The methods to expand and dynamically control the circulator could also be used here to realize complex nonreciprocal networks on chip.

## V. CONCLUSION AND OUTLOOK

We have presented an overview of the heterogeneous silicon photonics platform. Bonding allows for efficient electrically pumped light generation on silicon, solving the biggest obstacle in realizing more complex integrated photonic circuits using CMOS processes. A number of demonstrations have shown that the heterogeneous platform offers state-of-the-art device performance, in some cases outperforming native III–V devices, as it can leverage the superior processing and passive performance of the Si platform.

The ability to do multiple die bonding opens up a range of possibilities in realizing advanced photonic integrated circuits operating at a number of wavelengths, providing efficient modulators and high-speed photodetectors without a need for regrowth. With proper design it is possible to process all the components simultaneously, reducing the cost and improving the yield. As examples of advanced photonic integrated circuits, we have highlighted a fully integrated microwave generator, an integrated optical driver for interferometric gyroscope, and an optical NoC.

The increase in complexity and the number of active optical devices on an integrated chip makes the design more challenging as optical components and especially lasers are sensitive to reflections and backscattering. Heterogeneous integration allows for breaking the reciprocity

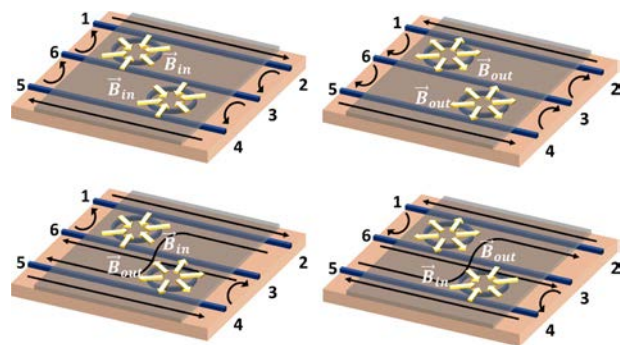


**Fig. 13.** *A schematic of a six-port circulator utilizing two microrings. In total, four independent operating configurations are possible, based on the direction of the magnetic field in each ring.*

and providing isolation on-chip by bonding magnetic materials such as Ce:YIG. The approach is very powerful and allows for switchable isolators as well as circulators.

The heterogeneous silicon technology is currently reaching maturity with first commercial products for data center market being shipped in volume and we expect that in near future it will penetrate other markets such as LIDARs, optical gyroscopes, sensing, and microwave and optical clocks as well. □

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