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Surface roughness is a key parameter for judging the performance of a given material's surface quality for its electronic application. A powerful tool to measure surface roughness is 3D laser scanning confocal microscopy (LSM), which will allow you to assess roughness and compare production and finishing methods, and improve these methods based on mathematical models.

Focus on creating high-conductivity electronic devices with minimal power loss using laser scanning microscopy is an effective tool to discern a variety of roughness parameters.

Design Rules for Addressing Material Asymmetry Induced by Templated Epitaxy for Integrated Heteroepitaxial On-Chip Light Sources

Chen Shang,* Eamonn T. Hughes, Matthew R. Begley, Rosalyn Koscica, Marc Fouchier, Kaiyin Feng, William He, Yating Wan, Gerald Leake, Peter Ludewig, and John E. Bowers

Integrating quantum dot (QD) gain elements onto Si photonic platforms via direct epitaxial growth is the ultimate solution for realizing on-chip light sources. Tremendous improvements in device performance and reliability have been demonstrated in devices grown on planar Si substrates in the last few years. Recently, electrically pumped QD lasers deposited in narrow oxide pockets in a butt-coupled configuration and on-chip coupling have been realized on patterned Si photonic wafers. However, the device yield and reliability, which ultimately determines the scalability of such technology, are limited by material uniformity. Here, detailed analysis is performed, both experimentally and theoretically, on the material asymmetry induced by the pocket geometry and provides unambiguous evidence suggesting that all pockets should be aligned to the [1 $\bar{1}$ 0] direction of the III-V crystal for high yield, high performance, and scalable on-chip light sources at 300 mm scale.

1. Introduction

Si photonic integrated circuits are expected to fulfill the soaring demand for high capacity and low-cost optical interconnects.[1] Despite the numerous successes in high performance passive Si components on 300 mm wafers,[2] integrating III-V gain elements with Si photonics is a crucial step to achieve on-chip light sources due to the indirect bandgap nature of Si and Ge. Heterogenous integration through wafer bonding, where the light is evanescently coupled to the underlying Si waveguides, is the only approach that has achieved mass production.[3–6] Monolithic integration via direct epitaxial growth is considered as the next generation integration approach as it would leverage most of the existing complimentary metal oxide semiconductor (CMOS) infrastructure, with more compact packaging and better heat sinking. The main challenge is the crystalline defects originating from material dissimilarities between III-V and Si, resulting in low device performance and reliability. Switching from a quantum well (QW) to QD active region has the advantages of superior defect insensitivity in QD active region with reduced carrier diffusion lengths[7,8] and hindered in-plane movement of dislocations due to the induced local strain field.[9] In the past few years, tremendous advances have been made in epitaxial QD devices grown on planar Si substrate. Threading dislocations (TDs) from lattice mismatch have been reduced to a density of 1×10^6 cm^{-2} within 2.55 µm of III-V grown on Si.[10] Misfit dislocations (MDs) near the active region

C. Shang, E. T. Hughes, M. R. Begley, R. Koscica, J. E. Bowers
Materials Department
University of California Santa Barbara
Santa Barbara, California 93106, USA
E-mail: shang00@ucsb.edu

M. Fouchier
Attolight AG
EPFL innovation Park, Lausanne 1015, Switzerland

K. Feng, W. He
Department of Electrical and Computer Engineering
University of California Santa Barbara
Santa Barbara, California 93106, USA

W. He, Y. Wan, J. E. Bowers
Integrate Photonics Lab
King Abdullah University of Science and Technology
Thuwal, Makkah 23955 – 6900, Saudi Arabia

G. Leake
RF SUNY Polytechnic Institute
Albany, NY 12203, USA

P. Ludewig
NAsPIII/V
GmbH
Am Knechtacker 19, 35041 Marburg, Germany

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from thermal mismatch have successfully been blocked by the inserted trapping layers.[11] Consequently, the extrapolated lifetime of epitaxially grown QD lasers on CMOS compatible planar Si substrate by molecular beam epitaxy (MBE) has exceeded 200 000 h at 80 °C.[12,13]

However, the required thick defect filtering layers elevate the QD active region to ≈3.5–4 μm above the Si substrate, preventing the evanescent light coupling to the underlying Si waveguides that are typically 1–3 um above the Si substrate. One promising solution is to deposit the III-V gain materials into etched oxide pockets in a butt-coupled configuration. The QD active region can be precisely aligned vertically to the embedded SiN or SOI waveguides in the surrounding oxide matrix during growth. This approach offers flexible placement of amplifiers and lasers, together with the densest integration of such on-chip gain elements with advanced Si photonic platforms. Both passive and active waveguide coupling have been demonstrated in such a configuration.[14,15] The first electrically pumped QD lasers deposited in narrow pockets by MBE have also been demonstrated on 300 mm Si photonic wafers with comparable reliability to those grown on planar Si substrates at a similar defect density.[16]

The eventual deployment of such integration architecture at 300 mm scale requires not only the combination of both high-quality in-pocket devices and high coupling efficiency, but also uniform device performance across 300 mm wafers. In this work, we have identified that the root cause of material non-uniformity, especially for the QD morphology in the active region, is from the pocket arrangement with respect to the III-V crystal. All pockets should then be aligned to the [1 1̄ 0] III-V crystal orientation to avoid diffusion-driven QD morphology asymmetry for high yield and scalable on-chip light sources at 300 mm scale.

It has previously been suggested that the pocket configuration would help mitigate the residual tension from the thermal mismatch,[17,18] which is proven to be the main contributor to device degradation.[11,19] Thus, in this work, we have also investigated the stress profile of the in-pocket materials both theoretically and experimentally. The residual thermal stresses, both parallel and perpendicular to the pocket, have been calculated with respect to the pocket widths. Both the calculations and measurements from polarization sensitive cathodoluminescence (CL) suggest a strong stress state difference between the two orthogonal directions. The misfit dislocation densities measured from cross-sectional transmission electron microscopy (XTEM) indicate that such stress state difference could be utilized to effectively remove the most detrimental misfit dislocation when aligning the pocket to the [1 1̄ 0] III-V orientation. Thus, the in-pocket devices would potentially experience better performance and reliability than those grown on planar Si substrates.

Growing III-V gain materials in narrow oxide pockets would be the "go-to" approach for attempting to achieve large scale monolithic on-chip light source. After investigating the pocket orientation and geometry dependent QD morphology, stress profile of the in-pocket materials, and defect configuration, we have provided unambiguous evidence suggesting that all pockets should be aligned to the [1 1̄ 0] direction with respect to the III-V crystal for optimal device yield and performance for large scale integration.
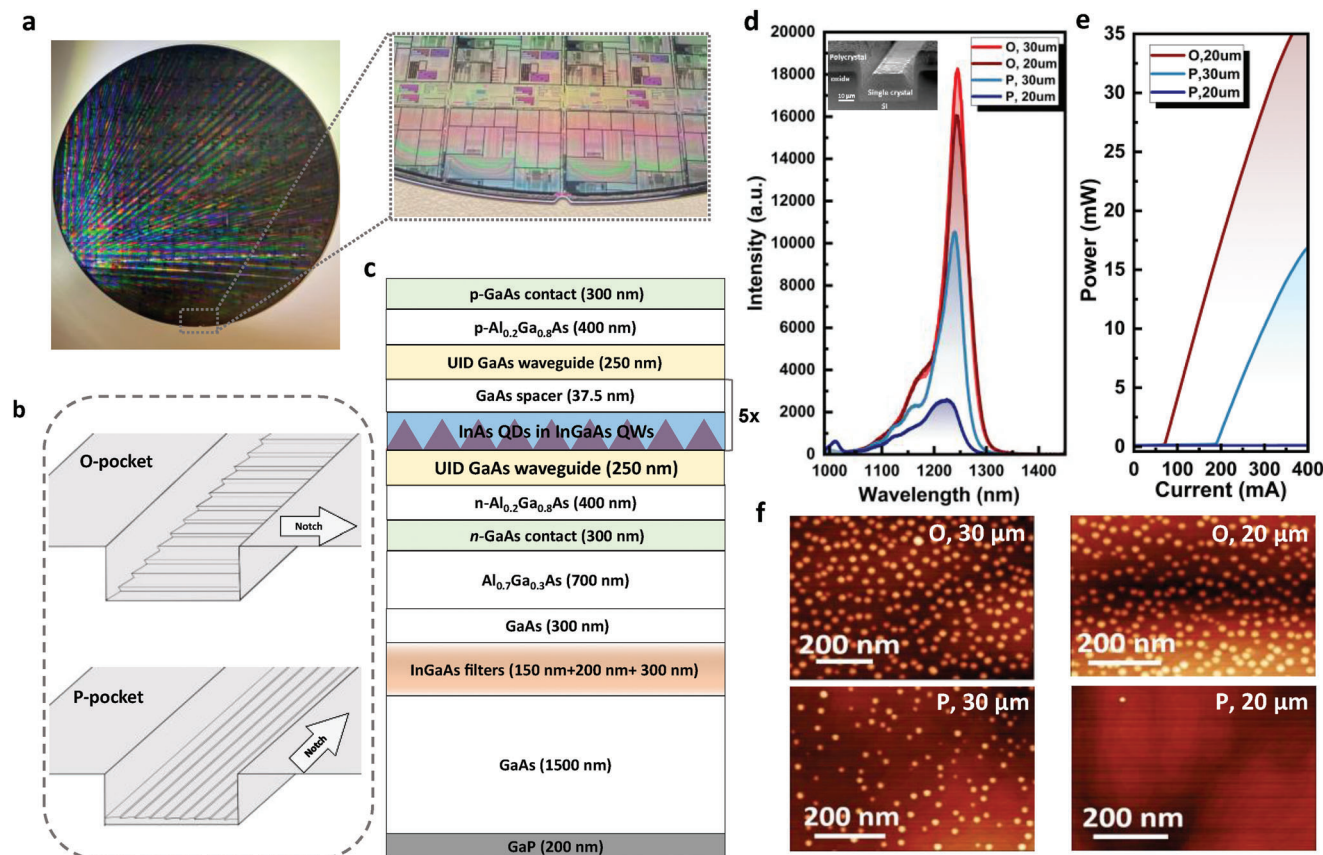
2. Results

2.1. Pocket Orientation Dependent QD Morphology

All laser samples were grown on diced coupons from a 300 mm template, described in Method, in a Veeco Gen-II solid source molecular beam epitaxy chamber equipped with indium, gallium, and aluminum as group III elements, arsenic as the only group V element, and silicon and beryllium as n- and p-type dopants, respectively. The as-fabricated patterned growth template on 300 mm SOI wafer is shown in **Figure 1**a with the "notch" direction parallel to the Si surface step edges. The growth template consists of rectangular oxide pockets both parallel and orthogonal to the "notch" direction, referred to as the "P-pockets" and the "O-pockets", respectively. Thus, the "P-pockets" are parallel to the Si substrate step edges, while the "O-pockets" are orthogonal to the Si step edges in a "staircase" configuration, schematically shown in Figure 1b.

The full laser epilayer structure above the Si substrate is shown in Figure 1c. Room temperature photoluminescent (PL) spectra of the in-pocket material, shown in Figure 1d, indicate that the material quality of the QD active region is higher in the wider "O-pockets". The corresponding laser performance, shown in Figure 1e, suggests that QDs in the narrower "P-pockets" do not provide enough gain for lasing, rendering a large portion of the wafer with no device yield for the said pocket configuration. The devices fabricated from narrower "O-pockets" also demonstrate better performance than those fabricated from wider "P-pockets". Since the growth front temperature within the pocket depends heavily on the thickness of the accumulated polycrystal on the surrounding oxide layer, and since QD nucleation process is highly sensitive to the surface temperature,[16] the origin of the QD morphology anisotropy was investigated with "half-laser" structures grown up to the active region with exposed surface dots, mimicking the growth conditions for the full laser structures.

Representative atomic force microscope (AFM) images of the in-pocket surface dots in the "half-laser" structure are shown in Figure 1f. The dot density in wider "O-pockets" is ≈6 × 10^10 cm^−2, comparable to those grown on planar GaAs or Si substrate (typically 5 to 6 × 10^10 cm^−2),[20–22] and the dot density decreases slightly in narrower pockets in the same orientation. However, the dot density drops more than an order of magnitude in the "P-pockets", with almost no observed dots in the narrower "P-pockets". This drastic discrepancy is hypothesized to result from asymmetric adatom surface diffusion, schematically illustrated in **Figure 2**a. It has previously been found that indium adatom surface diffusion is highly asymmetric due to surface reconstruction with the [1 1̄ 0] direction favored over the [1 1 0] direction due to the low-barrier pathways in the [1 1̄ 0] direction.[23]

To identify the orientation of the III-V crystal with respect to the pockets, we induce the formation of faceted trenches (FTs) in the "in-pocket" III-V strips. A test structure with a 200 nm In$_{0.18}$Ga$_{0.82}$As layer, followed by a 300 nm GaAs capping layer, was grown on the initial GaAs seed layer. Due to the high tensile strain between the GaAs capping layer and the partially relaxed In$_{0.18}$Ga$_{0.82}$As layer, FTs form in the GaAs capping layer, shown schematically in Figure 2b. The FTs elongate in the [1 1̄ 0] III-V crystal orientation due to the dislocation-mediated asymmetric

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Figure 1. a) As-fabricated 300 mm Si photonic wafers as the growth template with expanded view of the "notch". b) Schematic of the configuration of the "O-pockets" (top) and the "P-pockets" (bottom). c) Schematic of the full laser epi structure above the Si substrate. d) Room temperature PL spectrum of the as-grown material. Inset: cross-section SEM of the in-pocket III-V strip. e) Room temperature light-current (L-I) of the fabricated Fabry-Perot lasers. No laser structures were available on the mask for the "O, 30 μm" pockets. f) Corresponding AFM scans of the surface dots in the "half-laser" structure at the center of the in-pocket material. For (d), (e), and (f), "O" and "P" indicate "O-pockets" and "P-pockets", respectively. The number indicates the width of the pocket.

tensile stress relaxation, where the FTs relax excess stress in the [1 1 0] direction.[24] As shown in Figure 2c, the FTs extend along the "O-pockets" while cutting across the "P-pockets", suggesting the [1 1̄ 0] III-V crystal orientation runs parallel to the "O-pockets" and perpendicular to the "P-pockets". It is then inferred that the more volatile indium adatoms preferentially diffuse toward the sides if the strip edges are within a diffusion length given the more effective stress relaxation on convex corners.[25] Figure 2d illustrates such QD morphology evolution. The nucleated dots on the corners would then potentially evaporate via the Kelvin effect since the vapor pressure increases at convex corners as well if annealed.[26] However, the distance between the strip edge and the center is expected to be dependent on the thickness of the epi due to the formation of the slanted sidewalls.
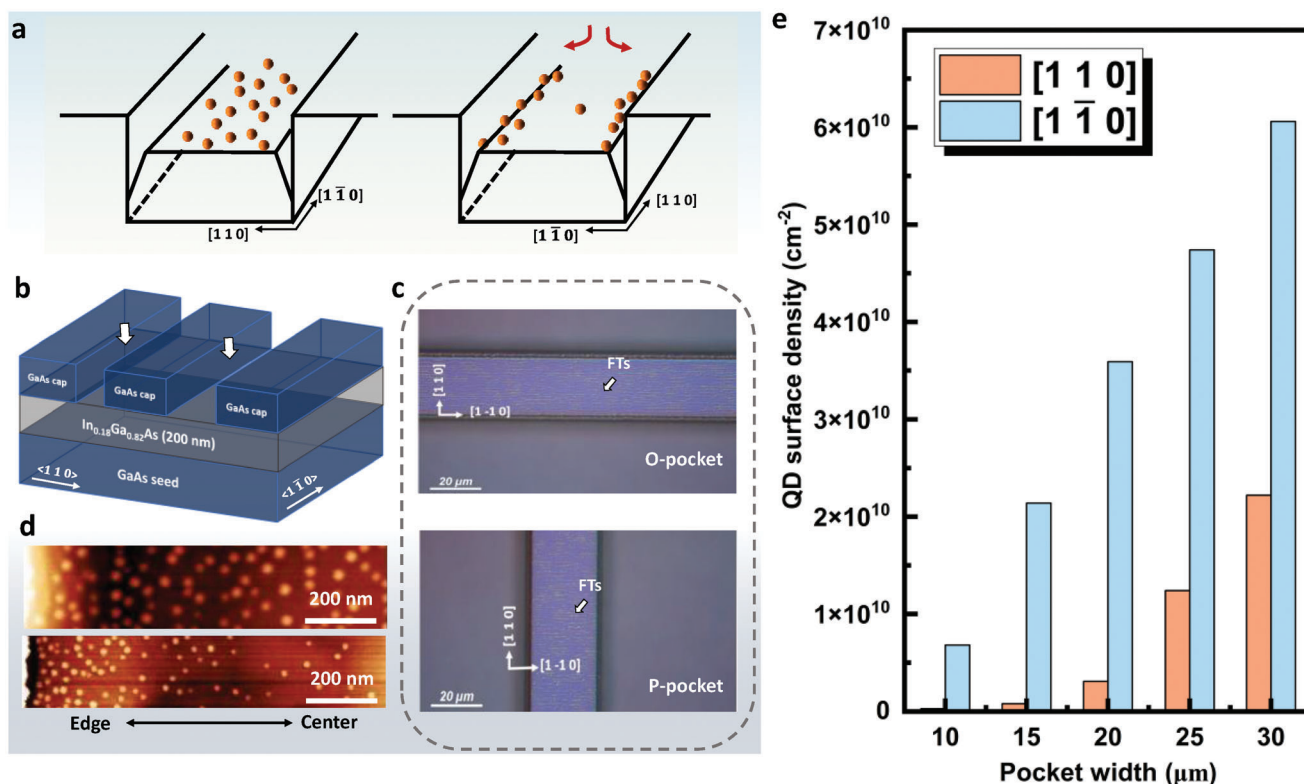
To deconvolve the possible diffusion effect from the residual stress between III-V and Si, simplified SiO₂ patterns with various pocket widths in both directions were fabricated on native GaAs substrate. The crystal orientation on the native GaAs substrate could be easily identified in situ, prior to pocket fabrication, with reflective high energy electron diffraction (RHEED). The surface dot density as a function of pocket width in both crystal orientations is summarized in Figure 2e, with dot density in the 30 μm

wide [1 1̄ 0] oriented pockets being comparable to those grown planar and patterned Si substrates. This clearly indicates that all pockets should be aligned to the [1 1̄ 0] orientation with respect to the III-V crystals to ensure high quality QD formations, and thus potentially driving higher and more uniform device yield for large scale integration of such devices. It is also clear that dot density increases as the pockets widen since the strip edges are further away. Though higher dot density is preferable for higher material gain, wider pockets inevitably reduce the integration density. Thus, a delicate balance between integration density and device performance must also be considered when designing an integration platform.

2.2. Stress And Defect Anisotropy of The In-Pocket Laser Material

2.2.1. Modeling of the in-Pocket Stress Profiles

Setting aside the QD quality, the stress state of the in-pocket laser material is expected to be dependent on the pocket geometry as well. Finite element calculations were conducted to quantify the impact of pocket dimensions on thermal misfit stresses that

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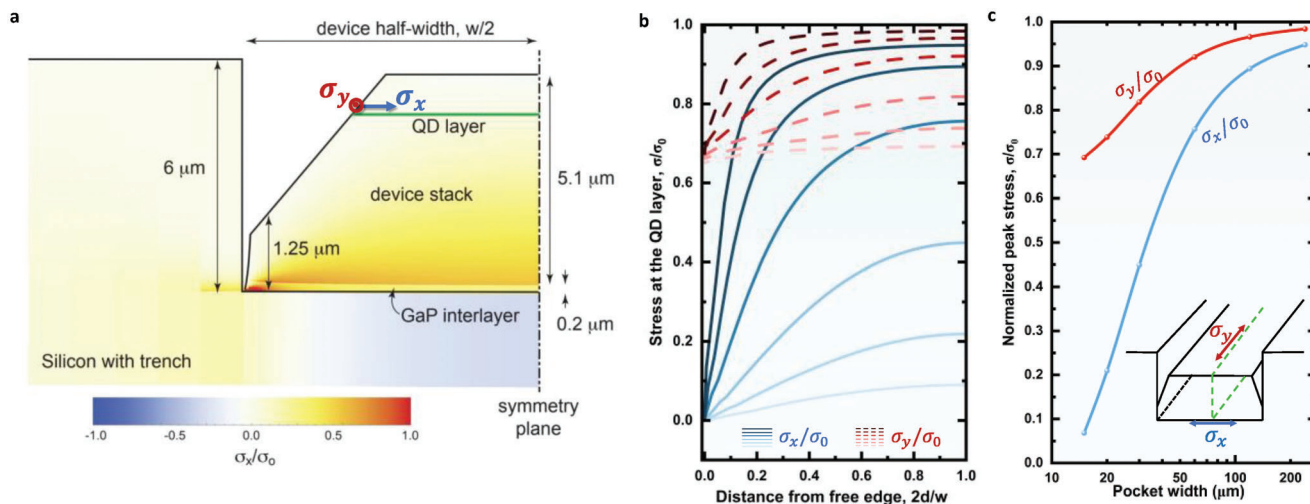MATERIALS**

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Figure 2. a) Schematic illustration of the effect of asymmetric diffusion of the adatoms. b) Schematic of the test structures for inducing FTs running in the [1 $\bar{1}$ 0] III-V crystal orientation. c) Nomarski images of the "O-pockets" (top) and the "P-pockets" (bottom), showing that the FTs are parallel to the "O-pockets" and perpendicular to the "P-pockets". d) AFM images of the surface dots near the edge of material grown in a 30 μm wide "O-pocket" (top) and "P-pocket" (bottom). e) Quantum dot density measured in pockets with various widths in both orthogonal directions patterned on native GaAs substrate.

generate new dislocation configurations. A schematic of the idealized geometry used in the analysis is shown in **Figure 3**a. The outer portions of the substrate have been truncated to highlight the device geometry. To simplify the analysis, the individual layers of the device are homogenized, such that the device (above the GaP interlayer) and the substrate have uniform properties: the elastic modulus, E, is 76 GPa, Poisson's ratio, ν, is 0.33, and the prescribed tensile misfit strain is 0.18%. The GaP interlayer is modeled explicitly with the properties $E = 88$ GPa, $\nu = 0.31$, and a tensile misfit strain of 0.12%. The Si substrate properties were taken as $E = 98$ GPa and $\nu = 0.265$ with no misfit strain. The substrate thickness and the width are sufficiently large as to have no impact on the analysis. The calculation assumes plane strain deformation, as justified by the fact the pockets are much longer than their width, and that the sidewalls are not firmly attached to the oxide. In the limit of very wide pockets, one recovers the biaxial stress in a planar layer, which corresponds to ≈240 MPa for the properties listed above and under typical MBE growth conditions for the given material stack and neglecting plastic relaxation from defect movement.[18]

Figure 3a provides a contour map of the stress distribution across the short edge of the as-grown material in the pocket, normalized by the theoretical result for stress in a planar film. The stress at the QD layer is of principal interest. The finite width of the stack and the slanted side walls reduce stresses relative

to a planar film due to the traction free surfaces along the sides of the in-pocket III-V strip. (One may note the stress concentration at the bottom edge of the device, immediately adjacent to the oxide wall. Stresses in these locations were not fully resolved as this has negligible impact on the stresses at the QD layer and depends on geometric details near the corner). The variation in stresses as one traverses the QD layer is shown in Figure 3b and the extracted peak stresses at the symmetry plane of the in-pocket material are shown in Figure 3c. The narrow pockets will significantly reduce the thermal stresses that act perpendicular to the pocket direction, especially for horizontal planes above the III-V film and the substrate interface. Stresses acting in the direction of the pocket are far less impacted, due to the fact the side walls do not relieve stresses in that direction. The modest reduction is a consequence of the effective Poisson's ratio of the stack, which provides coupling between the in-plane stresses. In the limit of very wide pockets, all stresses asymptote to the theoretical result for a planar film, as expected. It is worth mentioning that the width needed to reach this asymptotic limit depends on height of the material stack as the finite width effects are governed by the aspect ratio. The aspect ratio also determines the degree of stress relaxation as one moves vertically through the stack from the substrate, obtaining the lowest stress at the least constrained top surface. Thus, the finite element calculation results here are for the specific material stack previously shown in Figure 1c.

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Figure 3. a) Schematic of structure used in finite element analysis, with superimposed stress contour plot. Positive σ indicates tensile stress. b) Normalized stress along the QD layer as a function of fractional distance from the slanted side wall to the symmetry plane of the device, for several trench widths (from lighter to darker plots: 15 μm, 20 μm, 30 μm, 60 μm, 120 μm, and 240 μm). Stress across the trench (x-direction) and along the trench (y-direction) are shown. The x axis has been normalized to run from the free edge ($2d/w = 0$, where d is the distance from the free surface) to the symmetry plane of the in-pocket material. c) Peak stress at the symmetry plane in the QD layer as a function of trench width. The inset schematically illustrates the configuration of σ_x, σ_y, and the symmetry plane. All stresses are normalized by the theoretical result for a planar film.

2.2.2. Strain Anisotropy Measurement via Cathodoluminescence

The above calculated reduction of the overall residual tension of the in-pocket material and stress difference between the two orthogonal directions are investigated experimentally with CL via the measurements of GaAs peak emission energy shift and the degree of polarization (DOP) of the emitted light, respectively.[27] Assuming the emission energy correspond to the difference between conduction band and the weighted average of the valence band, the peak energy shift, ΔE, is proportional to the hydrostatic strain, ϵ_h.

$$\Delta E = a \times \epsilon_h \tag{1}$$

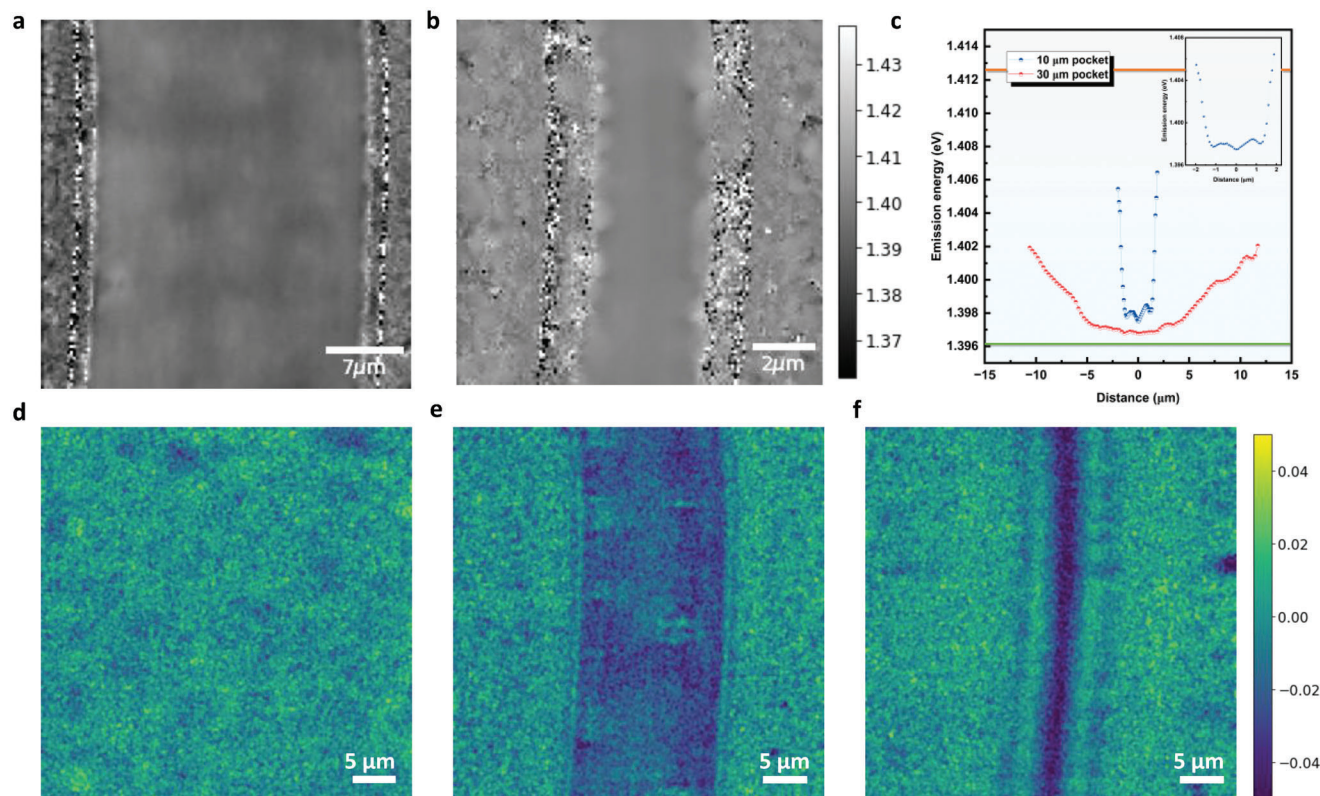The proportional constant, a, is approximately -24 eV for GaAs.[28] The emission spectra were collected top-down on an Allalin instrument from Attolight. The peak energy maps from materials in typical 30 μm and 10 μm pockets are shown in **Figure 4**a,b. The extracted peak energy profiles are shown in Figure 4c with horizontal lines indicating the peak energy of the same material stack under nominal zero stress (on native GaAs substrate) and maximum stress (on planar Si substrate). Due to the complication of the slanted III-V side wall and the existence of the polycrystal on the sidewall of the oxide, only the peak energy obtained from the flat top surface of the in-pocket material is shown. The peak residual tensile strain is ≈0.063% for the 30 μm pocket and 0.057% for the 10 μm pocket calculated from Equation 1. Materials in the narrower pocket experience a more rapid decrease of the residual strain toward the edge, thus a lower overall residual tension as modeled in Figure 3b. The numerical discrepancy between the modeled, shown in Figure 3, and the measured peak residual tension is attributed to the assumption of a free III-V sidewall. However, the details of the interaction between the in-pocket III-V and the oxide wall are beyond the scope of this work.

It is known that the degree of polarization (DOP), defined below in Equation 2, of the CL intensities is sensitive to the residual tensile strain due to the strain induced splitting of the $j = \frac{3}{2}$ heavy-hole ($m_j = \pm\frac{3}{2}$) and light-hole ($m_j = \pm\frac{1}{2}$) bands at $k = 0$.[29]

$$DOP = -C \ (\epsilon_x - \epsilon_y) = \frac{I_x - I_y}{I_x + I_y} \tag{2}$$

C is a positive calibration constant and has been measured experimentally for GaAs to be ≈50. The subscripts x and y indicate in-plane the directions perpendicular and parallel to the long side of the pocket, respectively, ϵ is the residual strain, and I is the measured CL intensity with light polarized to the indicated orientation. The transition probabilities, which determines the relative intensities, favor light polarized to the orientation with higher residual tension.[30]

The DOP measurements were performed on a modified CL tool. To distinguish light polarized perpendicular and parallel to the pocket, the CL tool was equipped with a Thorlabs WB25M-UB wire grid polarizer inserted between the collector and the spectrometer. All samples were measured in a top-down view at room temperature. The intensities from the GaAs layers were then recorded with the polarizer perpendicular or parallel to the pocket. Figure 4d-f shows the extracted DOP from the in-pocket materials and a planar substrate material as reference. While minimal DOP is observed in planar substrate materials, the DOP increases drastically as the width of the pocket decreases, suggesting a stronger stress difference between the two orthogonal directions in narrower pockets, as calculated in Figure 3 previously.

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Figure 4. Peak emission energy maps from a) a 30 µm and b) a 10 µm pocket. c) Extracted peak emission energy profile obtained in the flat area of the in-pocket material. "0" indicates the center of the pocket. The horizontal lines indicate the zero stress (orange) and the maximum stress (green) references. The inset shows the expanded view of the 10 µm pocket profile. Extracted DOP for materials from d) planar substrate, e) a 15 µm pocket, and f) a 5 µm pocket.

2.2.3. Defect Configuration via TEM

Both the above calculations from finite element analysis and the direct measurements of the stress state of the in-pocket materials suggest that the pocket geometry effectively lowers the residual tension, especially in the transverse direction. Residual thermal tension is known to be the cause of device degradation due to the formation of MD near the active region.[11,12,31] It is then expected that the pocket geometry will prove beneficial for MD reduction. To confirm this hypothesis, two XTEM foils were prepared with the foil surface either parallel ("∥") or perpendicular ("⊥") to the [1 $\bar{1}$ 0]-oriented 20 µm wide "O-pocket", shown in **Figure 5**a.

As shown in Figure 5b, cross section STEM shows the five InAs QD layers of the laser active region along with the upper InGaAs and lower InAlAs trapping layers, intended to hold misfit dislocations away from the active region. When tilting the foil about the horizontal axis into a (220) diffraction condition as shown in Figure 5c, the initially horizontal, point-like misfit dislocation becomes visible in projection, lying in plane at the outer boundaries of the QD active region and at the trapping layers. Compared to Figure 5d where the foil is oriented parallel to the pocket, it is immediately clear that the perpendicular orientation has a lower density of misfit dislocations. Measuring across the entire length of each foil, the parallel orientation has a misfit density of 1.53 µm^{-1} (44 MDs across 28.7 µm) while the perpendicular orientation has a density of 0.35 µm^{-1} (4 MDs across

11.2 µm), an approximately 4× reduction for the lower stress direction. However, since the zinc blende crystal structure lacks fourfold rotational symmetry, TDs have different glide velocities along the [1 1 0] and [1 $\bar{1}$ 0] directions resulting in differing MD densities, independent of stress asymmetries. Even so, we can compare the misfit densities measured here to those in typical planar laser samples we characterized previously where we measure misfit dislocation densities of 1.8 and 2.6 µm^{-1} along the [1 1 0] and [1 $\bar{1}$ 0] directions, respectively.[31] The asymmetry here is only 1.4×, strongly indicating that stress asymmetry accounts for a large portion of the remaining asymmetry observed in the pocket growths. The summary of the MD density comparison is shown below in **Table 1**.

We also note that the in-pocket misfit densities are lower in both directions than for the planar growth. This is

Table 1. MDs density comparison between the in-pocket and planar materials.

		⊥	∥
Number of MDs	At active region	3	34
	At trapping layer	1	10
Total MD density (µm^{-1})	In-pocket material	0.4	1.5
	On planar material	1.8	2.6
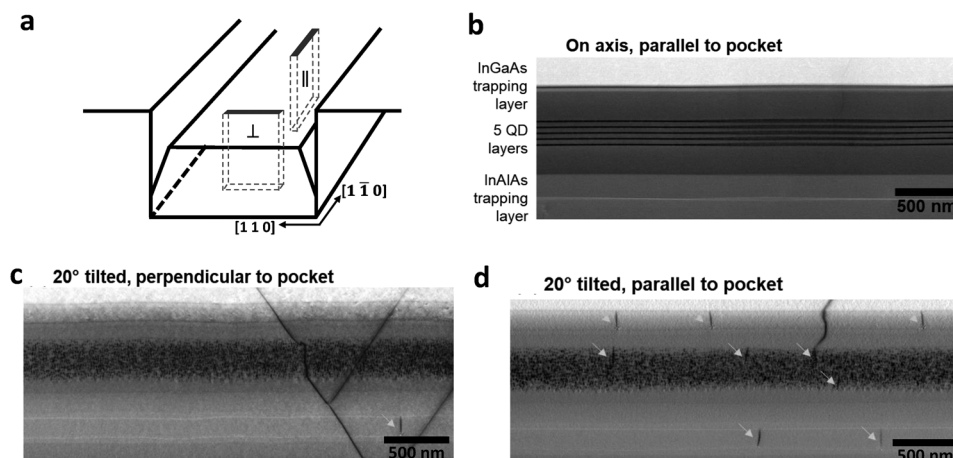
Figure 5. a) Schematic for the XTEM foil configuration. b) On axis bright-field STEM image of the active region of the laser. c) Tilting to the (220) condition for the foil oriented parallel to the pocket, misfit dislocations (indicated by yellow arrows) are visible at the upper and lower boundaries of the QD active region and the upper and lower trapping layers. d) In the foil oriented across the pocket, far fewer misfit dislocations are observed.

surprising since the threading dislocation density is approximately 10× higher in the in-pocket film compared to the planar film, which should yield a commensurate increase in misfit density, given that in the low-stress-relief regime, MD density scales approximately linearly with TD density. Instead, it appears that the stress reduction parallel to the pocket (σ_y) via the Poisson effect is sufficiently large to greatly suppress TD glide and MD formation. It has previously been found that MDs in the [1 $\bar{1}$ 0] direction that formed via tensile relaxation have a Ga-core structure, with energy states closer to the middle of the GaAs/AlGaAs bandgap than MDs in the [1 1 0] direction.[32] Experimental investigations have also revealed that MDs in the [1 $\bar{1}$ 0] direction exhibit more severe recombination enhanced dislocation climb,[31] which is considered to be a major cause of device degradation. Thus, even though the MDs running parallel to pocket (visible in the ⊥ foil) are reduced regardless of the alignment of the pocket with respect to the III-V crystal, all pockets should be aligned to the [1 $\bar{1}$ 0] direction to effectively lower the density of the most detrimental defects. With further optimization, the in-pocket devices may then surpass the performance of the state-of-the-art devices grown on planar Si substrate.

It is worth reiterating that the current patterns are aligned to the Si substrate so that the "O-pockets" are perpendicular to, and the "P-pockets" parallel to the Si step edges, previously shown in Figure 1. The [1 $\bar{1}$ 0] direction of the nucleated III-V crystal is thus perpendicular to the Si step edges. However, the orientation of the III-V crystal nucleated on Si could be flipped depending on the growth conditions.[33] Since the pockets are defined before depositing III-V materials, it's of paramount importance to calibrate the III-V crystal orientation with respect to the growth conditions prior to laying out the pockets.

3. Discussion

In summary, we have presented a detailed analysis of the pocket orientation and geometry influence on QD morphology and the stress profile of the in-pocket material, both experimentally and theoretically. All pockets should be aligned to the [1 $\bar{1}$ 0] orientation with respect to the III-V crystal for high quality QD nucleation. The same pocket orientation would conveniently help minimize the number of Ga-core misfit dislocations, the most detrimental type of defect, in the same orientation due to reduced residual tensile stress. All future integration templates should respect the same design rule for the pocket orientation for the device yield. With further improvements in the materials and device designs, one could envision that in-pocket lasers will surpass the performance and the reliability of those grown on planar Si substrates, providing the final piece for successful monolithically integrated Si photonics circuits.

4. Experimental Section

Growth Template Fabrication: Fabrication of the on-Si growth template started with depositing 4.5 µm tetraethoxysilane (TEOS) oxide on a 300 mm SOI wafer. Rectangular pockets were then dry etched down to the Si surface followed by a 2-µm Si recess for the defect-filtering buffer layers. The exposed Si sidewalls were then protected with a thin layer of SiO$_2$ to avoid lateral III-V growth. The initial 200 nm anti-phase-domain free GaP layer and the following 500 nm GaAs layer were then selectively deposited in a 300 mm MOCVD reactor at NAsP$_{III/V}$ GmbH as a seed layer.[34] The 300 mm wafer was then diced into small coupons and transferred to the above mentioned Veeco Gen-II reactor for growth studies and characterizations.

TEM Sample Preparation and Data Acquisition: Standard focused-ion beam (FIB) preparation methods were used on a FEI Helios Dualbeam Nanolab 600 to extract the TEM foils. Scanning transmission electron microscopy (STEM) was then conducted on a ThermoFisher Talos G2 with a bright field detector collection angle of 9 mrad and a beam convergence angle of 10 mrad. Each sample was tilted 15–20° along the accessible {220} condition from the ⟨110⟩ zone axis to image the horizontal misfit dislocations cutting through the foil.

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Conflict of interest

The authors declare no conflict of interest.

Author Contributions

C.S. and E.T.H. contributed equally to this work. C.S. designed this research, grew the samples, confirmed the crystal orientations, and measured QD AFM scans. E.T.H. performed the TEM characterization. M.R.B. conducted the calculation of the stress profiles of the in-pocket materials. R.K. confirmed QD density in pockets patterned on native GaAs substrate. M.F. performed the CL measurements. K.F. fabricated Fabry-Perot lasers. W.H. and Y.W. helped with AFM measurements. G.L. provided the 300 mm growth template. P.L. supervised the selective deposition of APD-free GaP. J.E.B. is the principal investigator of the research project.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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