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Towards Terabit-Scalable Silicon Photonic Short-Reach Interconnects

A dissertation submitted in partial satisfaction
of the requirements for the degree

Doctor of Philosophy
in
Electrical and Computer Engineering

by

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Veritas Omnia Vincit

Acknowledgements

First and foremost, I am obliged to acknowledge those important to me who will never read these words, as Death has been a prominent character in this period of my life. In chronological order of their passing: my paternal grandfather, Warren. My father, Roger. My paternal grandmother, Grace. My stepfather, Mike. My maternal grandmother, Jane. Some of these deaths were painfully unexpected and sudden, while others were painfully drawn out over years.

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Curriculum Vitæ

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Abstract

Towards Terabit-Scalable Silicon Photonic Short-Reach Interconnects

by

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This dissertation presents a path toward silicon photonic short reach dense wavelength division multiplexing interconnects capable of scaling to 1 Tbps with link energy consumption approaching 200 fJ/bit and areal densities exceeding 5 Tbps/mm^2 within ambient operating temperatures ranging from 20 to 80 °C. The system's architecture in the electronic and photonic domains, along with its evolution, are outlined with an emphasis on the photonic aspects. Such a transceiver photonic integrated circuit contains hundreds of photonic elements that have stringent performance requirements with regards to footprint, energy consumption, and fabrication reproducibility, among other things. As such, the measured performance of many of these photonic elements is detailed; further, methods are shown for modelling the performance of some of these components for practical design, namely elements formed using Mach-Zehnder interferometers and microring resonators.

Forming a system of that is appropriately electrically and optically interconnected to perform requires extensive packaging, which is outlined in this work with a focus on the silicon photonics chip. Co-packaging validation experiments are shown, building towards a demonstration of a discrete silicon photonic transceiver and a packaged mode-locked laser comb source at 27 Gbps per wavelength.

Finally, to further the goal of quantifying fabrication uncertainties and their impact on silicon photonic systems, this work also introduces an experimental methodology to estimate the lithographic overlay error between a waveguiding layer and another layer

capable of perturbing the guided mode; steps capable of introducing perturbations include ion implantation, etching of the waveguide layer, and deposition of material layers within close proximity to the waveguide. Such a tool should allow for more precise uncertainty quantification in photonic elements such as modulators, photodiodes, and passive mode-evolution based devices, which should in turn lead to more optimized component designs.

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Chapter 1

Introduction

With the recent explosion in popularity of artificial intelligence and machine learning applications that will only continue to demand more compute power and energy as proliferation of increasingly more sophisticated models like Chat-GPT accelerates, one thing remains clear: in order to keep up with demand with minimal environmental impact, interconnects need to be able to transmit even more capacity with a lower energy footprint [1]. We are now in the Terabit Era.

Optical interconnects are the preferred means of transmitting data at distances in excess of 1 meter, but electrical interconnects are currently the better-suited choice from a cost perspective for on-board distances and very short lengths [2, 3]. Changing this paradigm requires the development of optical transceivers that are highly compact, scalable, energy efficient, low latency, and thermally robust in terms of the underlying constituent components: integrated photonics, multi-wavelength laser source, control and driving electronics, and packaging.

Developing short reach optical interconnects faces some fundamental problems, but there are established strategies that introduce some tradeoffs. For instance, energy efficiency encourages dense wavelength division multiplexing (DWDM) with lower baud rate and simpler modulation format [4]. Lower baud rates are preferred to an extent because current ASIC internal logic clock speeds are limited to approximately 3-5 GHz, and using a SERDES gearbox to convert from low rate ASICs to higher symbol rate consumes power at each gearbox stage. This ultimately results in an maximum data rate to target before the SERDES gets too hot and negatively impacts the energy per bit consumed. Additionally, 3D integration of electronics to photonics reduces parasitics between chips and preserves energy efficiency, and the underlying electronics must be simple to reduce power.

With regards to a multi-wavelength data carrier for DWDM links, quantum dot mode-locked lasers (QD-MLLs) offer high wall plug efficiency, a flat comb, a fixed channel separation, a simple electrical pumping scheme, and a compactness that cannot be matched simultaneously by alternative options, namely distributed feedback laser (DFB) arrays and nonlinear optical frequency combs [5, 6, 7]. Some comb sources may also need to be thermally stabilized or require optical isolation; this adds to power consumption and may prevent integration of the light source onto a photonic integrated circuit (PIC) [8, 9, 10, 11]. Fiber comb sources also exist, but are comparatively much larger, require stabilization and a pump laser, and their repetition rates are too low to be practical for such an end use [12, 13].

Compactness encourages minimizing component size, placing components as close together as possible, and minimizing the number of components used. Maximizing the per-channel data rate within energy consumption limits aids compactness by reducing the number of transmit-receive unit cells needed in the system. Silicon photonics is a clear choice of platform for compact short-reach transceiver PICs due to its many features, including tight bends, high core confinement, phase shifters, modulators, photodetectors, and low-loss passive components, along with its cost effectiveness and scalability [14, 15, 16]. Key components in these silicon photonic PICs are wavelength-selective microring resonators used as modulators and WDM demux filters, as other components such as arrayed waveguide gratings and Mach-Zehnder modulators are easily orders of magnitude larger. Electronic unit cells for data encoding and reception must also be able to fit into a tight area constraint, and the 3D integration of the electronics and photonics must occur at relatively small flip chip pitches. Simple drivers with distributed logic for serialization is preferred over complex unit cells. Additionally, clocking and power distribution become challenging at tight pitches and need to be carefully managed.

Another aspect to consider is port count required to transport a given requisite capacity. Some may argue that it would be more energy efficient to have more parallel lanes and ports to cut out losses from WDM hardware. However, increasing the port count increases the footprint of the chip, and having more ports on such a short length scale can easily become unwieldy when the goal is within-the-package communications. Thus, there obviously exists a tradeoff between port count, number of channels per port, footprint, and energy efficiency. When the number of comb lines available from the laser source and the data rate per channel have reached their maximum limit, a port's capacity can be increased through multiplexing parallel data streams across fibers, polarization or modes of the fiber; polarization multiplexing comes with the benefits of using more commonly available single-mode polarization-maintaining fibers with considerably less coupling losses than compared to few mode fiber needed for mode division multiplexing [14, 17].

1.1 System Overview

Figure 1.1 illustrates the photonic architecture of the proposed transceiver. A 20-wavelength O-band QD-MLL comb source with a channel separation of 60 GHz has its outputs coupled to two separate 1 Tbps (per direction) silicon photonic PICs; the 60

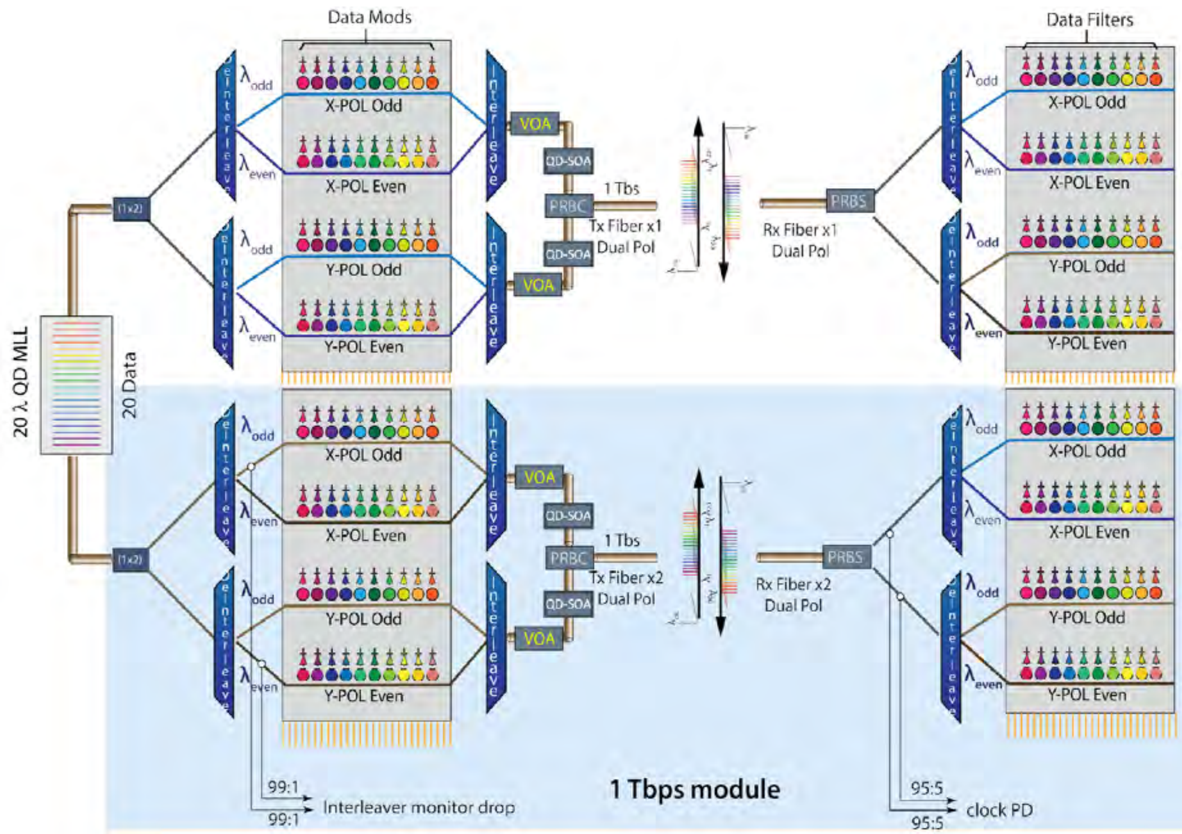

Figure 1.1: Diagram illustrating the photonic transceiver architecture of the system.

GHz channel separation chosen is set by the symbol rate to prevent cross-talk. The input comb power coupled to each PIC is split across two separate paths equally and is then deinterleaved into "odd" and "even" combs with 120 GHz channel separation that are then fed into micro-ring modulator (MRM) banks for data encoding. Deinterleaving is done both to reduce off-resonance losses by having fewer rings in series on the bus and to reduce inter-modulation crosstalk by increasing the spectral separation between channels [18, 19]. Each MRM operates at 26.4 Gbps NRZ with a 5.6 % forward error correction (FEC) overhead. A discussion on the case for FEC in compact, energy efficient links and its impact on link latency can be found in the following subsection. This modulation signal is provided by an electronic driver chip, and the ring resonances are stabilized by a controller IC. NRZ is the preferred modulation format over alternatives like PAM-4 because PAM formats are disadvantageous from energy perspective; their optical power penalty accumulates much faster than capacity gain. Coherent modulation formats are also possible to be encoded with ring modulators, but the receiver is too complex for high energy efficiency. Additionally, phase shift keying with ring modulators typically has a higher excess loss than amplitude modulation for the same ring modulator quality factor [20].

The modulated odd and even comb lines are interleaved together, and a shallow 209 MHz clock signal is encoded onto all channels for optical clock transmission via a variable optical attenuator (VOA). Optical clock transmission allows for simpler clock recovery circuitry and can reduce system power [21]. Prior proposals for optical clock transmission in similar links have allocated one of the optical channels for the data clock [22, 23]. A downside of this approach is the need for a dedicated ring site on the TX and RX that must align to one another — even when the TX and RX are at different temperatures and experienced different fabrication errors; this conflicts with the goal of minimizing power consumption introduced by DC tuning of rings.

The net-500G lanes then pass through off-chip quantum dot semiconductor optical amplifiers (QD-SOAs) before being polarization multiplexed onto a single 1T port for propagation over polarization-maintaining (PM) fiber using a polarization rotating beam combiner (PRBC); since the propagation distance is short and the carrier frequencies are in the O-Band, signal distortions due to chromatic dispersion and optical nonlinearity in fiber are negligible. It is optimal to place the optical amplification at this point in the link because it is energetically preferable to place it at a spot where optical power is already low, i.e. given desired target optical gain it will minimize optical output power which is proportional to electrical power consumption. While studies involving Mach-Zehnder modulators have shown that there are circumstances where the optical amplifier can be placed before the modulator to trade increased power consumption for a less distorted optical waveform, the power handling limits of ring modulators are likely to make this tradeoff less worthy of consideration [24, 25].

The receiver (RX) portion of the PIC first polarization demultiplexes the two 500G lanes with a polarization rotating beam splitter (PRBS); a small fraction of the power of each channel is sent to a photodiode (PD) that detects the clock signal for synchronization on the RX side of the driver IC. The rest of the power is deinterleaved, and then each individual 25G channel is demultiplexed by a ring resonator add-drop filter with a high-speed PD receiver on its drop port; the electrical output of the PD is connected to a receiver cell input on the driver IC.

As shown in the architecture, a complete optical link is composed of several photonic components that can potentially be at very different temperatures and come from different wafer fabrication lots. It is also noted that the laser, TX-side PIC and RX-side PIC can all be at physically different locations and may experience uncorrelated temperatures. However, components on the same PIC typically experience both highly correlated temperatures as well as correlated manufacturing deviations. Individual channels coming from a laser have to be aligned to the transmit side deinterleavers, modulators and interleavers, as well as to receiver side deinterleavers and channel drop filters. These have to be maintained over specified operating temperature range, which is specified for commercial grade optics as 0-70° C or a more relaxed 15-70° C [26]. Allocations must be made for fabrication-induced spread of initial component set points at a fixed temperature.

The integrated phase shifters commonly used for component alignment in silicon photonics is the heater, and it is recognized that reducing static link heater power consumption is a primary focus of increasing link efficiency [4]. There are ways to reduce static heater power consumption, such as substrate removal and optimized heater placement [27, 28]. Substrate removal may make the PIC more delicate and add complexity to packaging. Furthermore, it has recently been shown that the 3D integration of electronics onto silicon photonics with a flip chip pitch of 50 μm degrades thermal tuning efficiency by 43.4% and increases the thermal crosstalk by 44.4% [29]. These thermal tuning performance metrics are expected to further degrade with tighter flip chip pitches in the aforementioned study. Another approach is index trimming by locally amorphizing and annealing the waveguide [30]; this allows for correcting of fabrication alignment errors, but not for thermal drifts. Athermalization of elements like the ring modulator using techniques like negative thermo-optic coefficient cladding are not worth the incurred penalty to performance from reduced core confinement [31]. Overall, the most effective way to eliminate heater power would be to eliminate the need for heaters, but phase shifters of some sort are still needed. Exploring this problem will be a recurring topic throughout this dissertation.

The lasers selected for our system also have three temperature-related effects that need to be considered. First, optical efficiency generally decreases with increasing temperature, impairing overall system efficiency. Second, optical gain shifts at a rate of roughly 80 GHz/$^\circ$ C for III/V material system. Third, optical channel frequencies shift at a rate of 18 GHz/$^\circ$ C due to III/V cavity optical length changes.

Given above considerations, we performed a detailed system energy efficiency analysis of various combinations for system thermal stabilization (including manufacturing offsets) and have selected the following combination as optimal for our system design. We implement athermal deinterleavers/interleavers, ensuring that TX and RX sides are well aligned. These serve as a thermally-invariant frequency reference for the optical link. The laser is designed to operate close to the system thermal range mid-point and a thermo-electric element stabilizes temperature either by cooling or heating, as needed. This provides a good trade-off between minimizing TEC power consumption and not penalizing laser efficiency at higher temperatures. Finally, ring modulators and demultiplexers are stabilized using the free carrier plasma dispersion effect (FCPDE, colloquially referred to as electro-optic or EO throughout this work), rather than with thermal heating. The trade-offs and design considerations are described in more detail in the following chapters.

This research and proposed architecture did not occur in a vacuum, and there are several other teams presently researching this topic [16, 14, 15]. There are some commonalities among the approaches and some marked differences. All use integrated silicon photonics, and in particular ring resonators, as a common core technology for modulation and demux. As a multiwavelength light source, some use DFB arrays [16], while others use integrated nonlinear frequency combs [14, 15]. Some comb sources have a broader repetition rate that encourages band interleaving rather than odd-even interleaving [15]. Some attempt to improve thermal tuning efficiency with techniques such as local thermal isolation [27], which serves as the basis for asserting later in this dissertation that even the most optimized heaters are not energy efficient enough to be used in this application. Some reduce port count with the use of multimode fiber and mode division multiplexing rather than wavelength interleaving [14]. Overall, the largest simultaneous system capacity demonstrated among these players in the present literature is 5.12 Tbps [32], and the lowest energy consumption is claimed to be less than 1 pJ/bit [15].

1.2 Dissertation Overview

This dissertation outlines work performed in the aim to practically realize the introduced architecture for dense, energy-efficient, high capacity links. The next two upcoming chapters will focus on the theory and design of three of the fundamental components: the athermal (de)-interleaver in the former and the ring resonator-based modulator & wavelength demultiplexing (demux) filter in the latter. Chapter 4 details the performance and theory of operation of each component in the system, outlines preliminary system integration experiments, benchmarks performance based upon those system tests, and proposes methods for making an even smaller, more energy efficient system. Chapter 5 discusses efforts to experimentally quantify lithographic overlay error in silicon photonics processes and their impact on device (and ultimately system) design and performance. Chapter 6 serves as a conclusion to the dissertation topic and proposes many avenues for future work.

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Chapter 2

Athermal, Fabrication-Tolerant Si-SiN Interleaver

2.1 Introduction

As mentioned in the previous chapter, requiring compact transceiver photonic integrated circuits (PICs) urges the use of ring resonator modulators and add-drop filters to avoid demultiplexing each individual spectral channel to its own separate waveguide with the use of bulky arrayed waveguide gratings (AWGs)[1]. However, an odd/even channel (de)-interleaver may still be an element required in these links to reduce crosstalk between neighboring channels from the low quality factors of the rings utilized. The most compact, low-loss, and low-power means of achieving a (de)-interleaver is an unbalanced Mach-Zehnder interferometer (uMZI). It is important that the free spectral range (FSR) of the uMZI appropriately matches the DWDM comb source channel spacing. The uMZI must also be aligned to a fixed spectral grid, and this alignment must be maintained in the presence of perturbations in temperature; this often requires the inclusion an integrated phase shifter in the device, such as a heater.

An athermal uMZI would not require applying phase adjustments to the device as temperature changes due to the thermo-optic (TO) effect changing the phase between the arms [2], eliminating the need for a statically-on thermal phase shifter to correct for these thermal phase errors. To achieve athermality, approaches such as negative TO cladding have been demonstrated, but are not readily available in commercial silicon photonics foundry offerings and could degrade performance of other elements in the PIC, such as the high-speed RF modulators due to changing the core confinement [3, 4]. Many commercial foundry platforms include the potential for utilizing both silicon and silicon nitride waveguides [5, 6, 7, 8], so thermo-optic drifts can be reduced by designing passive elements like the uMZI in the silicon nitride waveguide, which has a TO coefficient about an order of magnitude smaller than that of silicon [9]. However, this is only a relative mitigation of thermal drift and is not capable of a true athermalization.

Additionally, these uMZIs are sensitive to waveguide fabrication errors that lead to accumulated phase offsets and require phase correction. These waveguide dimension fluctuations also introduce changes in group length imbalance that cause changes in FSR. A technique commonly leveraged to mitigate these fabrication tolerance issues is to widen the waveguide core to reduce the change in waveguide effective and group indices with core width and thickness fluctuations; however, once again, mitigation is not equivalent to achieving true fabrication invariance, and this does not offer a remedy for the magnitude of effective index change introduced by waveguide thickness fluctuations, which is relatively constant as a function of waveguide width [10].

A promising technique utilized in finite impulse response filters (in particular, uMZIs and AWGs) to ensure athermality or improved fabrication tolerances is to use dissimilar waveguides to form the interfering paths (either through different waveguide dimensions, different materials, or different modal excitations) to ensure an accumulated optical path length difference remains constant between paths of different physical lengths [11, 10, 12, 13, 14, 15, 16, 17]. Previous works have described how to achieve this compensation technique for at most two dimensions of interest at once and therefore would still require an integrated phase shifter [14, 15].

This work describes the compensation technique and its limits in detail, and measurements will be shown of an athermal Si-SiN uMZI deinterleaver on a 300 mm wafer in a silicon photonics foundry process. These devices achieve 6 times better athermality than has been previously demonstrated using a hybrid Si-SiN material system [17]. Further, this work proposes that simultaneous use of multiple core widths, materials, and modes allows for compensation of up to five dimensions of fluctuations simultaneously; this is sufficient to not require integrated phase shifters in the device if the resultant variations in FSR are within tolerances for the target application. Finally, this work outlines an approach for achieving athermal FIR filters on a silicon photonics foundry platform with FSRs sufficiently stable across a 300 mm wafer for next-generation DWDM interconnects.

2.2 Athermalized uMZI (De)-Interleaver Via Thermo-Optic Compensation

An example of a Mach-Zehnder interferometer with one input port and two output ports is shown in Figure 2.1. In the ideal case, the spectral response of an MZI in the electric field domain is a sinusoidal function impacted by the phase difference between the two interfering paths $\Delta\phi$ [18], and the two outputs will be 90° out of phase with one another:

$$\frac{E_{Out,1}}{E_{In}} \propto \cos(\frac{\Delta\phi}{2}) \tag{2.1.a}$$

$$\frac{E_{Out,2}}{E_{In}} \propto \sin(\frac{\Delta\phi}{2}) \tag{2.1.b}$$

$$\Delta\phi = \frac{2\pi}{\lambda}\Delta L_{eff} = \frac{2\pi}{\lambda}(n_{eff,1}L_1 - n_{eff,2}L_2) \tag{2.2}$$

In Equation (2.2), λ is the vacuum wavelength of the input light, n_{eff} is the effective index of a path within the MZI, and L_k is the length of one of the two interfering paths. Interfering paths with dissimilar lengths or group indices n_g will typically introduce a periodic frequency dependence on $\Delta\phi$; this period is the FSR, $\Delta\nu$:

$$\Delta\nu = \frac{c}{\Delta L_g} = \frac{c}{n_{g,1}L_1 - n_{g,2}L_2} > 0 \tag{2.3}$$

Achieving an MZI deinterleaver like the one shown in Figure 2.1 requires $\Delta\phi$ to be an integer multiple of π radians at the wavelengths of the input comb source and for the frequency separation between neighboring channels in the input comb source to be $\frac{\Delta\nu}{2}$. If these circumstances are not fulfilled, a DWDM link can incur penalties from the subsequent increased crosstalk, losses, and signal distortion.

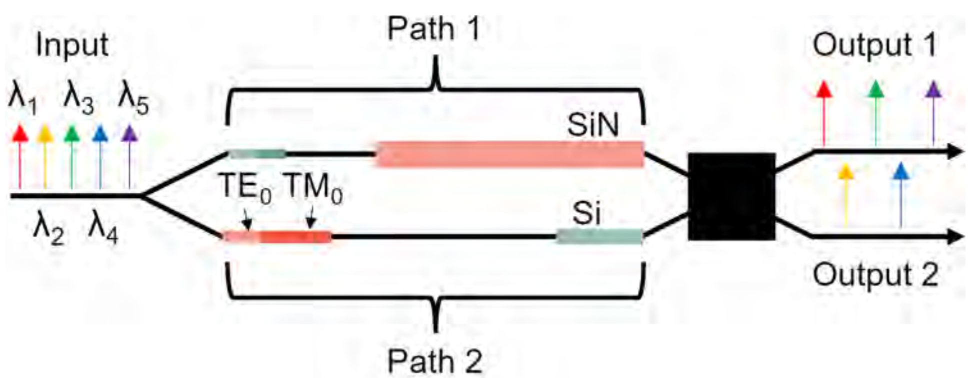

Figure 2.1: Schematic of an MZI deinterleaving an input comb of carrier channels onto two separate output waveguides. The interfering paths can consist of multiple core widths, core materials, and modes. The black box before the output is a 2x2 3 dB coupler.

Both Equation (2.2) and Equation (2.3) involve on an optical path length difference between two interfering paths: the effective length ΔL_{eff} in the former and the group length ΔL_g in the latter. Additionally, the inequality in Equation (2.3) is a convention that requires L_1 to represent the path with the longer group length in cases of finite FSR. This work will commonly refer to this as the imbalancing path throughout and refer to the other, whose length is represented by L_2, as the compensating path.

The n_{eff} and n_g of a waveguide can be susceptible to perturbations in its core geometry and temperature, leading to changes in ΔL_{eff} and ΔL_g. When temperature fluctuates, ΔL_{eff} responds in the following manner:

$$\frac{\partial \Delta L_{\mathit{eff}}}{\partial T} = \left(\frac{\partial n_{eff,1}}{\partial T} + n_{eff,1}\alpha_{Sub}\right) L_1 - \left(\frac{\partial n_{eff,2}}{\partial T} + n_{eff,2}\alpha_{Sub}\right) L_2 = A_1 L_1 - A_2 L_2 \quad (2.4)$$

The term α_{Sub} in Equation (2.4) represents the linear coefficient of thermal expansion (CTE) of the substrate and accounts for changes in the physical lengths of the paths over temperature [19]. A maximally imbalanced MZI ($L_2 = 0$) acts as one of two bounds on $\frac{\partial \Delta L_{\mathit{eff}}}{\partial T}$, which is $A_1 L_1$ m/K. When the paths are instead balanced ($n_{g,1} L_1 = n_{g,2} L_2$), the other bound of the range appears: $\left(A_1 - \frac{n_{g,1}}{n_{g,2}} A_2\right) L_1$ m/K. These bounds aid in establishing criteria on whether a particular MZI can achieve the desired tailored thermal response; in the case of athermalization ($\frac{\partial \Delta L_{\mathit{eff}}}{\partial T} = 0$ m/K), there are two criteria:

$$\left|A_1\right| \leq \left|\frac{n_{g,1}}{n_{g,2}} A_2\right| \quad (2.5.a)$$

$$A_1 A_2 \geq 0 \quad (2.5.b)$$

The length ratio of viable paths that will achieve the targeted compensation in the case of athermalization, referred to as a thermal compensation ratio R_T in this work, is:

$$\frac{L_1}{L_2} = \frac{A_2}{A_1} = R_T \geq \frac{n_{g,2}}{n_{g,1}} \quad (2.6)$$

Equation (2.6) demonstrates that a long path with a small thermal drift coefficient can be thermally compensated by a proportionally shorter path with a comparatively larger thermal drift coefficient so that ΔL_{eff} remains constant with temperature. As long as this length ratio between the two paths is greater than the balanced MZI condition, a uMZI with the target FSR can be made with the desired thermal response using Equation (2.3). Additionally, if an athermal uMZI is achievable, inverting the sign of the thermal phase drift is possible with a smaller R_T than is needed for athermality. In other words, if the original uMZI response would red shift with increasing temperature, it could be designed to blue shift to some extent. Another observation is that a balanced MZI can be designed with an arbitrary nonzero thermal phase drift coefficient, which could be leveraged to produce a broadband optical thermometer with varying thermal sensitivity. This varying thermal sensitivity would be achieved by proportionally increasing the lengths of the paths to preserve the balanced MZI state while accumulating more effective length difference for the same amount of temperature change; an effective figure of merit for such a device would be $T_\pi L_1$ (where T_π is the temperature change needed induce a π phase shift), similar to the driving voltage figure of merit used for Mach-Zehnder modulators.

Designing a component to have a compact footprint is typically valued, as doing so enables more dense photonic integration and can minimize optical losses. The most compact means to achieve the target FSR is without utilizing any compensation ($L_2 = 0$), and any tailoring of the thermal phase drift through compensation expands device footprint. A figure of merit that indicates how much L_1 increases relatively to an uncompensated design with the same FSR, denoted by ϵ, is as follows:

$$\epsilon = \frac{L_1\big|_{L_2=\frac{L_1}{R_T}}}{L_1\big|_{L_2=0}} = \frac{n_{g,1}}{n_{g,1} - \frac{n_{g,2}}{R_T}} \tag{2.7}$$

Equation (2.7) shows high R_T will result in a more compact design, which in turn

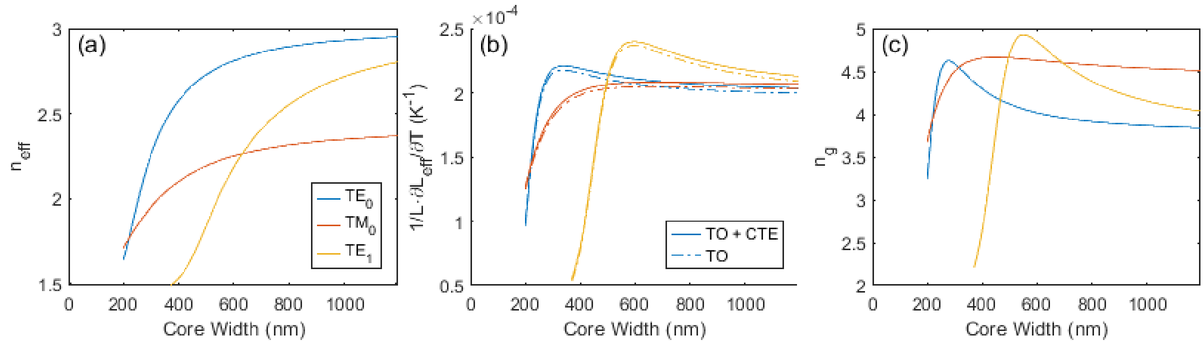

Figure 2.2: Simulation results of the effective index (a), the normalized effective optical length change with temperature (b), and the group index (c) of a 220 nm thick silicon waveguide with a top and bottom SiO_2 cladding and a silicon substrate at λ = 1300 nm.

relies on having highly dissimilar thermal drift coefficient magnitudes in the compensating and imbalancing paths. Other contributing factors that will aid in this endeavor are a high $n_{g,1}$ and a low $n_{g,2}$. However, the lower bound on Equation (2.6) suggests that R_T may be larger when the opposite trend of group indices is present.

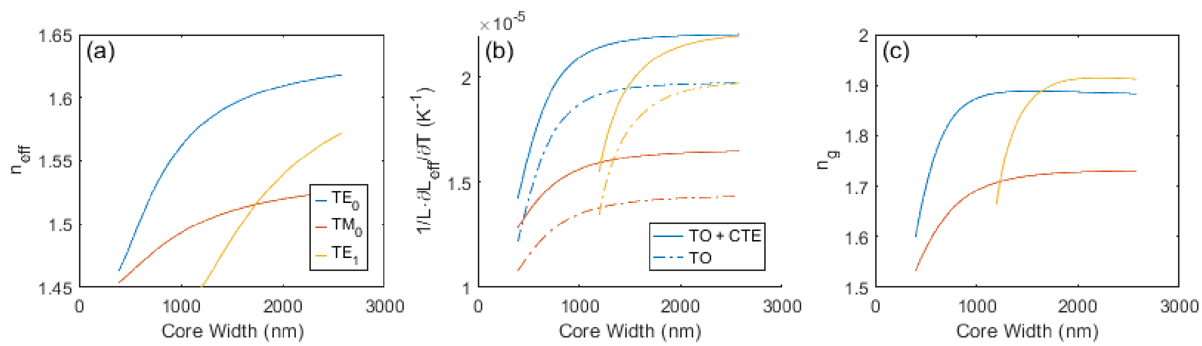

Figure 2.3: Simulation results of the effective index (a), the normalized effective optical length change with temperature (b), and the group index (c) of a 220 nm thick silicon nitride waveguide with a top and bottom SiO_2 cladding and a silicon substrate at λ = 1300 nm.

Figure 2.2 shows the Lumerical MODE simulation results for a 220 nm thick silicon waveguide needed to design an athermal uMZI for the TE_0, TM_0, and TE_1 modes. This data shows that achieving a large R_T can be challenging to do by solely utilizing different core widths and/or modes in the same waveguide material; reaching a compensation ratio of at least 2 could be possible if the imbalancing path is in a low-confinement waveguide. As mentioned previously, many silicon photonics platforms introduce a secondary silicon nitride layer for low-loss waveguiding and improved edge coupling to an optical fiber mode, and the thermo-optic coefficient of nitride is 7.8 times smaller than that of silicon [9, 2]. The simulation results shown in Figure 2.3 suggest an athermal device consisting of a silicon nitride imbalancing path that is compensated with a silicon path can be made in which $\epsilon = 1.04$ when $R_T = 10.22$ using a nitride core width of 1200 nm and a silicon core width of 400 nm. Additionally, Figure 2.2.b and Figure 2.3.b show that the CTE term is a noticeable contribution to changes L_{eff} in silicon nitride, unlike in silicon.

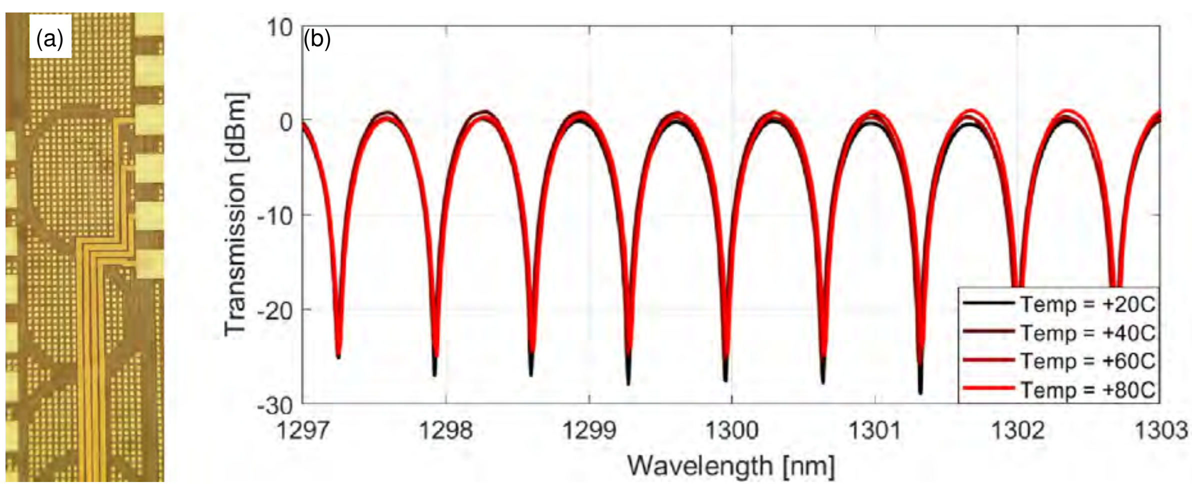

Figure 2.4: Micrograph of the fabricated Si-SiN athermal interleaver (a) and its measured spectral response over the application's spectral region of interest across the temperature range of interest (b).

Figure 2.4.a shows a microscope view of a Si-SiN thermally compensating uMZI fabricated on a 300 mm silicon photonics foundry platform with $R_T = 10.48$, and the measured spectra of such a Si-SiN athermal uMZI across temperature between 20 to 80 °C is plotted in Figure 2.4.b [20]; it is expected that this device was made with a nitride core width of 1200 nm and a silicon core width of 400 nm due to this being the default foundry waveguide core widths. This particular measured device exhibits extinc-

tion ratios greater than 20 dB, an FSR of 119 GHz, and an estimated wavelength drift is about +0.5 pm/K, showing that the chosen R_T is slightly too large in this design, as predicted previously. This magnitude of wavelength drift is about 20 times smaller than what would be achievable in a standard silicon nitride uMZI (see Figure 2.5), and the measured wavelength drift aligns well with the theoretical expectation of +0.47 pm/K. Test structures on the reticle allow for the extraction of the silicon and silicon nitride core waveguide thickness fluctuations across the wafer, the results of which are shown for half of a 300 mm wafer in Figure 2.6.a & b. The silicon waveguide thickness varies by about 4.4 nm across the wafer and the nitride layer varies by 23.7 nm. Figure 2.6.c also illustrates the computed thermal wavelength drift across the wafer in the presence of these waveguide dimension perturbations is rather stable, indicating the practicality of this compensation technique to achieve athermal interleavers at wafer-scale.

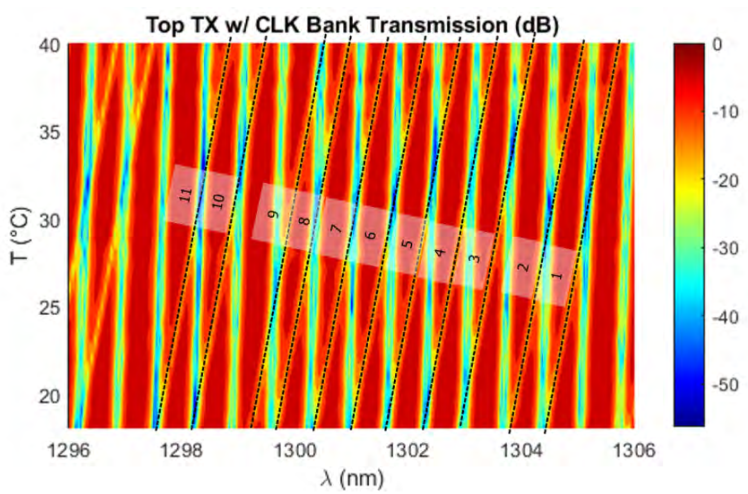

Figure 2.5: Measured spectral response across temperature for a pure silicon nitride uMZI with 11 silicon ring resonators on its output port (identified by the overlaid black dashed lines). The red lines in the trace correspond uMZI maxmia and drift at +10 pm/K.

Despite this benefit of reduced thermal phase drifts, phase changes from both of these waveguide dimensions are estimated to exceed 1 radian/nm, and phase errors from core width fluctuations are of a similar strength. Therefore, an integrated phase shifter is required in this design to meet a specified spectral grid. Additionally, these waveguide dimension tolerances introduce FSR variability, as shown in Figure 2.6.d. The measured FSR varies by 3.3 GHz across the wafer with a mean value of 117.9 GHz. In a DWDM link application targeting 120 ± 0.6 GHz, the observed amount of FSR variation requires matching a comb source with the appropriate channel spacing to minimize the impact on signal integrity of the link. Since the channel spacing of the comb source is defined by the physical dimensions of the comb source cavity and is not easily adjusted [21], this would prohibit monolithic integration of the comb source onto the PIC. Therefore, in the name of compactness and energy efficiency, a means of mitigating the fabrication errors on system performance requires investigation.

2.3 Fabrication Error Tolerance

Utilizing the same approach to achieve athermalization in the previous section to eliminate the change in effective path length difference in the presence of waveguide core width fluctuations requires that:

$$\frac{L_1}{L_2} = \frac{\frac{\partial n_{eff,2}}{\partial w}}{\frac{\partial n_{eff,1}}{\partial w}} = R_w \tag{2.8}$$

Figure 2.7.a shows how the effective index in a silicon waveguide is perturbed by core width changes. The data suggests it is possible to compensate core width changes with a high R_w by creating the path imbalance with a wide waveguide and compensating it with a narrow one [10]. This can be done by utilizing a single mode, such as the TE_0.

Similarly, compensating for effective path length changes due to change in core thickness h would require to achieving the following:

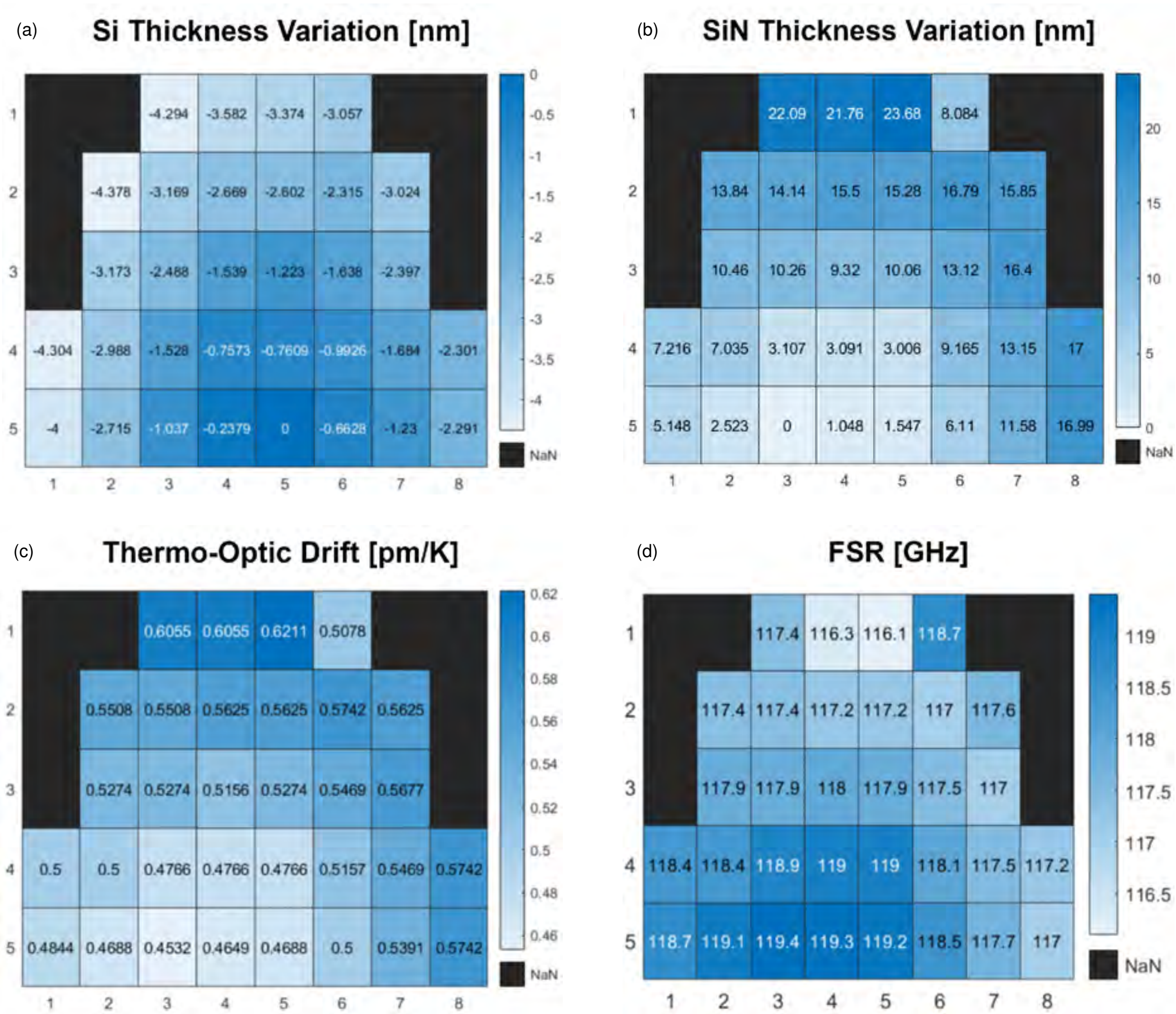

Figure 2.6: Estimated change in (a) silicon core thickness and (b) change nitride core thickness across one half of a 300 mm wafer. These waveguide varations result in the following computed TO drifts (c) in the athermal interleaver and also its measured FSR changes (d).

$$\frac{L_1}{L_2} = \frac{\frac{\partial n_{eff,2}}{\partial h}}{\frac{\partial n_{eff,1}}{\partial h}} = R_h \tag{2.9}$$

In this case study of the TE_0 mode in the silicon waveguide, Figure 2.7.b shows there is not as appreciable of a change in $\frac{\partial n_{eff}}{\partial h}$ across the range of explored core widths as there is in $\frac{\partial n_{eff}}{\partial w}$, so compensation could not be achieved with a large R_h. However, it

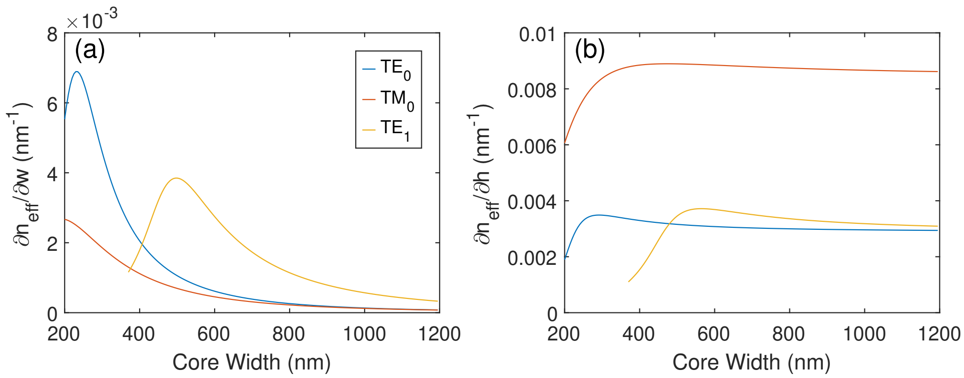

Figure 2.7: Simulation results of the effective index change with core width (a) and thickness (b) perturbations of a 220 nm thick silicon waveguide with a top and bottom SiO_2 cladding at $\lambda = 1300$ nm.

is possible to get a compensation ratio of about 2-4 by compensating a TE_0 imbalance with a TM_0 path. This can be readily achieved with the use of integrated polarization rotators [22, 23].

2.3.1 Fabrication Phase Tolerance In Two Dimensions

Attempting to ensure a constant effective length difference in the presence of both core width and thickness fluctuations would require $R_w = R_h = R_{Fab}$. This can be done in the silicon waveguide by compensating an imbalance in a wide TE_0 core (Path 1) with a comparatively narrower TM_0 core width (Path 2) at a compensation ratio of about 3. To refine the similarity of the width and height compensation ratios even further, the compensating length could utilize a small amount of one or more additional modes to create a more tailored composite drift coefficient for the overall path. Additionally, since $\frac{\partial n_{eff}}{\partial h}$ is relatively stable with respect to core width in the simulated range, there are many potential TE_0/TM_0 core width pairs that should yield similar values of $R_{Fab,Si}$. For example, Figure 2.8 shows it is possible compensate for the fabrication errors in phase of a 800 nm wide Si imbalance waveguide propagating the TE_0 mode by utilizing a composite compensating path consisting of 99.8 percent of a 480 nm wide waveguide propagating the TM_0 mode and the remainder as a 280 nm wide waveguide propagating the TE_0 mode with an $R_{Fab,Si} = 2.96$.

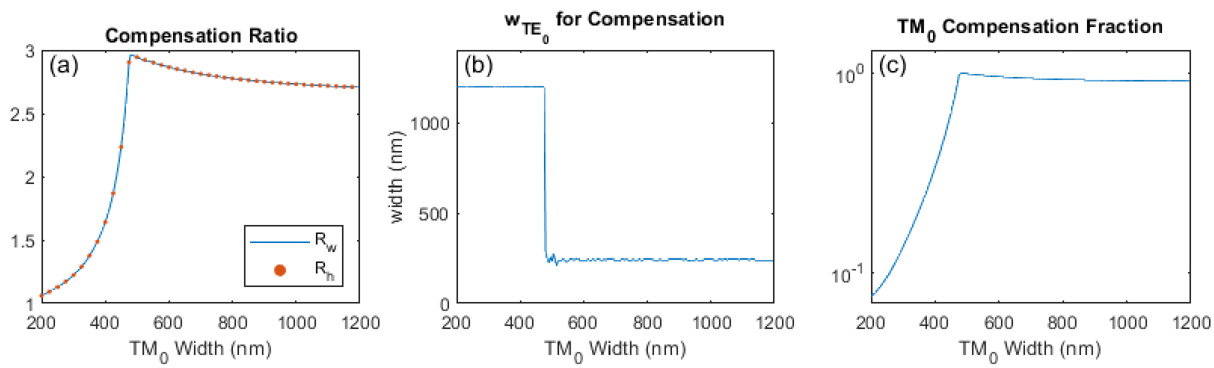

Figure 2.8: Optimizing the compensating path for both waveguide core thickness and width fluctuations of an 800-nm wide TE_0 Si 220 nm waveguide at $\lambda = 1300$ nm.

In the case of the silicon nitride waveguide, Figure 2.9.a & b illustrate that compensating either one of these waveguide fluctuations at one time is possible utilizing a single mode. However, compensating for both dimensions simultaneously would again require utilizing multiple modes. The simplest means of doing so appears to be to compensate an imbalance in a TM_0 waveguide with a primarily TE_0 compensation path. Unlike in silicon, there is only a small range over which a compensation ratio between 2 and 3 is achievable, as shown in Figure 2.9.c. Specifically, the data suggests it is possible to create the imbalance with a 500 nm wide waveguide propagating the TM_0 mode which is compensated by a composite path consisting of 98.3 percent 700 nm wide waveguide propagating the TE_0 mode and the remainder in the TM_0 mode of a 2554 nm wide waveguide. The $R_{Fab,SiN}$ of this system is about 2.41. In this regime of maximum compensation ratio, both the compensating and imbalancing paths are noticeably unconfined, which could introduce substrate coupling losses; a localized substrate etch could potentially be leveraged to mitigate these losses [24]. Alternatively, a thicker cladding could be utilized.

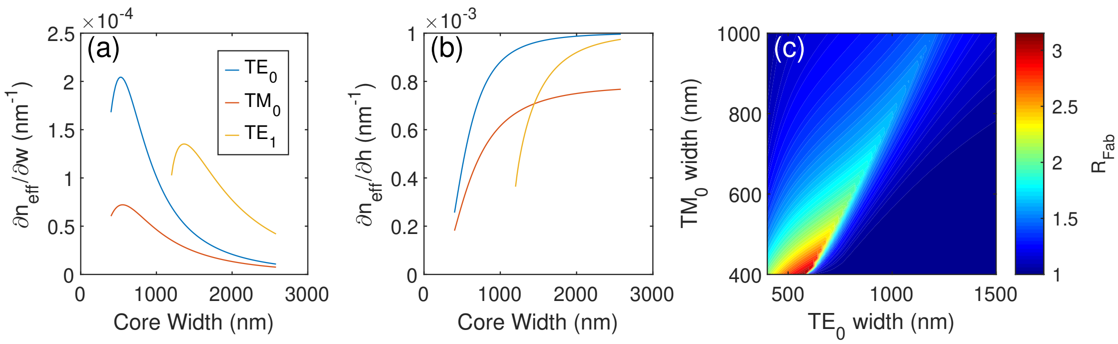

Figure 2.9: Simulation results of the effective index change with core width (a) and thickness (b) perturbations of a 220 nm thick silicon nitride waveguide with a top and bottom SiO_2 cladding at $\lambda = 1300$ nm. Contour plot searching for the optimum core width for both the imbalancing and compensating paths to maximize $R_{Fab,SiN}$ (c)

2.3.2 Simultaneous Athermality And Fabrication Phase Tolerance

Attempting to achieve athermality and fab phase tolerance in a singular material like silicon would introduce even stricter constraints on the device design, as it would require achieving three simultaneously equal compensation ratios between the two arms in a singular waveguide core material (i.e., $R_w = R_h = R_T$). Referring back to Figs. 2.2.b & 2.7.a, the TO coefficient exhibits the opposite trend of the width fluctuations where more tightly confined modes exhibit a larger slope; therefore, the silicon-only compensation ratio that achieves this goal would likely be ≈ 1. An alternative solution is to again utilize a second material to aid in achieving the athermality while compensating for waveguide dimension changes within each material layer. It is assumed the waveguide dimension changes will not necessarily be strongly correlated with one another and therefore it is not possible to compensate for the dimension errors of one waveguide layer in the other waveguide layer. This fabrication tolerant and athermal approach can be done with the same silicon-silicon nitride material system utilized throughout the work with the modes and waveguide dimensions utilized in the previous subsection to achieve waveguide core dimension compensations, along with their dictated fabrication compensation ratios. The resulting uMZI would look similar to the one shown in Figure 2.1 except with differences in mode utilization. A silicon nitride fabrication imbalancing path is present in Path 1 which is compensated in Path 2; the path assignments are reversed for the silicon waveguide fabrication compensation. Overall, Path 1 acts as the thermal compensation's imbalancing path and Path 2 as its compensation path. The corresponding path lengths would be as follows:

$$L_1 = \frac{L_{Si}}{R_{Fab,Si}} + L_{SiN} \tag{2.10.a}$$

$$L_2 = \frac{L_{SiN}}{R_{Fab,SiN}} + L_{Si} \tag{2.10.b}$$

Revisiting Equation (2.6) shows that athermality requires the following material length ratio to hold:

$$\frac{L_{SiN}}{L_{Si}} = \frac{A_{Si,2} - \frac{A_{Si,1}}{R_{Fab,Si}}}{A_{SiN,1} - \frac{A_{SiN,2}}{R_{Fab,SiN}}} \tag{2.11}$$

To clarify Equation (2.11), $A_{Si,1}$ is the weighted average thermal effective length scaling factor for all silicon waveguides present in Path 1. The composite TO coefficients from fabrication compensation lead to a thermal compensation ratio of about 2.22 with composite group indices $n_{g,1} = 1.6186$ and $n_{g,2} = 2.0036$. These parameters show that while simultaneous athermalization and fabrication compensation is possible in this design, there is a considerable thermal compensation ratio penalty compared to solely achieving athermalization. This is due to the fact that the ratio between L_{SiN} and L_{Si} is about 24.18 compared to 10.48 in the measured athermal-only devices; the comparatively low $R_{Fab,SiN}$ leads to the TO compensation being primarily conducted in the nitride waveguide rather than in silicon, expanding device footprint.

2.3.3 FSR Stability

An important constraint on DWDM (de)-interleavers is a precisely-fabricated FSR to match the data carrier frequency separation. Although phase changes at one instantaneous wavelength are designed to be appropriately compensated in the uMZI outlined in the previous section, this does not necessarily imply the compensation stabilizes the group length path difference, as it is also affected by how the waveguide dispersion changes with these fluctuating parameters. Analyzing how one of these variables of concern, such as nitride waveguide core thickness, contributes to FSR instability can be done via the following:

$$\frac{\partial \Delta\nu}{\partial h_{SiN}} = \frac{-\Delta\nu^2}{c}\frac{\partial \Delta L_g}{\partial h_{SiN}} \tag{2.12}$$

Figure 2.10 shows the simulation results for group length scaling factors with perturbations in both silicon and silicon nitride. Thermal expansion of the substrate is once again accounted for with changes in temperature as in the effective path length case; its impact on silicon is negligible, but it is a noticeable contribution to the silicon nitride waveguide.

Table 2.1 summarizes both phase and FSR variability due to perturbations in waveguide dimensions and temperature for a series of interleaver designs, both uncompensated and compensated in the ways previously outlined in this work; the uncompensated Si and SiN results utilize the TE_0 mode with core widths of 0.4 and 1.2 μm, respectively, and $L_2 = 0$. For the outlined simultaneously athermal and fabrication phase-tolerant design at the target FSR of 120 GHz, the estimates of variable-dependent FSR drift indicate that the primary concern is nitride waveguide thickness, which is also true in the solely

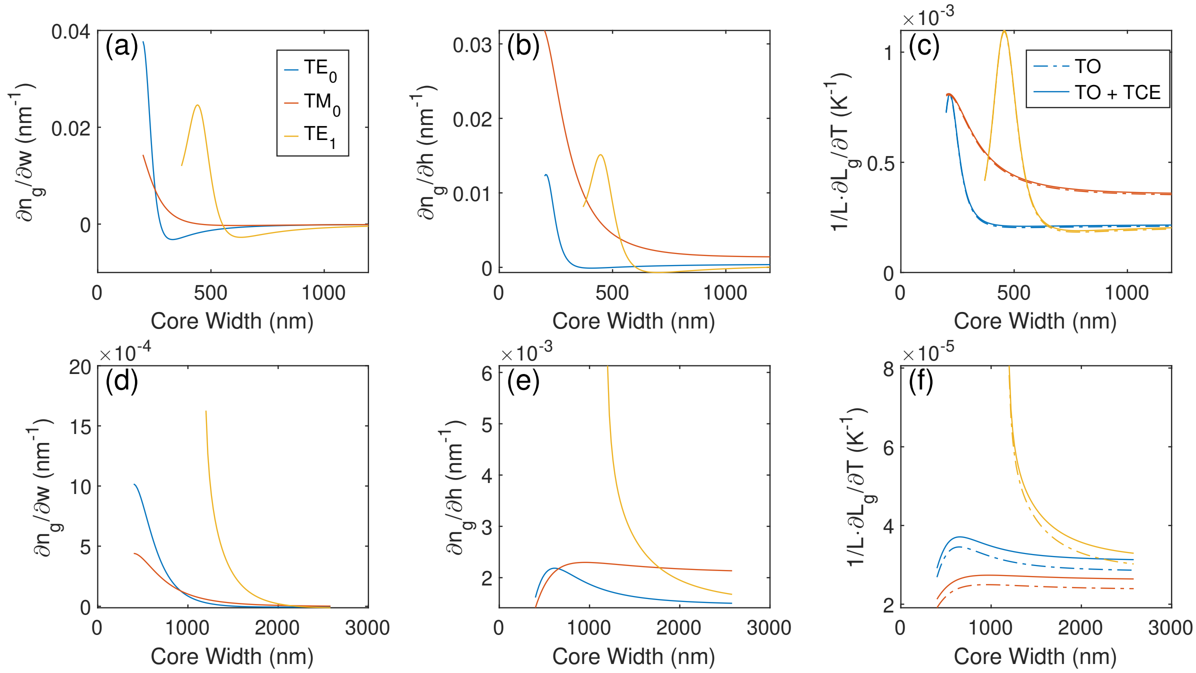

Figure 2.10: Simulation results of the group index change with core width and thickness perturbations and temperature change of 220 nm thick silicon (a-c) and silicon nitride (d-f) waveguides with top and bottom SiO_2 cladding and a silicon substrate at $\lambda = 1300$ nm

athermal design in previous sections and the uncompensated nitride-only uMZI. The table also shows that introducing fabrication phase tolerance increased the magnitude of the nitride thickness FSR drift by 14 percent relative to the athermal design and by 45 percent of the uncompensated design, which could be sufficient for some applications. However, the target application requires the containment of FSR fluctuations to accumulate overall less than 600 MHz; given the estimates of waveguide thickness fluctuations in Figure 2.6.a & b, that is unlikely to be assured across a 300 mm wafer without changing the design approach and instead compensating for group length differences rather than effective length differences. Figure 2.10.e shows that the modes selected for phase compensation in Section 3.1 are not a viable choice for a high compensation ratio for FSR stability. Instead, compensating either a TE_0 or TM_0 imbalance with a TE_1 waveguide section should be able to achieve compensation ratios as high as about 2.7 and 3.5, respectively.

The performance of an interleaver where the imbalancing nitride path utilizes the TM_0 mode compensated primarily by TE_1 is outlined in the final entry of Table 2.1. Since there are now phase fluctuations due to nitride thickness tolerances of about 1.7 radians/nm and it is estimated the nitride thickness can vary by 23.7 nm across a wafer (as this was the absolute range of thickness on the wafer measured in this study), the phase of this device has once again become highly fabrication sensitive. Therefore, there is not a need for phase compensation for waveguide dimensions in the silicon, especially when device compactness is a concern. Such a device has an FSR which is suitably stable for the target application, and there is not a need to revise the design to compensate for FSR changes due to silicon waveguide dimensions. However, as noted, the stability of the phase response with waveguide dimensions is lost in the process; phase errors can be fixed with an integrated phase shifter but FSR errors cannot, so it makes sense to prioritize FSR stability. The downside is the continued incursion of an integrated phase shifter with a static power draw unless a means like waveguide index trimming is utilized [25], or unless a lower-power phase shifter technology is introduced [26]; however, the latter option is likely more disruptive to an established process than the former while also potentially requiring external feedback loops and having a limited tuning range. For future DWDM links with highly stringent energy budgets, any use of a heater is too energy consumptive, as some of the most efficient heaters would require allocating up to 7.2 percent of the entire system energy budget solely to tuning uMZIs in some architectures when energy consumption is limited to 0.1 pJ/bit [1, 27, 28]. Regardless of method implemented to overcome the fabrication-induced phase error hurdle, care will need to be taken to ensure this does not introduce a new means of FSR or TO phase fluctuations.

Material(s) *Compensated Variable(s)*	$\frac{\partial \Delta\phi}{\partial T}$ (rad/K)	$\frac{\partial \Delta\phi}{\partial w}$ (rad/nm)	$\frac{\partial \Delta\phi}{\partial h}$ (rad/nm)	$\frac{\partial \Delta\nu}{\partial T}$ (MHz/K)	$\frac{\partial \Delta\nu}{\partial w}$ (MHz/nm)	$\frac{\partial \Delta\nu}{\partial h}$ (MHz/nm)
Si	0.62	5.8	9.3	6.2	-66	-2.9
SiN	0.14	0.4	6.0	2.1	1.8	110
Si/**SiN** $\Delta\phi(T)$	0.0047*	-1.7 **0.6**	-2.7 **7.7**	1.0	19 **2.4**	0.8 **140**
Si/**SiN** $\Delta\phi(T, w_{Si}, h_{Si}, w_{SiN}, h_{SiN})$	0	0 **0**	0 **0**	1.1	1.9 **40**	9.7 **160**
Si/**SiN** $\Delta\phi(T)$, $\Delta\nu(w_{SiN}, h_{SiN})$	0	-0.1 **0.5**	-1.7 **1.7**	-1.0	1.8 **0**	-1.4 **0**

Table 2.1: A comparison of various modelled 120 GHz FSR interleaver designs and their susceptibility to phase and FSR deviations in the presence of changes in temperature and waveguide dimensions. An asterisk denotes a value taken from measurement. In an interleaver design with multiple materials, a bolded value in some fields denotes the parameter in silicon nitride. The compensation ratios, modes, materials, and core widths utilized for each device are listed throughout this work.

2.4 Discussion

This compensation technique as outlined has the narrow focus of compensating perfectly at one wavelength of interest; the quality of the compensation will degrade for large offsets from the target wavelength due to dispersion. In a DWDM system occupying approximately 1.2 THz of spectral bandwidth, this is not a primary concern, as demonstrated in the spectra shown in Figure 2.4. In circumstances where a broader wavelength span is needed, compensating for FSR drifts and phase errors simultaneously would aid in making the compensation's effects more broadband, and the limiting factor for spectral stability of the compensation would become second order dispersion. Alternatively, it may be possible to compensate for phase drifts at more than one wavelength by utilizing a wider linear combination of slightly different waveguide cores for each mode. However, both of these approaches are likely to result in a degradation in compensation ratio in the process.

Another caveat is the analysis assumes a uniform field of change. In a practical system, it is possible to have a non-uniform heating or a non-uniform device dimension fluctuation across the uMZI. A maximally compact implementation of the device results in the uniformity approximation being more valid, but there may be circumstances under which compactifying will not mitigate non-uniform perturbations, especially when it comes to temperature. Since different waveguide materials and geometries will have different thermal impedances and time constants, the various distinct regions of the device could be at different temperatures; since the model predicts the measured wavelength drift in the fabricated device rather well, this does not seem to be an issue within these measurements. However, this effect could be more pronounced in a time-varying temperature field and increasing the thermal time constant of the waveguides through substrate isolation [28]. Self-heating of the waveguides could also occur when the input power is high and approaching its power handling limits, which is likely to occur at lower powers in silicon than silicon nitride due to the relatively large two photon absorption coefficient in silicon [29, 30]; for example, a 2 pm red shift was observed in the spectrum of the measured device when the input power was 20 mW. In cases of high input power, it is expected to merely behave as a phase offset relative to low power and can be accounted for in circumstances when the time-average input power is stable relative to the thermal time constant of the device (e.g., CW inputs and high-speed amplitude modulation interconnnects) and nonlinear loss thresholds have not been achieved. Overall, extensive modelling and statistical simulation may yield more accurate results for a particular application[31]. Additional phenomena that would potentially be of interest to introduce in a more detailed model include verticality of waveguide sidewalls and the stress-optic effect [32, 19].

Successful utilization of path imbalance compensation with the means outlined in this work hinges on maintaining pure polarization states in multimode waveguides and conducting mode conversions in compact footprints with low loss and sufficiently broadband response. Compact bends in the required modes are also of interest to reduce device footprint. Advances in optimization techniques will likely aid in improving these factors [33, 34].

The transitions between waveguide layers is done via evanescent couplers between both material layers, and some of the other required mode transitions also benefit from being comprised of multiple waveguide layers. These elements could be susceptible to errors introduced by fluctuations in the oxide thickness between the two waveguide layers along with overlay error between the two layers [35]; this in turn can lead to variability in their L_{eff} and L_g. It is therefore possible that an optimal approach to placing mode converters would be to locate those of a similar type (i.e., all requisite silicon TE_0 to silicon nitride TE_0 converters) as close to each other as possible and oriented along the same axis so that their group and phase lengths are as close to identical as possible, minimizing their impact on the device response.

Finally, there may be degrees of freedom remaining to be leveraged for improved performance that went unexplored in this work. For example, hybrid modes that use both core materials would produce a mode that is susceptible to changes in both material layers; however, as mentioned during discussion of multi-waveguide mode converters, this raises the possibility of susceptibility to intermediate cladding material thickness and inter-waveguide overlay error variations that would possibly also require compensation if utilized. Secondly, if a stable, uniform shallow etch is available, waveguide thickness could become an added dimension to leverage.

2.5 Conclusion

An exploration was conducted of the theory of engineering phase and group length imbalance within an uMZI to achieve a targeted performance in the presence of changes in temperature and waveguide dimensions via use of different waveguide geometries, excited modes, and core materials; additionally, leveraging a combination of these methods simultaneously has been proposed to allow for compensating for changes in up to five of these dimensions at the same time with greater ease. The model utilized accounts well for the thermal phase drifts measured in a fabricated device. Further, with a minor amount of process development, an outline is provided on how one might achieve simultaneously athermal and fabrication-tolerant FIR filters suitable for highly energy efficient and compact DWDM links on a 300 mm silicon photonics foundry platform.

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Chapter 3

Ring Resonators

3.1 Introduction

Silicon photonic microring resonators are of great interest due to their compact size, low power consumption, and scalability into wavelength division multiplexed (WDM) transceiver PICs. This chapter first serves as a tutorial for the fundamentals of ring resonator properties, as much of the outstanding literature does not unify variable definitions or outline what concepts are based on approximations and the limits of the validity of expressions. Integrated phase shifters for high speed communication applications will then be discussed. While several works have explored means to accurately model single-bus ring modulators, describing microring modulators with a drop port has received significantly less focus [1]; this chapter remedies this by developing both large signal and small signal models that capture the effects of the drop port. The model equations will guide a design flow of both a ring modulator and wavelength demux filter based on a process in a silicon photonics foundry MPW offering; considerations will be made for both individual rings in isolation and their interactions with each other in a system outlined in the introduction chapter.

3.2 Modelling

This section outlines the expressions and methodologies used to describe the ring resonator and its figures of merit in general and specifically to their use communication links. Since there are two main methods to derive a description of a ring resonator, this section will discuss the applicability of each to particular problems. This section will also cover modelling of integrated phase shifters and their impact on device performance.

3.2.1 Steady State

First, the behavior of the ring resonator will be explored in the simplest case: when all the input parameters are time-invariant. Such a scenario is illustrated in Figure 3.1. A ring resonator is at its core a directional coupler (with field transmission coefficient σ and coupling coefficient κ) that has one of its outputs connected to an input [2]. This produces feedback of light coupled into the cavity, accumulating phase ϕ and loss a while propagating around the ring, that interferes with transmitted light when coupled back onto the other output port. The ring can have more than one coupler connected to it (commonly referred to as an add-drop ring resonator); the extra coupler provides additional utility to the ring by allowing light to be diverted to another waveguide path (”dropped” when taken off a primary path and ”added” when placed onto one). Add-drop ring resonators, their utility to drop light, and how the addition of the drop port perturbs established models will be of primary focus for this chapter.

3.2.1.1 Travelling Wave Model

The transmission function for a ring resonator can be derived by adding together all the paths light can take to reach the same spot in the system [3]. For the through port response, some light initially is not coupled into the ring, and some fraction of the light

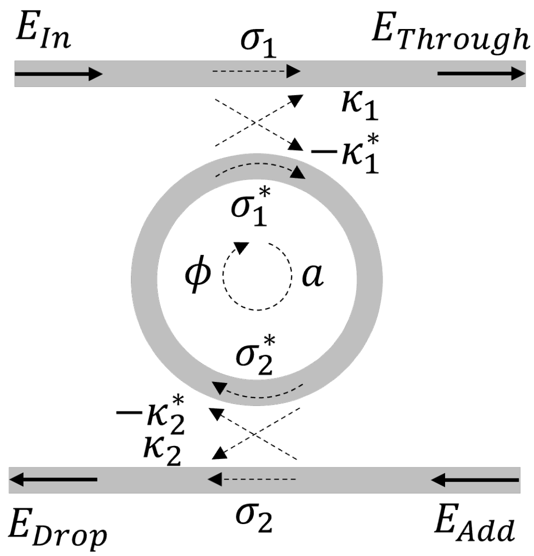

Figure 3.1: Schematic of an add-drop ring resonator.

that was coupled into the cavity is attenuated by losses and accumulates phase from a traversal of the cavity, partially coupled onto the drop port, and partially coupled back out onto the through port; since some ever-shrinking fraction of light will always remain in the cavity after each pass around the ring, this summation is an infinite series. To aid in simplifying the expression for the though port response, the couplers are assumed to be lossless such that $|\kappa|^2 + |\sigma|^2 = 1$ [2]; it should be noted that the lossless coupler approximation breaks down for rings formed with tight bend radii and with small separations between the bus and ring waveguides in the coupling sections [4].

$$\frac{E_{Through}}{E_{In}} = \sigma_1 - |\kappa_1|^2 \sigma_2^* a \mathrm{e}^{j\phi} \sum_{k=0}^{\infty} (\sigma_1^* \sigma_2^* a \mathrm{e}^{j\phi})^k = \frac{\sigma_1 - \sigma_2^* a \mathrm{e}^{j\phi}}{1 - \sigma_1^* \sigma_2^* a \mathrm{e}^{j\phi}} \tag{3.1.a}$$

$$\frac{E_{Drop}}{E_{In}} \approx -\kappa_1^* \kappa_2^* \sqrt{a \mathrm{e}^{j\phi}} \sum_{k=0}^{\infty} (\sigma_1^* \sigma_2^* a \mathrm{e}^{j\phi})^k = \frac{-\kappa_1^* \kappa_2 \sqrt{a \mathrm{e}^{j\phi}}}{1 - \sigma_1^* \sigma_2^* a \mathrm{e}^{j\phi}} \tag{3.1.b}$$

$$\frac{E_{Circ}}{E_{In}} \approx -\kappa_1^* \sigma_2^* a \mathrm{e}^{j\phi} \sum_{k=0}^{\infty} (\sigma_1^* \sigma_2^* a \mathrm{e}^{j\phi})^k = \frac{-\kappa_1^* \sigma_2^* a \mathrm{e}^{j\phi}}{1 - \sigma_1^* \sigma_2^* a \mathrm{e}^{j\phi}} \tag{3.1.c}$$

$$a = e^{\frac{-\alpha L}{2}} \tag{3.1.d}$$

In Equation 3.1.d, α is the waveguide loss in units of m^{-1}.

The power and phase response of the through and drop ports are plotted in Figure 3.2. In terms of power, it is a Lorentzian lineshape function that is spectrally periodic with ϕ that has a free spectral range $\Delta\nu$, much like the unbalanced MZI discussed in Chapter 2. In a ring resonator, $\Delta\nu$ is proportional to the group length of the path around the ring rather than to the difference of group lengths between two paths; in the point coupler approximation, the group length difference can be thought of as the group length of the resonator interfering with the transmitted light of the point coupler that has travelled no additional distance. Generally speaking, κ, σ, and a are also wavelength dependent; κ typically increases for longer wavelengths in the same waveguide geometry due to decreased core confinement [5].

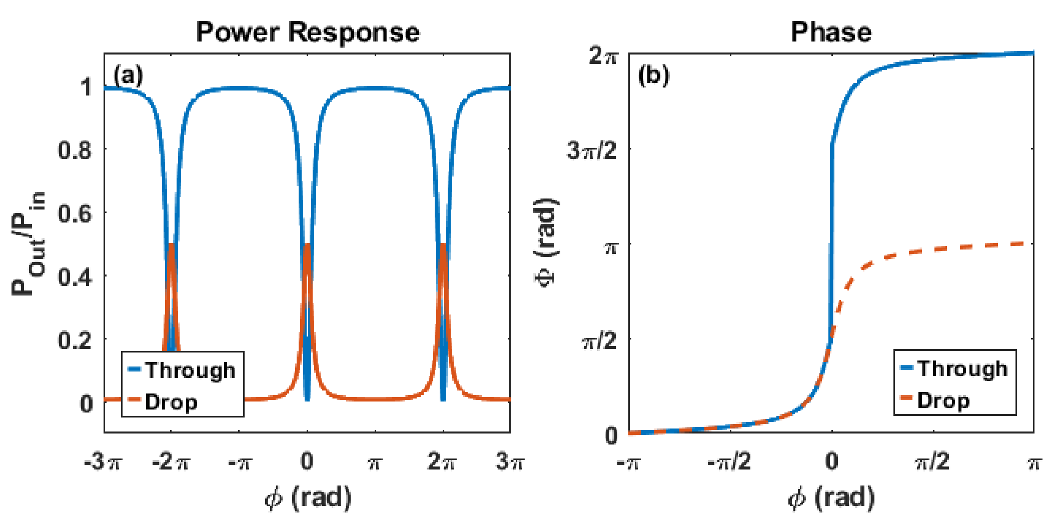

Figure 3.2: Power (a) and phase (b) response an add-drop ring resonator for which $\kappa_1 = 0.45$, $\kappa_2 = 0.31$, and $a = 0.95$.

The square root term in the drop port field response reveals an additional assumption: that the drop coupler is placed halfway along the circumference of the ring away from the input coupler. More generally, the transfer function can be written as:

$$\frac{E_{Drop}}{E_{In}} = \frac{-\kappa_1^* \kappa_2 a^{\psi_a} \mathrm{e}^{j\psi_\phi \phi}}{1 - \sigma_1^* \sigma_2^* a \mathrm{e}^{j\phi}} \tag{3.2}$$

$$\psi_a = \frac{1}{\ln(a)} \int_0^{L_{Drop}} \frac{\alpha(L)\,dL}{2} \tag{3.3}$$

$$\psi_\phi = \frac{2\pi}{\lambda\phi} \int_0^{L_{Drop}} n_{eff}(L)\,dL \tag{3.4}$$

An interesting observation is that if the drop coupler were placed closer to the input coupler, the drop spectrum would experience less attenuation. This is shown in Figure 3.3.a, in which there is up to 0.25 dB extra power to collect at the drop port than if it is located at the half-loss accumulation point for $a = 0.95$; of course, the benefit of this technique will be greater for lossier cavities and have diminishing returns for those with low round-trip losses. For photonic integrated circuits that prioritize energy efficiency and have exhausted all other modes of optimization, this opens up an additional avenue for shrinking power consumption a bit more. The drawback in making this choice is that the loss to the drop port is proportionally increased for the counterpropagating direction, which could hinder performance when light is intentionally coupled into both the clockwise and counterclockwise directions of the cavity. There may also be footprint-related issues in relocating the drop port coupler in another position in highly dense photonic integrated circuits. Figure 3.3.b shows how to drop port output phase relationship is also perturbed by drop port placement. In general, it appears coupler placement is an additional degree of freedom by which a designer can tailor the spectral response of the ring for the target application and should be aware of.

In the event where there is not a drop port coupler present (commonly referred to

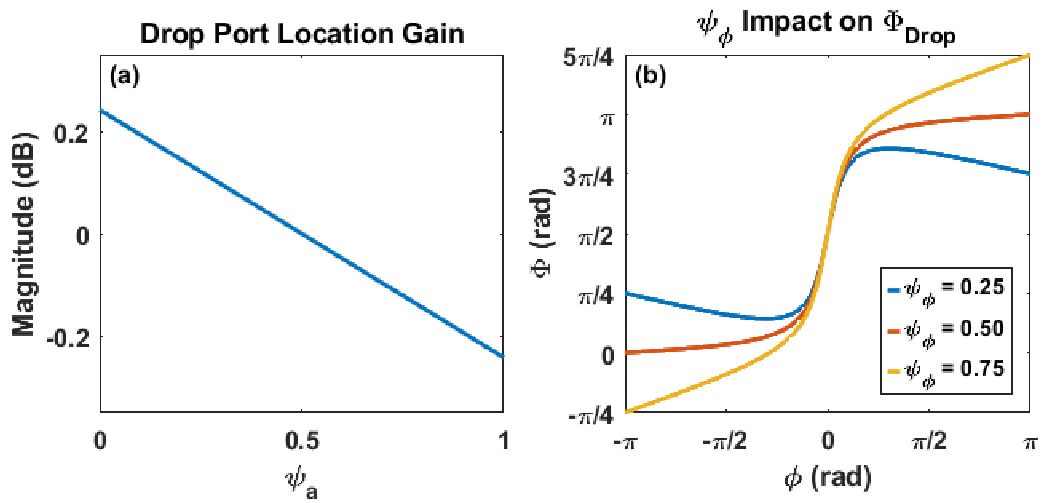

Figure 3.3: Impact on the power (a) and phase (b) response of the drop port placement on an add-drop ring resonator for which $\kappa_1 = 0.45$, $\kappa_2 = 0.31$, and $a = 0.95$.

as an all-pass resonator), $\sigma_2 = 1$ and $\kappa_2 = 0$; the through port repsonse for an all-pass resonator is shown in Equation 3.5.

$$\frac{E_{Through,All-Pass}}{E_{In}} = \frac{\sigma_1 - ae^{j\phi}}{1 - \sigma_1^* ae^{j\phi}} \tag{3.5}$$

When comparing Equation 3.5 to Equation 3.1.a, it can be seen that the drop port coupler effectively acts an extra loss term on the through port response; having a drop port is indistinguishable from having more waveguide loss when looking at only the through response. $a_{eff} = \sigma_2^* a$. Equation 3.6 therefore represents the power response of the through port for both all-pass and add-drop rings.

$$\frac{P_{Through}}{P_{In}} \propto \frac{I_{Through}}{I_{In}} = \left|\frac{E_{Through}}{E_{In}}\right|^2 = \frac{|a_{eff}|^2 - 2|\sigma_1||a_{eff}|\cos(\phi) + |\sigma_1|^2}{1 - 2|\sigma_1||a_{eff}|\cos(\phi) + (|\sigma_1||a_{eff}|)^2} \tag{3.6}$$

One key aspect of describing the Lorentzian shape of the resonance is its full width at half of its maximum in the power domain, $FWHM$. Some approximations are available in literature [6, 7], but an exact solution can be found by applying Equation 3.7.a to $\frac{P_{Drop}}{P_{In}}$ to solve for ϕ_{HM}.

$$\frac{P_{Out}(\phi = \phi_{HM}) - P_{Out}(\phi = \pi)}{P_{Out}(\phi = 0) - P_{Out}(\phi = \pi)} = \frac{1}{2} \tag{3.7.a}$$

$$\phi_{HM} = \cos^{-1}\left(\frac{2\,|\sigma_1|\,|\sigma_2|\,a}{(|\sigma_1|\,|\sigma_2|\,a)^2 + 1}\right) \approx \cos^{-1}\left(1 - \frac{(1 - |\sigma_1|\,|\sigma_2|\,a)^2}{2\,|\sigma_1|\,|\sigma_2|\,a}\right) \approx \frac{(1 - |\sigma_1|\,|\sigma_2|\,a)}{\sqrt{|\sigma_1|\,|\sigma_2|\,a}} \tag{3.7.b}$$

$$FWHM = \frac{\Delta\nu}{\pi}\phi_{HM} \tag{3.7.c}$$

Figure 3.4 plots the various expressions for ϕ_{HM} across the full range of losses a ring can experience. While all three expressions are valid under typical circumstances, exploring the extreme cases can provide interesting insight to the functioning of the device. It intuitively makes sense that ϕ_{HM} should be less than π for a function that reaches its minimum at $\pm\pi$ (by definition not half the maximum prominence of the lineshape) and that the two approximations are incorrect in regimes that defy this intuition. Using this exact expression, a fundamental upper limit can be placed on the full width at half maximum: $FWHM \leq \frac{\Delta\nu}{2}$.

While the output phase of the transfer function can be extracted from each point of the transfer function, generalized expressions for Φ of the through and drop ports can be produced by quantifying the contributions of each term of Equation 3.1.a and Equation 3.2 . To simplify the expressions, the coupling and transmission coefficients can be rewritten as phasors and the imaginary part of σ_i is assumed to be negligible ($\sigma_i = |\sigma_i|\,e^{j\phi_{\sigma_i}} \approx |\sigma_i|$ and $\kappa_i = |\kappa_i|\,e^{j\phi_{\kappa_i}}$).

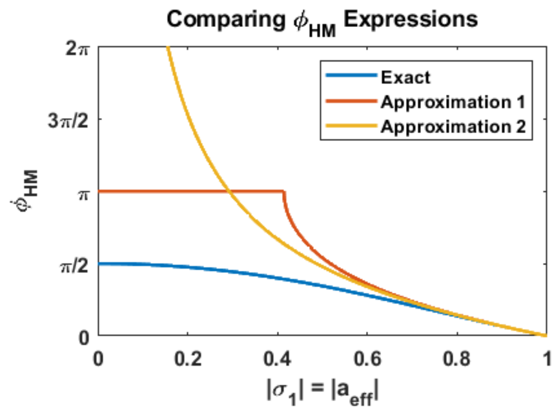

Figure 3.4: Comparing the different expressions of the ϕ_{HM} of a ring resonator as a function of $|\sigma_1|$ and $|a_{eff}| = |\sigma_1|$.

$$\Phi_{Through} \approx -\tan^{-1}\left(\frac{|\sigma_2|\, a \sin(\phi)}{|\sigma_1| - |\sigma_2|\, a \cos(\phi)}\right) + \tan^{-1}\left(\frac{|\sigma_1|\,|\sigma_2|\, a \sin(\phi)}{1 - |\sigma_1|\,|\sigma_2|\, a \cos(\phi)}\right) \tag{3.8}$$

$$\Phi_{Drop} \approx \psi_\phi \phi - \phi_{\kappa_1} + \phi_{\kappa_2} + \tan^{-1}\left(\frac{|\sigma_1|\,|\sigma_2|\, a \sin(\phi)}{1 - |\sigma_1|\,|\sigma_2|\, a \cos(\phi)}\right) \tag{3.9}$$

When on resonance, no light will be output if the light that was not coupled into the ring at the input port perfectly destructively interferes with the light that has circulated around the cavity (o.e., $|\sigma_1| = |a_{eff}|$); this phenomenon is referred to as critical coupling. The other two cases ($|\sigma_1| < |a_{eff}|$ and $|\sigma_1| > |a_{eff}|$) are respectively referred to as overcoupling and undercoupling; the more dissimilar $|\sigma_1|$ and $|a_{eff}|$ are, the more the extinction ratio of the resonance is degraded. The output phase relationship also changes. In the circumstance of an add-drop ring, critical coupling can also roughly occur also when the coupling coefficients of the input and drop port are the same and $a \approx 1$. When attempting to maximize the amount of power received at the drop port, it is key to maximize the coupling strength of both couplers and to also maximize a while preserving critical coupling. These statements are validated in Figure 3.5, along with showing that

$\Phi_{Through}$ has a much more limited range when undercoupled.

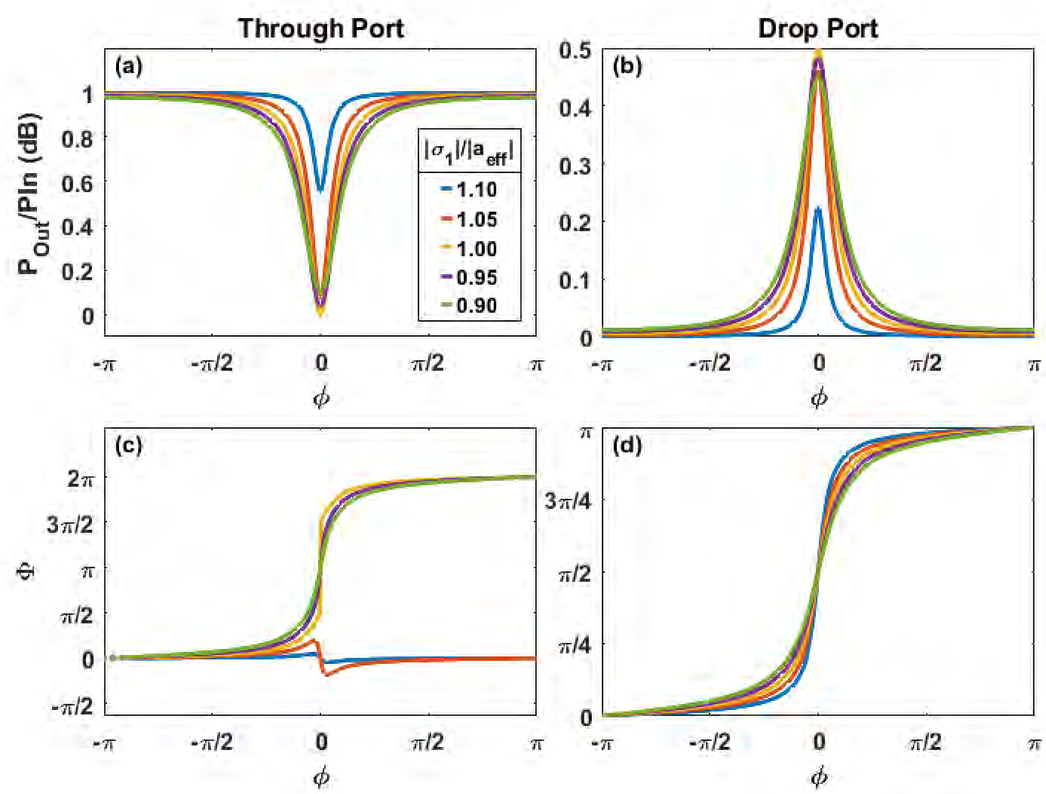

Figure 3.5: Impact on the power (a & b) and phase (c & d) response of the through (a & c) and drop (b & d) ports when the cavity is undercoupled, critically coupled, and overcouped on an add-drop ring resonator for which $\kappa_2 = 0.31$, $a = 0.95$, and $\psi_a = \psi_\phi = 0.5$.

There are some good insights to be made about coherent modulation formats with rings given these equations and plots. Φ changes most quickly around $\phi = 0$, so the carrier should be aligned to the resonance. There is a specific phase difference that leads to a π phase shift with equal amplitudes, which is what is sought for BPSK, if the ring is critically or overcoupled on the through port. Only BPSK is really possible with one ring due to only having 2 equal-amplitude points for any available phase separation. For the drop port, a π phase difference of the output levels is always possible regardless of coupling conditions as long as $\psi_\phi > \frac{1}{2}$; more strongly undercoupled rings with larger ψ_ϕ

have an advantage at reducing the difference between ϕ levels to get a π phase shift output at the cost of reduced peak output power on resonance; if the reduction in outweighs the amount of drop loss introduced (like in Figure 3.3), an overall increase in amplitude at the π-separated points may occur. A similar situation is present for the through port: by overcoupling the resonator, a BPSK signal with lower insertion loss can be generated if a larger phase shift between levels can be achieved. Therefore, the competition between insertion loss and available phase shifting range should be considered one of the fundamental tradeoffs for ring-based BPSK.

This large change in Φ near resonance can be reframed as a wavelength-dependent effective length enhancement of the resonator, which has applications in using rings for dispersion compensation and designing lasers with external cavity mirrors containing rings [8, 9].

$$\begin{aligned} Ł_{eff,Through} &= \frac{\partial \Phi_{Through}}{\partial \beta} = L\frac{\partial \Phi_{Through}}{\partial \phi} \\ &\approx -L\left(\frac{(|\sigma_2|\,a)^2 - |\sigma_1|\,|\sigma_2|\,a\cos(\phi)}{(|\sigma_2|\,a)^2 - 2\,|\sigma_1|\,|\sigma_2|\,a\cos(\phi) + |\sigma_1|^2} + \frac{1 - |\sigma_1|\,|\sigma_2|\,a\cos(\phi)}{(|\sigma_1|\,|\sigma_2|\,a)^2 - 2\,|\sigma_1|\,|\sigma_2|\,a\cos(\phi) + 1} - 1\right) \end{aligned} \tag{3.10}$$

$$Ł_{eff,Drop} \approx L\left(\frac{1 - |\sigma_1|\,|\sigma_2|\,a\cos(\phi)}{(|\sigma_1|\,|\sigma_2|\,a)^2 - 2\,|\sigma_1|\,|\sigma_2|\,a\cos(\phi) + 1} + \psi_\phi - 1\right) \tag{3.11}$$

Some popular formulations of effective length in the literature differ in their expression by including a $\frac{-1}{2}$ scaling factor [10]. Both formulations are application-specific, in that scaling factor is for computing the effective length of a reflective element to account for the π phase shift of the reflection and for propagating through the element between the input and the reflection twice. When dealing with a transmissive propagation, the scaling factor should not be included [11].

Figure 3.6 shows how L_{eff} is affected by the coupling conditions. As anticipated, effective length is of greatest magnitude on resonance. As critical coupling is approached from both the undercoupling and overcoupling regimes, the lineshape narrows and the magnitude increases. Undercoupled through port effective lengths are negative near the resonance. Additionally, the more strongly undercoupled the cavity is, the greater the drop port effective length. It should be noted that the drop port effective length is offset by $L\psi_\phi$ and will converge to $L\left(\psi_\phi - \frac{1}{2}\right)$ off-resonance.

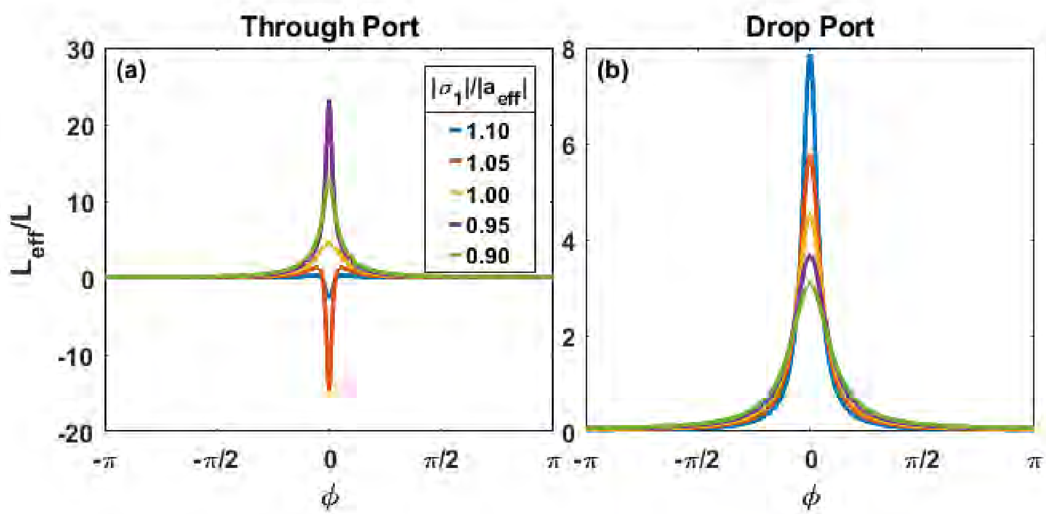

Figure 3.6: Normalized effect length of the through (a) and drop (b) ports when the cavity is undercoupled, critically coupled, and overcouped on an add-drop ring resonator for which $\kappa_2 = 0.31$, $a = 0.95$, and $\psi_\phi = 0.5$.

The resonant behavior of rings also enhances field amplitude in the cavity along with imparting a strong phase shift. In this way, ring resonators and other optical cavities can be thought of as energy storage devices.

$$\mathcal{B} = \left|\frac{E_{Circ}}{E_{In}}\right|^2 \approx \frac{|\kappa_1|^2 |\sigma_2|^2 a^2}{1 - 2|\sigma_1||\sigma_2| a \cos(\phi) + (|\sigma_1||\sigma_2| a)^2} \tag{3.12}$$

Figure 3.7 shows how $\mathcal{B}$ is influenced by the coupling conditions. Much like the drop port power response, the buildup factor is maximized on resonance and when critically coupled.

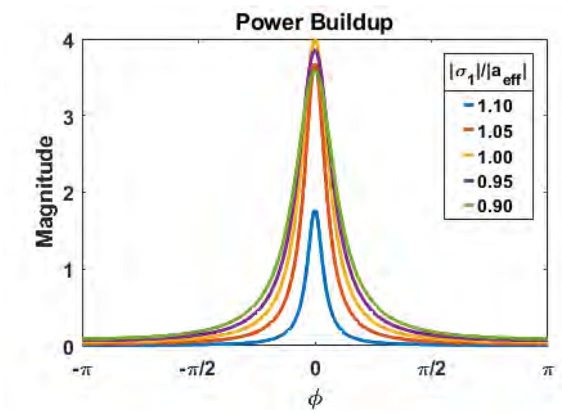

Figure 3.7: Input phase-dependent power buildup factor when the cavity is undercoupled, critically coupled, and overcouped on an add-drop ring resonator for which $\kappa_2 = 0.31$ and $a = 0.95$.

There is discrepancy in the literature about the definition of Equation 3.1.c and therefore $\mathcal{B}$ [3, 12]. Field amplitude is not necessarily uniform inside the cavity when losses and coupling is large enough, and therefore $\mathcal{B}$ should be considered more of a sampling at a particular point in the cavity; this work has chosen to define $\mathcal{B}$ for the point at the end of the propagation about the cavity whereas others choose the start. The ability to quantify buildup factor accurately at any point in the cavity is muddied further by the fact that coupling is distributed and would factor into buildup nonuniformity as well [6]. By including the accumulation of losses around the cavity and holding onto the point coupler approximation, the energy stored inside the cavity can be computed with the following expression.

$$U \approx \frac{P_{In}\tau\,|\kappa_1|^2}{1 - 2\,|\sigma_1|\,|\sigma_2|\,a\cos(\phi) + (|\sigma_1|\,|\sigma_2|\,a)^2}\left[\psi_L \frac{a^{2\psi_a} - 1}{2\ln(a)} + |\sigma_2|^2\,(1-\psi_L)\,\frac{a^2 - a^{2\psi_a}}{2\ln(a)}\right] \approx \mathcal{B}P_{In}\tau \tag{3.13.a}$$

$$\tau = \frac{L}{v_g} = \frac{1}{\Delta\nu} \tag{3.13.b}$$

$$\psi_L = \frac{L_{Drop}}{L} \tag{3.13.c}$$

In the above equations, τ is the round-trip transit time for a pulse travelling around the cavity. Calculating U with the highest degree of accuracy would also require integrating across the frequency span of the input power spectrum (e.g., finite carrier linewidth, data bands, multiple input carrier tones, amplified spontaneous emission).

3.2.1.2 Rate Equation Model

A second way to derive the expressions related to ring resonators is to instead frame the parameters in terms of the rate at which energy exits and enters the cavity [13, 14, 15, 16]. $|A|^2$ represents the amount of energy stored in the cavity, and the units of A are $\sqrt{\mathrm{J}}$ [13]. This rate equation for A in the simplest add-drop ring resonator case is provided in Equation 3.14.a.

$$\frac{\partial A}{\partial t} = \left(j\omega_0 - \frac{1}{\tau_p} \right) A - j\mu_1 E_{In} \tag{3.14.a}$$

$$E_{Through} = E_{In} - j\mu_1 A \tag{3.14.b}$$

$$E_{Drop} = -j\mu_2 A \tag{3.14.c}$$

$$E_{Circ} = \frac{A}{\sqrt{\tau}} \tag{3.14.d}$$

$$\tau_{e_i} = \frac{2L}{v_g \left|\kappa_j\right|^2} = \frac{2\tau}{1 - \left|\sigma_i\right|^2} \tag{3.14.e}$$

$$\tau_l = \frac{2\tau}{1 - a^2} \approx \left.\frac{2}{v_g \alpha}\right|_{a \approx 1} \tag{3.14.f}$$

$$\mu_i = \sqrt{\frac{2}{\tau_{e_i}}} \tag{3.14.g}$$

$$\frac{1}{\tau_p} = \frac{1}{\tau_l} + \frac{1}{\tau_{e_1}} + \frac{1}{\tau_{e_2}} \tag{3.14.h}$$

The τ_p term in the above expressions is referred to as the photon lifetime, and it represents how long energy is stored in the cavity before decaying by e^{-1} of its original value; its constituent terms are decay rates related to propagation losses and coupler transmission coefficient attenuation of the amplitude. μ_i is referred to as the mutual coupling rate and is used to describe coupling between the cavity and the through and drop ports.

The rate equation has the same form for all-pass and add-drop cases, just different photon lifetime contributions. Unlike in the travelling wave case, being able to approximate an add-drop cavity using the all-pass photon lifetime with an a_{eff} substitution only introduces no additional error in particular circumstances (e.g., if either $|\sigma_2| = 1$ — which is not an add-drop ring by definition — or $a = 1$ — a perfectly lossless cavity).

$$\frac{1}{\tau_{l,eff}} = \frac{1}{\tau_l} + \frac{1}{\tau_{e_2}} \iff 1 - a^2 - \left|\sigma_2\right|^2 + a^2 \left|\sigma_2\right|^2 = 0 \tag{3.15}$$

By representing A as a phasor, a solution can be found for the differential equation in 3.14.a.

$$A = |A|\,\mathrm{e}^{j\omega t} \tag{3.16.a}$$

$$A = \frac{-j\mu_1 E_{In}}{j\Delta\omega + \frac{1}{\tau_p}} \tag{3.16.b}$$

$$\Delta\omega = \omega - \omega_0 \tag{3.16.c}$$

$$\frac{E_{Through}}{E_{In}} = \frac{j\Delta\omega + \frac{1}{\tau_p} - \frac{2}{\tau_{e_1}}}{j\Delta\omega + \frac{1}{\tau_p}} \tag{3.16.d}$$

$$\frac{E_{Drop}}{E_{In}} = \frac{-\mu_1\mu_2}{j\Delta\omega + \frac{1}{\tau_p}} \tag{3.16.e}$$

Figure 3.8 show the through power response for a critically coupled add-drop ring derived from the rate equation and travelling wave models. The most obvious difference between the two spectra is that the output of the rate equation model is not periodic like the travelling wave model is (and how real devices are). On resonance, the two models do appear to agree well with each other.

Since the rate equation model spectrum is nonperiodic, the minimum value of $A(\omega) = 0$. The $FWHM$ can then be derived from Equation 3.16.b.

$$FWHM = \frac{1}{\pi\tau_p} = \frac{|\kappa_1|^2 + |\kappa_2|^2 + 1 - a^2}{2\pi\tau} = \frac{\Delta\nu}{\pi}\frac{3 - \left(|\sigma_1|^2 + |\sigma_2|^2 + a^2\right)}{2} \tag{3.17.a}$$

$$\tau_p = \frac{\tau}{\phi_{HM}} \tag{3.17.b}$$

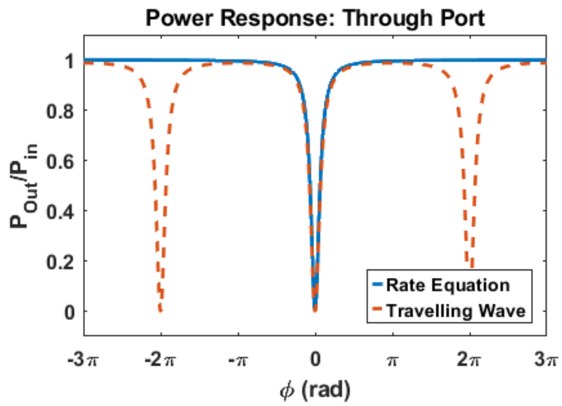

Figure 3.8: Comparison of the power response an add-drop ring resonator for which $\kappa_1 = 0.45$, $\kappa_2 = 0.31$, $a = 0.95$, and $\Delta\nu = 1.2$ THz utilizing both the rate equation and travelling wave models as a function of $\phi = \frac{\Delta\omega}{\Delta\nu}$.

When examining Figure 3.9.a, it is clear the above expression for $FWHM$ clearly does not match the one from the previous sub-subsection for all coupling coefficients and losses; however, there is agreement when $|\sigma_1| \approx |\sigma_2| \approx a \approx 1$ (i.e., when $\phi_{HM} \approx 0$). As shown in Figure 3.9.b, less than one percent error can be expected for $\phi_{HM} \leq 0.186$. This degradation of accuracy with higher losses is due to another limitation of this model: it assumes that the energy is evenly stored in the cavity such that $U = |A|^2 = P_{Circ}\tau$ [13, 17]; as established in the previous sub-subsection, the accuracy of this assumption is reduced as losses increase and photon lifetime decreases. One outcome of the low loss assumption failing is Equation 3.17.a underestimates the $FWHM$ when losses are high. Another strange implication of the rate equation is that the upper bound of $FWHM$ effectively depends on the number of constituent loss terms in the photon lifetime.

Since there is a limit on accuracy of the results the rate equation model can provide, establishing figures of merit that aid in determining the trustworthiness of the rate equation model's results would be of value, especially if they can be quantified in terms of parameters easily extracted from a wavelength scan. Two such contenders are finesse ($\mathcal{F}$) and Q, defined below.

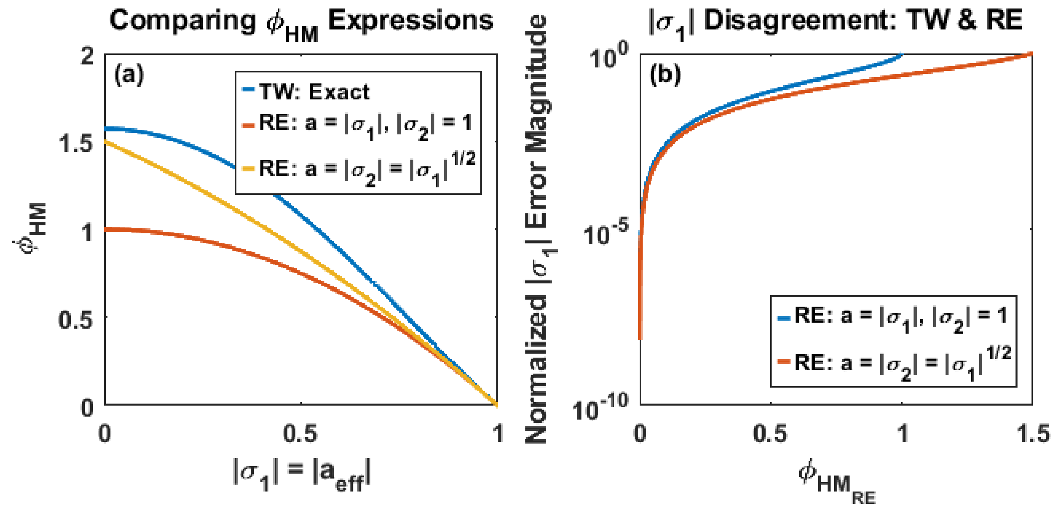

Figure 3.9: Comparing the travelling wave model (TW) expression of ϕ_{HM} to the two critically-coupled limit cases of the rate equation model (RE) for an add-drop ring resonator (a). Quantifying the error between $|\sigma_1|$ values for a given ϕ_{HW} between the travelling wave and rate equation models for the two cases explored in the rate equation model (b).

$$\mathcal{F} = \frac{\Delta\nu}{FWHM} = \frac{\pi\tau_p}{\tau} = \frac{\pi}{\phi_{HM}} \tag{3.18.a}$$

$$Q = \frac{\omega_0}{2\pi FHWM} = \frac{\omega_0\tau_p}{2} \tag{3.18.b}$$

Revisiting definitions of τ and τ_P, finesse appears to be proportional to the number of revolutions energy takes around the cavity before decaying by e^{-1}. To that effect, finesse is a figure of merit of how well energy is stored in the cavity. Q is proportional to how many oscillations occur in the resonant frequency during the time it takes for energy in the cavity to decay by e^{-1}. Q is slightly simpler to collect from a measurement and is usually the reported value about a ring, but finesse serves as the more direct measured figure of merit regarding how well the rate equation model will accurately represent the system. It appears that in the travelling wave model, which does not include the photon lifetime, ϕ_{HM} serves as surrogate parameter for energy storage; the travelling wave model asserts a fundamental lower bound of finesse in ring resonators: $\mathcal{F} \geq 2$.

One way to reconcile the uniform energy distribution assumption, the nonperiodicity of the output function, and the disagreement in ϕ_{HM} with the travelling wave model is that the rate equation model is describing a travelling wave expression for which $L = 0$. In other words, the cavity is envisioned as a singular point in space in the rate equation model. This would require energy storage to be uniform, the presense of only one resonance in the frequency domain, and effectively force $\phi_{HM} = 0$.

3.2.1.3 Picking Between the Two Models

While the previous sub-subsection may appear to have been highly critical of the rate equation model, it most certainly has value. When describing more complicated scenarios than a single ring operated in a linear, cold cavity regime that does not exhibit any backscatter, the simplicity inherent to introducing these advanced phenomena into the rate equation model makes it an attractive choice [13, 14, 18, 19]; however, this does not mean implementations for a travelling-wave based model do not exist for similar scenarios [20, 21, 12]. Many of these approaches are focused in a high Q resonator regime and therefore are minimally impacted by the assumptions built into the rate equation model.

Another benefit inherent to the rate equation model comes from its usefulness in parameter extraction [14]. As mentioned previously, $|\sigma_1|$ and $|a_{eff}|$ are effectively indistinguishable in the rate equation model; this makes determining contributions from cavity losses and coupling from a measured power spectrum of a ring resonator tricky. However, when fitting to that same power spectrum with the rate equation model, each term can be identified because the effect of coupling appears in both the photon lifetime and the mutual coupling rate.

In high-speed communication applications, the finesse of some rings may be low enough that using the rate equation model introduces some error to the design that is greater than the designer's tolerance, especially at progressively higher baud rates. Under these circumstances, best practice would call for establishing as many models that are needed from a travelling wave foundation; when making a travelling wave model would be too complex or cumbersome to implement, a rate equation approach could be leveraged, especially if there is a travelling-wave-based test to verify using a rate equation-based approach is not distorting the conclusions of the model.

3.2.2 Integrated Phase Shifters

At their essence, phase shifters operate by applying a perturbation field to a waveguide. The primary focus of this perturbation field for a phase shifter is to perturb the refractive indeces of the materials that form the waveguide by Δn, but losses can also be affected ($\Delta\alpha$). Change in waveguide effective index and loss can be determined by computing the overlap between the optical mode and the index and loss perturbation fields [5, 10].

$$n_{eff} = n_{eff_0} + \frac{\int\int E^*(x,y)\Delta n(x,y)E(x,y)\,dx\,dy}{\int\int E^*(x,y)E(x,y)\,dx\,dy} \tag{3.19.a}$$

$$\alpha = \alpha_0 + \frac{\int\int E^*(x,y)\Delta\alpha(x,y)E(x,y)\,dx\,dy}{\int\int E^*(x,y)E(x,y)\,dx\,dy} \tag{3.19.b}$$

In the above equations, n_{eff_0} and α_0 are the unperturbed effective index and loss of the waveguide mode under investigation, and $E(x,y)$ is the electric field profile of the mode.

The perturbation to index and loss could be from any sort of available physical mechanism, such as a changing temperature field. The perturbative phenomenon of particular interest for high-speed communications in silicon photonics is the free carrier plasma dispersion effect (FCPDE), in which the displacement of free carriers changes the refractive index and loss of the material [22].

$$\Delta n = \frac{-q^2\lambda^2}{8\pi^2 c^2 \epsilon_0 n}\left(\frac{\Delta N_e}{m^*_{c,e}} + \frac{\Delta N_h}{m^*_{c,h}}\right) \tag{3.20.a}$$

$$\Delta\alpha = \frac{q^3\lambda^2}{4\pi^2 c^3 \epsilon_0 n}\left(\frac{\Delta N_e}{m^{*2}_{c,e}\mu_e} + \frac{\Delta N_h}{m^{*2}_{c,h}\mu_h}\right) \tag{3.20.b}$$

In the above equations, q is the elementary charge, ϵ_0 is the vacuum permittivity, ΔN is the concentration of displaced free carriers, m^*_c is the carrier conductivity effective mass, μ is the carrier mobility, and subscripts e and h denote carrier type (electron or hole, respectively) . As can be seen in the above equations, the displacement of free carriers induces a local perturbation in the refractive index and loss. For example, as charge is accumulated, effective index decreases, resulting in a blue shift when this occurs inside a ring resonator; this is accompanied by an increase in losses, which can make the ring more undercoupled. As can also be deduced from these expressions, displaced holes and electrons impart different magnitudes of index and charge change; under most circumstances, a displaced concentration of holes with perturb index more and loss less than the same concentration of displaced electrons [5]. Further, the magnitude of the index and loss perturbations increases as wavelength increases. Displacing more charge increases the magnitude of the loss and index changes, though there is a regime for dopant concentrations around 1E+18 cm^{-3} in which a significant fraction of carriers will not be ionized due to the dopant band still being separated from the conduction/valence band and not enough thermal energy to ionize all the dopants (reducing the amount of available free carriers) [23].

Another avenue for enhancing the magnitude of effective shift is to change the carrier transport properties of the waveguide materials. One method that would do so is increasing temperature, which will perturb many of the terms in the free carrier plasma dispersion effect equations, including material refractive index, carrier mobility, conductivity effective mass, and the fraction of ionized charge [24, 25, 26, 27, 28, 23]. Figure 3.10 shows the index changes between room temperature and 80° C can be about 10 percent for holes, and losses for holes can increase by about 30 percent. Separately from a mechanism to leverage, this temperature-dependent performance should be kept in mind when designing devices that operate across a broad temperature range to ensure adequate performance throughout the entire temperature span.

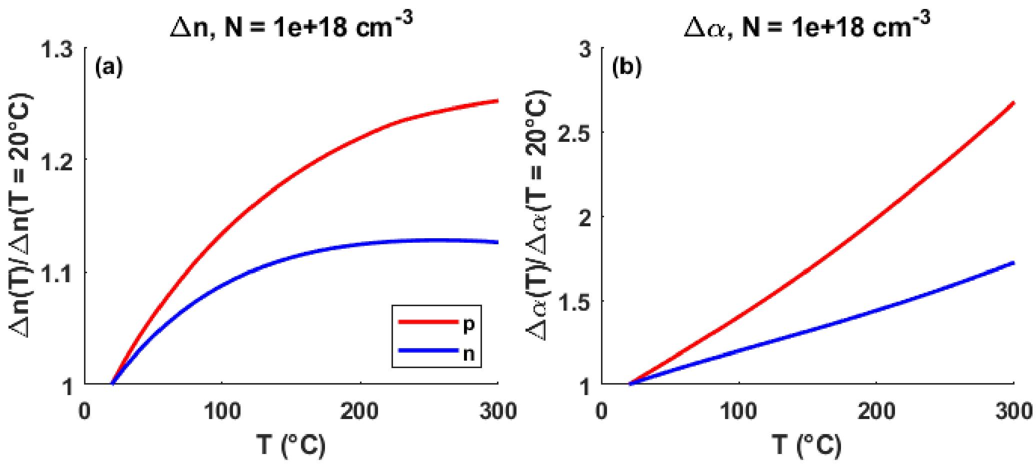

Figure 3.10: Modelled effect of temperature on the magnitude of electrorefraction (a) and electroabsorption (b) induced by electrons and holes via the free carrier plasma dispersion effect for a dopant concentration $N = 1\text{E}{+}18\text{cm}^{-3}$.

An additional means to affect carrier transport would be to change the material composition or introduce strain (which is induced when dissimilar materials are grown on one another); one commonly proposed method is to use $\text{Si}_{1-x}\text{Ge}_x$ alloys to enhance hole mobility and reduce effective mass [29, 28, 30]. To explore the potential value, a model was constructed to estimate how alloy fraction may enhance the free carrier plasma dispersion effect magnitude at room temperature compared to pure Si [29, 31, 32, 33, 34, 35, 36, 37, 38], and the results are plotted in Figure 3.11. It can be seen that the anticipated loss increase from displaced electrons is disproportionate to magnitude of index perturbation, and therefore introducing SiGe would only be worthwhile for enhancing hole displacement. The maximum alloy fraction allowed would depend on operating wavelength due to bandgap narrowing introducing absorption. While certainly not trivial to introduce into a foundry process, the boost to tuning efficiency strained SiGe phase shifters could bring combined with the relatively low cost to do so compared to other materials (such as III-V) may make it an appealing option to realize compact and energy efficient links of the future.

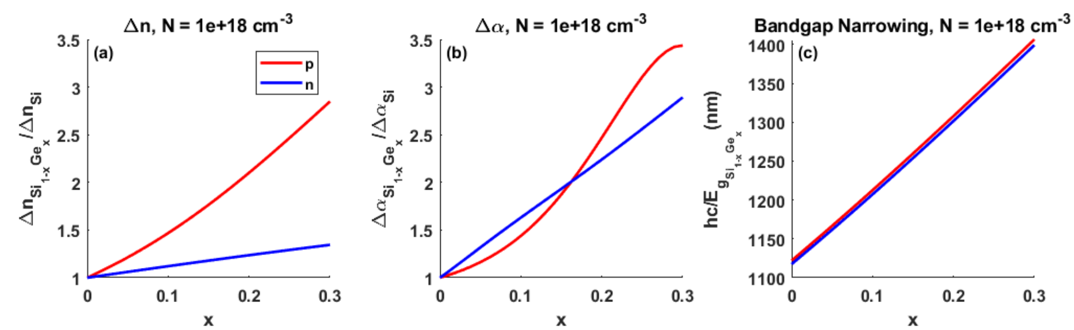

Figure 3.11: Modelled effect of strained SiGe alloys grown on Si on the magnitude of electrorefraction (a) and electroabsorption (b) and bandgap narrowing (c) induced by electrons and holes via the free carrier plasma dispersion effect for a dopant concentration N = 1E+18cm^{-3} at room temperature.

Commonly-available device structures for leveraging the free carrier plasma dispersion effect are the p-n junction, metal-insulator-semiconductor capacitor (MOSCAP), and semiconductor-insulator-semiconductor capacitor (SISCAP) [39]; illustrations of both devices are shown in Figure 3.12. It is also possible to induce electrostatic doping with a large substrate or gate bias [40, 41], but this will not be a primary feature of the discussion.

Phase shifter based on p-n junctions can displace charge either in forward bias by injecting carriers or depleting carriers in reverse bias; carrier depletion is typically a weaker phenomenon than injection, but injection is much slower due to being limited by the minority carrier lifetime [42]. Depletion-based ring modulators have been demonstrated at data rates in excess of 100 GBaud [43]; since the p-n junction is formed via ion implantation, complex cross-sectional geometries can be formed to maximize the charge displacement overlap with the optical mode [44, 45]. Periodically interdigitated p-n junctions can also be formed to introduce displacement in the longitudinal dimension, but the junction profile formed is sensitive to effects like lithographic resolution limits and the lateral spreading of the implanted dopants [46, 47].

MOSCAP/SISCAP phase shifters are usually operated in accumulation mode and are typically able to displace more charge than a depletion-mode phase shifter, but they are typically more complicated to manufacture due to needing to form a thin gate dieletric between the two electrodes. There are multiple waveguide geometries (with either vertical or horizontal capacitor interfaces) and material systems to pair with silicon photonics to achieve these device structure, such as deposited polycrystalline silicon or bonded III-V material [30, 48, 49, 50]. Polycrystalline silicon has the advantage of being more easily integrated into a foundry process than bonded III-V material, but its higher losses and worse carrier transport properties could induce a performance penalty compared to using III-V as the second terminal of the capacitor. However, the enhanced carrier recombination rates of polycrystalline silicon may improve its power handling capabilities, as self-heating is enhanced by two-photon absorption induced free carrier absorption [18, 12]. Finally, the amount of total charge these acccumulation mode devices can displace is limited by dielectric breakdown voltage of the capacitor. Using a gate dielectric with a high relative permittivity ϵ_r such as HfO_2 would increase the breakdown voltage limit and allow for greater accumulation of charge at the cost of increased capacitance [39].

Most ring modulator phase shifters are small enough to be approximated as a lumped

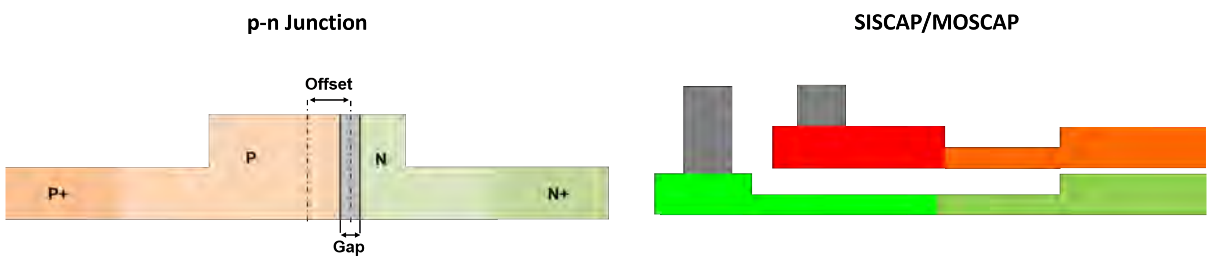

Figure 3.12: Cartoon illustrations of a p-n junction (left) and a SISCAP/MOSCAP phase shifter (right).

electrical element. The depletion-mode p-n junction phase shifter and the MOSCAP/SISCAP devices have a similar equivalent circuit: a load capacitance C with a parasitic series resistance R_S. Capacitance can be defined as follows:

$$C = \left| \frac{\partial Q}{\partial V} \right| \approx \frac{\epsilon_0 \epsilon_r A}{d} \tag{3.21}$$

In the above expression, Q is total charge, A is the surface area of a parallel plate capacitor approximation, and d is the gap between parallel plates. Since the amount of charge displaced is voltage-dependent for both depletion p-n junctions and MOSCAP/SISCAP devices, the capacitance is also voltage dependent; to first order, this can be modelled as a parallel plate capacitor with a voltage-dependent gap between the electrodes [39]. However, built into the parallel plate capacitor approximation requries that the gap between the electrodes is significantly smaller than the width and length of the parallel plates; this does not always hold true in these phase shifter elements, and fringing fields can contribute a noticeable additional fraction to the capacitance [51].

The series resistance of a circular arc of phase θ can be described with the following equations:

$$R_{S,Circular} = \frac{R_\square}{\theta} \ln\left(\frac{r_{Out}}{r_{In}}\right) \tag{3.22.a}$$

$$R_{\square} = \frac{1}{\int_0^h \frac{1}{\rho(x)} dx} \tag{3.22.b}$$

$$\frac{1}{\rho} = q(N_e \mu_e + N_h \mu_h) \tag{3.22.c}$$

In the above equations, $R_{\square}$ is the sheet resistance, r_{Out} and r_{In} are the out and inner radius of the circular arc, h is the thickness of the implanted region, and ρ is the resistivity of the implanted region. Ion implantation means the charge distribution is not uniform because ion implantation profiles typically have a spatial Gaussian distribution associated with them [52]. Overall, the best results for modelling charge displacement and electrical parasitics will come from finite element modelling [5]. Like the FCPDE magnitude, series resistance is also temperature dependent due to changes in carrier mobility [25, 26].

The more fundamental expression of capacitance above also reveals a tradeoff of FCPDE-based phase shifters: developing a stronger phase shift for the same magnitude of applied voltage requires increasing $\frac{\partial Q}{\partial V} = C$. Therefore, more efficient FCPDE phase shifters typically have higher capacitance.

Since what is of primary concern is maximizing the change in effective index, manipulating the waveguide geometry can also be leveraged to maximize phase shift efficiency. This is done by ensuring that the charge displacement is occurring at the peak intensity of the optical mode and designing a waveguide cross section that tightly confines the mode and enhances peak intensity. In rib waveguides, one method that can be used to increase confinement is to increase the depth of the shallow etch that forms the rib [51]. Depending on the curvature of the waveguide, the peak intensity of the mode may not be at the same position it would be at in a straight waveguide [53]. Some manipulations intended to enhance effective index change could also increase electrical parasitics. For example increasing the shallow etch depth to form a rib waveguide increases core confinement, but also increases series resistance [51].

A more complete electrical model would include electrical parasitics from the pads, vias, interconnects, and substrate to increase the accuracy [54]. Modelling the SISCAP structure accurately would also require knowledge of the electrical and optical characteristics of polycrystalline silicon. Finally, a more complete description of the magntiude of refractive index change these phase shifters induce would include secondary phenomena such as the DC Kerr effect [55, 56].

3.2.3 Large Signal Domain

Describing the large signal response is not of import solely for modulators, but also rings who optical input is time-domain varying such as the WDM demux filter. Passive time-invariant filters in a cold cavity regime can use simple rational models [57] or take the Fourier transform of the input signal to the filter function; something gained from using a dynamic large signal model such as the one in this subsection instead would be to include effects that typically might be ignored, such as the impact on signal integrity that the a stabilizing circuit has on a ring-based demux filter undergoing temperature variations [58].

Since it has been shown in the previous subsection that the rate equation model may not be the most accurate choice for cavities with high losses (such as high speed ring modulators and WDM demux filters), the travelling wave model will be the basis of the large signal domain modelling in this chapter rather than the rate equation model (though there are also implementations of simulating ring modulators with a rate-equation based large signal model [1, 59]). Several assumptions are in place in the current model: that there is no field present at the add port, that there is no backscatter or backcoupling, that there is no loss associated with the couplers such that $\sigma_j^2(t) = 1 - \kappa_j^2(t)$, that the coupling occurs at an instantaneous point in space, and that the two bus waveguides coupled to the ring are placed apart such that the time difference between the two ports normalized to round trip transit time τ, ψ_τ, is rational. The significance of the final assumption is that it allows for discretizing the ring into even segments in the time domain; in the simplest case, $\psi_\tau = \frac{1}{2}$, and that is what will primarily be used in this chapter; temporal discretization is a feature introduced into this model that was absent from prior work to be able to introduce a drop port. As shown in Figure 3.13, the round-trip phase and propagation loss is discretized for the two distinct sections between the bus waveguides (expressed as $\phi_k(t)$ and $\alpha_k(t)$ for phase and loss, respectively, and k is an integer denoting the corresponding subsection of the ring); it is suspected that further discretization could aid in more advanced modelling scenarios, such as a cavity with more than two couplers, couplers placed at irregular intervals, pulley couplers, backscatter, backcoupling, segmented phase shifters, coupled cavities, nonuniformity of refractive index and loss distributions, nonlinearities, and capturing any potential phenomena with time constants much smaller than τ.

Let us consider the impact of what happens when the drop port is placed such that it is not $\frac{\tau}{2}$ away in time from the input port (which, once again, is not necessarily $\frac{L}{2}$ away in physical distance) with a ring that has been discretized into two regions. Much like how the add-drop model would be affected in terms of accumulated loss and phase distribution, this model can be affected by a simultaneously nonuniform and asymmetric group index distribution across the cavity in that one segment would take longer than $\frac{\tau}{2}$ to traverse one segment and shorter than $\frac{\tau}{2}$ for the other if the discretization were placed halfway around the physical length rather than the group length. Further, if higher levels of discretization are employed, these segments should be evenly distributed in time rather than space. Finally, it is assumed that the changes in group index negligibly perturb τ such that it can be assumed constant rather than also a time-varying parameter; if this did not hold, the K spatial discretizations employed would need to move dynamically such that their temporal separation remained $\frac{\tau(t)}{K}$.

The large signal model for the through port, much like the steady state travelling wave model, can be constructed by tracking the accumulated loss, phase, coupling, and transmissions that occur during a revolution around the ring and relating the circulating field amplitude to the input and transmitted values [60, 2]. This leads to the dynamic response of the present being dependent on the dynamic response in the past. The solution can be found by using the Fredholm integral of the second kind [42].

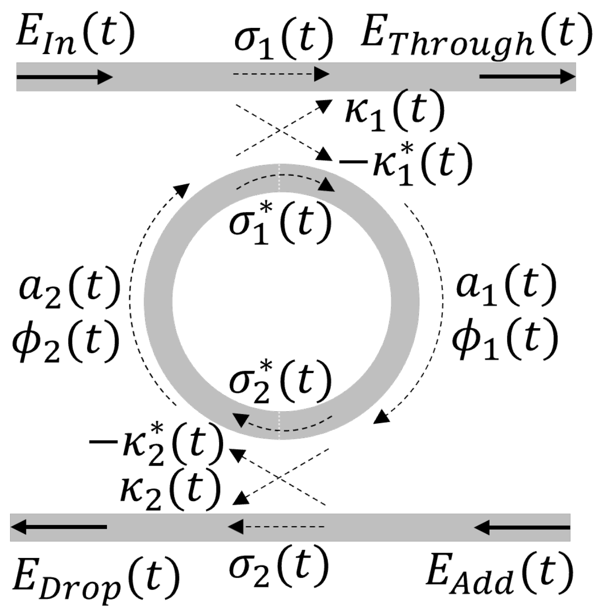

Figure 3.13: Schematic of the dual-bus microring modulator for dynamic modelling in which $\psi_\tau = \psi_L = \frac{1}{2}$.

$$T_{Through}(t) = \frac{E_{Through}(t)}{E_{In}(t)}$$
$$= \sigma_1(t) - \frac{\kappa_1(t)}{\kappa_1(t-\tau)}\sigma_2^*(t-(1-\psi_\tau)\tau)a(t)\mathrm{e}^{j\phi(t)}\frac{E_{In}(t-\tau)}{E_{In}(t)}\left[\sigma_1^*(t-\tau)T_{Through}(t-\tau)-1\right] \tag{3.23.a}$$

$$T_{Through}(t) \approx \Xi(t) + \sum_{n=1}^{N} \left[\frac{\kappa_1(t)\Xi(t-n\tau)}{\kappa_1^*(t-n\tau)} \times \prod_{m=0}^{n-1} \sigma_1^*(t-(m+1)\tau)\Upsilon(t-m\tau) \right] \quad (3.23.b)$$

$$\Xi(t) = \sigma_1(t) - \frac{\kappa_1(t)}{\kappa_1(t-\tau)}\Upsilon(t) \quad (3.23.c)$$

$$\Upsilon(t) = \sigma_2^*(t-(1-\psi_\tau)\tau)a(t)\mathrm{e}^{j\phi(t)}\frac{E_{In}(t-\tau)}{E_{In}(t)} \quad (3.23.d)$$

$$\psi_\tau = \frac{1}{c\tau}\int_0^{L_{Drop}} n_g(L)\,dL \quad (3.23.e)$$

$$a(t) = \prod_{k=1}^{K} a_k(t - \frac{(K-k)\tau}{K}) \quad (3.23.f)$$

$$\phi(t) = \sum_{k=1}^{K} \phi_k(t - \frac{(K-k)\tau}{K}), \quad (3.23.g)$$

In the steady state circumstance, Equation 3.23.a reduces to Equation 3.1.a as expected. This large signal function accounts for temporal fluctuations in the coupling and round-trip propagation terms as well as the input field, and this inclusion allows for modelling of laser carrier relative intensity noise and phase noise, as well as inter-channel crosstalk in the case of a WDM transmitter with several modulators in series. The dynamic transfer function of the drop port can be related to the through port response by:

$$T_{Drop}(t) = \frac{\kappa_2(t)}{\kappa_1^*(t-\psi_\tau\tau)} a_{Drop}(t) \mathrm{e}^{j\phi_{Drop}(t)} \left(\sigma_1(t-\psi_\tau\tau) T_{Through}(t-\psi_\tau\tau) - \frac{E_{In}(t-\psi_\tau\tau)}{E_{In}(t)} \right). \tag{3.24.a}$$

$$a_{Drop}(t) = \prod_{k=1}^{\frac{K}{\psi_\tau}-1=K'} a_k(t - \frac{(K'-k)\tau}{K}) \tag{3.24.b}$$

$$\phi_{Drop}(t) = \sum_{k=1}^{K'} \phi_k(t - \frac{(K'-k)\tau}{K}) \tag{3.24.c}$$

Figure 3.14 shows the through and drop power response with a short input NRZ data sequence, and Figure 3.15 shows the time dependent output phase for that same simulation. It shows that the large signal model captures phenomena that a steady state model could not, such as the gradual rise and fall from one amplitude level to another and the peaks and dips in amplitude and phase at level transitions. This peaking or ringing is introduced by the change in Φ and $\mathcal{B}$ changing the interference condition with the input coupler and how much energy can be stored in the cavity. The degree of peaking experienced is influenced by many factors, including the loaded Q of the cavity, whether the ring is undercoupled, overcoupled, or critically coupled, the amount of frequency detuning between the carrier and the resonance, and the speed of the transition [1, 17].

The fact that this ringing effect is onset by sudden changes in power and output phase implies the onset of another impacting factor: frequency chirp. Chirp can be a limiting factor in optical links limited by chromatic dispersion, and ring modulators typically exhibit higher levels of chirp than MZI-based devices (though the magnitude and sign of chirp can be controlled via coupling conditions) [61]; chirp can be quantified in terms of

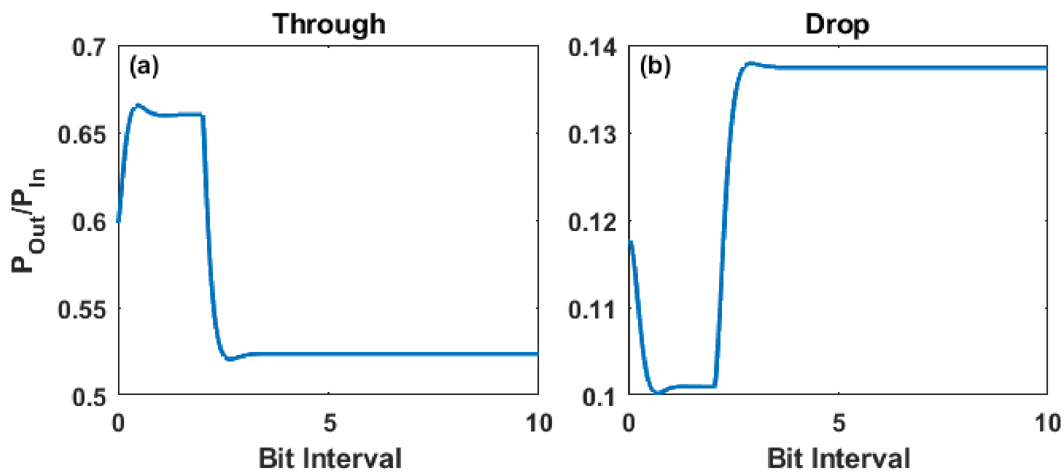

Figure 3.14: Example dynamic power response of the through (a) and drop (b) ports due to loss and phase modulation from an integrated phase shifter.

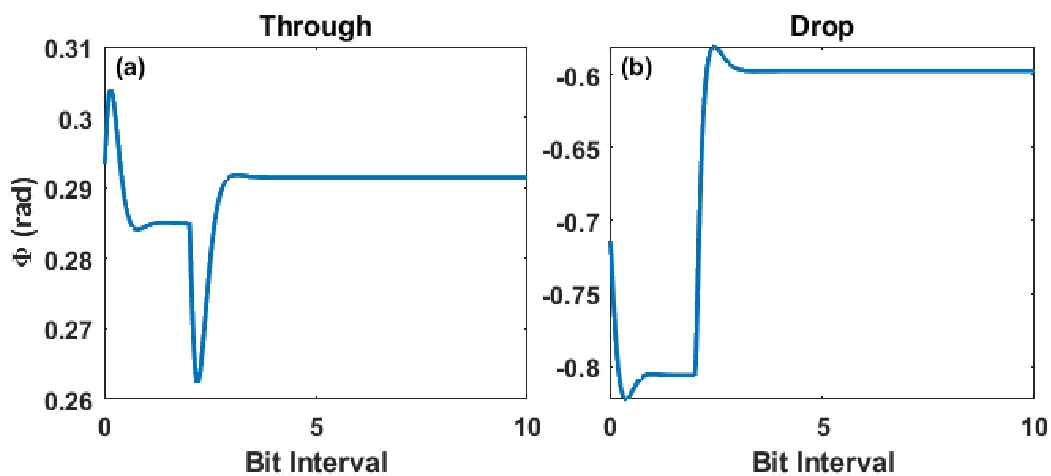

Figure 3.15: Example dynamic phase response of the through (a) and drop (b) ports due to loss and phase modulation from an integrated phase shifter.

the instantaneous frequency change Δf or the chirp parameter a_{Chirp} [62, 10].

$$\Delta f_{Through}(t) = \frac{1}{2\pi}\frac{\partial \Phi_{Through}(t)}{\partial t} = \frac{\alpha_{Chirp}(t)}{4\pi P_{Through}(t)}\frac{\partial P_{Through}(t)}{\partial t} \tag{3.25}$$

Figure 3.16 depicts the instantaneous frequency chirp and chirp parameter for the through and drop port for the dynamic responses shown in Figure 3.14. It appears that the drop response exhibits much higher chirp than the through response and with an opposite polarity.

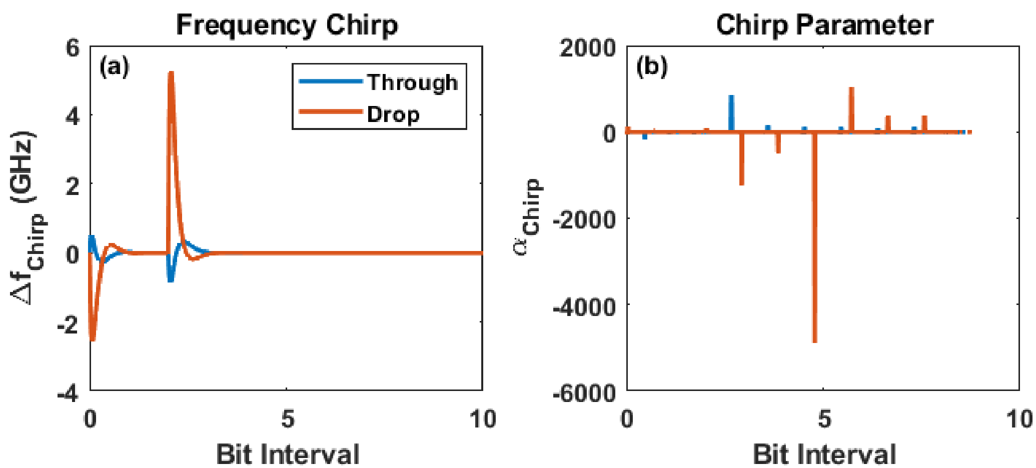

Figure 3.16: Simulated frequency chirp (a) and chirp parameter (b) observed at the add and ports due to loss and phase modulation from an integrated phase shifter.

Revisiting Equation 3.23.b, an approximation symbol is used to underscore the fact that this method truncates an infinite series into a finite summation. N should then be a significantly large integer to approximate an infinite arithmetic series with minimal relative error. However, it would be rather beneficial to know how much error a particular choice of N can introduce into the result, since using a smaller value of N will reduce runtime of the simulation. A simple way to think about this is the truncation of the integral from an infinite series down to N amounts to erasing knowledge of energy from the cavity once its field amplitude has decayed by $\mathrm{e}^{-\frac{N\tau}{\tau_p}}$ in the rate equation model. Therefore, the maximum relative error in the magnitude and phase of $T(t)$ associated with a particular selection of N can be expected to be:

$$\delta|T|_{max} \approx \delta\Phi_{max} \approx \mathrm{e}^{-\frac{N\tau}{\tau_p}} \approx \mathrm{e}^{-\frac{N\pi}{\mathcal{F}}}. \tag{3.26}$$

The validity of the approximation is tested in Figure 3.17, which compares the maximum relative error predicted in Equation 3.26 to the relative error in amplitude and phase of the through and drop response in a datastream modelled with varying degrees of N normalized to the output when $N = 1000$; there is clearly good agreement between the simulation and the equation. An interesting outcome is that a cavity with a higher $\mathcal{F}$ requires a larger N to achieve the same degree of accuracy in the simulation result, and perhaps reformulating Equation 3.26 in terms of $\mathcal{F}$ can allow for using travelling wave definition of $FWHM$ and improve the maximum error expectation in cavities with low finesse. Additionally, time varying propagation losses or coupling coefficients imply a time varying finesse, and the maximum expected error should then use the highest finesse to get a more accurate upper bound. Finally, beginning a simulation requires providing initial conditions of the time dependent variables in the system for $N\tau \leq t < 0$; for example, once can assume the cavity was in a steady state before $t = 0$.

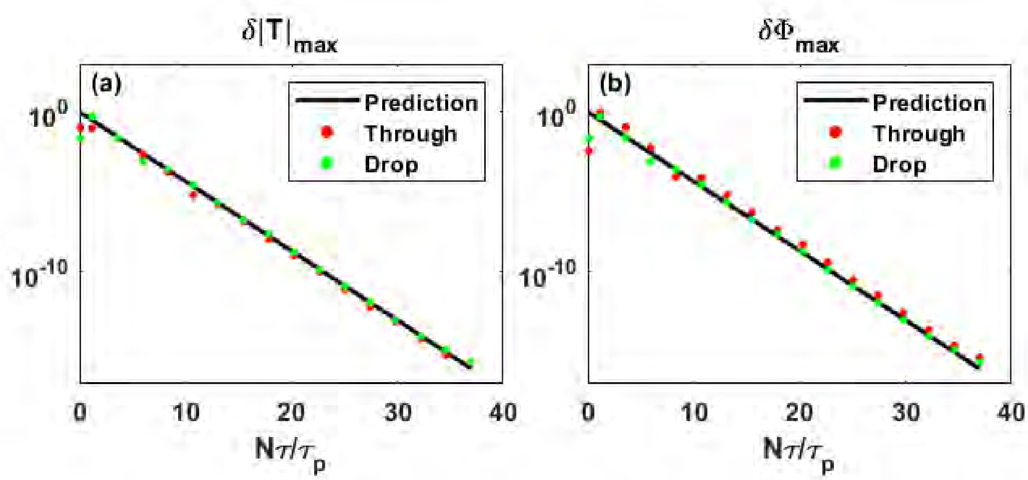

Figure 3.17: Comparison of maximum relative error in magnitude (a) and phase (b) of the large signal model through and drop response of the first 2^8 bits of a 27.5 Gbps PRBS($2^{11} - 1$) NRZ sequence and the expected degree of error from a rate equation approximation.

The technique of using the through port dynamic response as the basis of analyzing another region of the cavity can also be used to describe the transfer function at the start of each time discretization of the cavity, the energy stored in each discretization, and the total energy stored in the cavity (allowing for future expansions of the model to include nonlinear phenomena).

$$T_{Circ_k}(t) = \begin{cases} \frac{1}{\kappa_1(t)}\left[\sigma_1^*(t)T_{Through}(t) - 1\right], & \text{if } k-1=0 \\ a_{k-1}(t)\mathrm{e}^{j\phi_{k-1}(t)}T_{Circ_{k-1}}(t-\frac{\tau}{K}), & \text{if } 0 < \frac{k-1}{K} < \psi_\tau \\ \sigma_2^*(t)a_{k-1}(t)\mathrm{e}^{j\phi_{k-1}(t)}T_{Circ_{k-1}}(t-\frac{\tau}{K}), & \text{if } \psi_{\tau \leq \frac{k-1}{K} < 1} \end{cases} \tag{3.27.a}$$

$$U(t) = \sum_{k=1}^{K} U_k(t - \frac{(K-k)\tau}{K}), \tag{3.27.b}$$

$$U_k(t) = \left|T_{Circ_k}(t)\right|^2 P_{In}(t)\frac{\tau}{K}\frac{a_k(t)-1}{\ln\left(a_k(t)\right)}, \tag{3.27.c}$$

An example of the computed stored energy of a ring during modulation with 1 mW input power is shown in Figure 3.18. Previous studies have shown that self-heating and other nonlinear phenomena can occur with peak stored energies in the cavity of about 30 fJ or less [18].

For a typical ring modulator, both the phase and losses in the cavity vary with time due to the input voltage waveform to the integrated phase shifter, and the coupling coefficients are assumed to be static. The driving waveform can be distorted by the parasitics of the phase shifter and therefore distort the optical waveform. Since the capacitance of the phase shifter (and, to a lesser extent, its series resistance) is voltage-dependent, its impedance is time-varying as well [63].

$$\frac{\partial V_j(t)}{\partial t} = \frac{V_{In}(t) - V_j(t)}{R_S(t)C(t)} \tag{3.28}$$

Figure 3.19 shows an example of how the parasitic electrical characteristics can affect

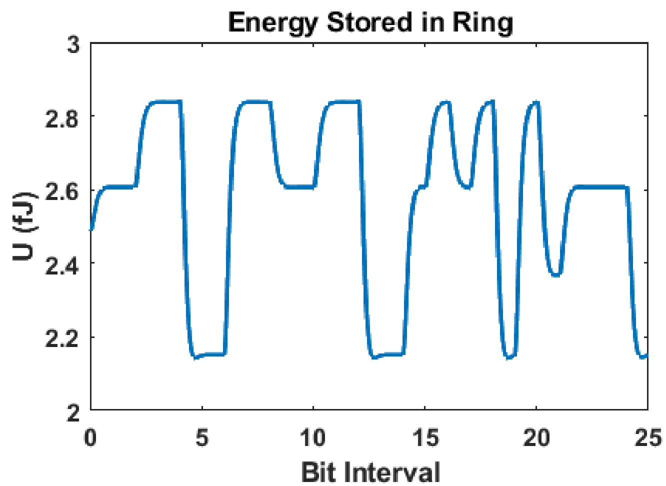

Figure 3.18: Simulated stored energy during PAM-4 modulation and an input power of 1 mW.

the driving voltage waveform. It effectively increases the rise and fall transition time between amplitude levels, which negatively impacts the fidelity of the transmitted signal.

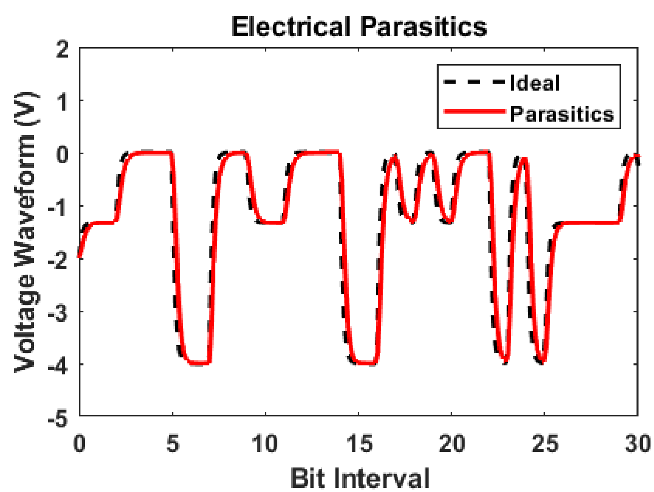

Figure 3.19: Simulated of voltage waveform illustrating distortion from its electrical parasitics.

3.2.4 Small Signal Domain

While a large signal model is a highly useful tool for accurately evaluating how datastreams are encoded and filtered by a ring resonator, it does not really provide sufficient intuition on what makes a good ring modulator on its own; it also is the most computationally expensive analysis tool available. Therefore, it would be beneficial to have access to comparatively cheap computation tools that enhance our intuition about optimizing device performance, and small signal analysis is a critical part of this toolbox. Small signal models, as the name suggests, apply a small-magnitude sinusoidal perturbation of modulation angular frequency ω_m to the system; it is assumed that the perturbation amplitude is small enough that the system remains in a linear regime, and therefore no additional tones are generated. While small signal analysis equations can be derived from large signal travelling wave models, prior work has done so for only one degree of modulation at a time (i.e., index modulation, loss modulation, or coupling modulation) without a high degree of agreement betwen the large signal and small signal results [60]. Instead, the rate equation model will be used as the basis for deriving the transfer function and its validity will be tested by sending a small signal through our large signal travelling wave model and comparing the performance between the two. In context of a modulator with an integrated phase shifter, a small signal driving voltage induces a small signal perturbation in the cavity's round trip phase and losses, which ultimately perturbs the resonance frequency, the photon lifetime, and A.

$$V_{In}(t) = V_{DC} + \delta v \sin(\omega_m t) \tag{3.29.a}$$

$$\omega_0(t) = \omega_0 + \delta\omega_0 \sin(\omega_m t) \tag{3.29.b}$$

$$\tau_p(t) = \tau_p + \delta\tau_p \sin(\omega_m t) \tag{3.29.c}$$

$$A(t) = A + \delta A \sin(\omega_m t) \tag{3.29.d}$$

Previous works have developed small signal modulation expressions for all-pass ring modulators [17, 15]. By following the derivation in those works for the add-drop resonator rate equation model and following similar rules (second order small signal terms neglected, $\frac{\delta \tau_p}{\tau_P} \approx 0$), the small signal response of add-drop device can be expressed:

$$H_{EO,Through}(\omega_m) = \eta \left[j\omega_m \left(\zeta\xi_2 - \Delta\omega\right) - 2\Delta\omega\xi_1 - \zeta\left(\Delta\omega^2 - \frac{\xi_2}{\tau_p}\right)\right] \tag{3.30.a}$$

$$H_{EO,Drop}(\omega_m) = \eta\mu_2^2 \left(\Delta\omega - \zeta\left(\frac{1}{\tau_p} + j\omega_m\right)\right) \tag{3.30.b}$$

$$\eta = \frac{2\mu_1^2 P_{In}\left(-\frac{\omega_0}{n_g}\left.\frac{\partial n_{eff}}{\partial v}\right|_{V_{DC}}\right)}{\left(\frac{1}{\tau_p^2} + \Delta\omega^2\right)\left(-\omega_m^2 + \frac{2}{\tau_p} j\omega_m + \Delta\omega^2 + \frac{1}{\tau_p^2}\right)} \tag{3.30.c}$$

$$\zeta = \frac{\left.\frac{\partial(1/\tau_p)}{\partial v}\right|_{V_{DC}}}{-\frac{\omega_0}{n_g}\left.\frac{\partial n_{eff}}{\partial v}\right|_{V_{DC}}} \tag{3.30.d}$$

$$\xi_1 = \frac{1}{\tau_p} - \frac{1}{\tau_{e_1}} \tag{3.30.e}$$

$$\xi_2 = \frac{1}{\tau_p} - \frac{2}{\tau_{e_1}} \tag{3.30.f}$$

The terms responsible for introducing the effects of the perturbation of the cavity dynamics are ζ and the term in parentheses in the numerator of η. They are written in such a way that both small signal index and loss perturbations can be accounted for, but are incomplete in describing small signal coupling modulation due to not incorporating perturbations to the mutual coupling rates $\delta\mu_i$. Those wishing to capture simultaneous coupling, index, and loss modulation would need to run through the derivation in [17] with those added terms.

$$\begin{aligned} H_{EO+\delta\kappa,Through}(\omega_m) = \mu_1 \Re \Bigg[\Bigg(& \frac{E^*_{Through}\left(\delta\omega_0 A - \delta\mu_1 E_{In} - j\frac{\delta\mu_1}{\mu_1} A \left(\frac{1}{\tau_p} + j(\Delta\omega + \omega_m)\right)\right)}{\frac{1}{\tau_p} + j(\Delta\omega + \omega_m)} \\ & + \frac{E_{Through}\left(\delta{\omega_0}^* A^* - \delta\mu_1 E^*_{In} + j\frac{\delta\mu_1}{\mu_1} A^* \left(\frac{1}{\tau_p} - j(\Delta\omega - \omega_m)\right)\right)}{\frac{1}{\tau_p} - j(\Delta\omega - \omega_m)} \Bigg) \mathrm{e}^{j\omega_m t} \Bigg] \end{aligned} \tag{3.31.a}$$

$$\begin{aligned} H_{EO+\delta\kappa,Drop}(\omega_m) = \mu_2 \Re \Bigg[\Bigg(& \frac{E^*_{Drop}\left(\delta\omega_0 A - \delta\mu_1 E_{In} - j\frac{\delta\mu_2}{\mu_2} A \left(\frac{1}{\tau_p} + j(\Delta\omega + \omega_m)\right)\right)}{\frac{1}{\tau_p} + j(\Delta\omega + \omega_m)} \\ & + \frac{E_{Drop}\left(\delta{\omega_0}^* A^* - \delta\mu_1 E^*_{In} + j\frac{\delta\mu_2}{\mu_2} A^* \left(\frac{1}{\tau_p} - j(\Delta\omega - \omega_m)\right)\right)}{\frac{1}{\tau_p} - j(\Delta\omega - \omega_m)} \Bigg) \mathrm{e}^{j\omega_m t} \Bigg] \end{aligned} \tag{3.31.b}$$

$$\delta\mu_i = \left.\frac{\partial\mu_i}{\partial v}\right|_{V_{DC}} \tag{3.31.c}$$

However, the ring modulators of interest in this thesis do not need to account for coupling modulation effects, so simplifying the above expressions in the vein of [15] is left as an exercise for the reader. These transfer functions are electro-optic small signal responses (i.e., the output is relative to the optical field amplitude) [15]. Since the spectral response of the received electrical signal is typically of concern in communication links, this requires converting the response from optical amplitude to electrical amplitude (proportional to optical power); the fact that these small signal transfer functions are not in terms optical power is confusing due to the many indications in the derivation that they would be, but comparing the results of these expressions to the output of the travelling wave large signal model with a small signal input seems to verify this. Additionally, these transfer functions are not normalized to DC (i.e., $\omega_m = 0$). With these considerations in mind, 3 dB bandwidths in the electrical domain can be defined by identifying the ω_m for which the normalized small signal transfer functions equal $\frac{1}{\sqrt{2}}$.

$$f_{3dBe,PSK} = \frac{1}{2\pi\tau_p} \tag{3.32.a}$$

$$f_{3dBe,ASK,Through} \approx \frac{1}{4\pi\tau_p^2\xi_1}\sqrt{1 + 2\Delta\omega^2\tau_p^2 - 4\tau_p^2\xi_1^2 + \Delta\omega^4\tau_p^4 + 4\Delta\omega^2\tau_p^4\xi_1^2 + r_A} \tag{3.32.b}$$

$$r_A = \sqrt{1 + 4\Delta\omega^2\tau_p^2 - 8\tau_p^2\xi_1^2 + 6\Delta\omega^4\tau_p^4 - 8\Delta\omega^2\tau_p^4\xi_1^2 + 32\tau_p^4\xi_1^4 + 4\Delta\omega^6\tau_p^6 + r_B} \tag{3.32.c}$$

$$r_B = 8\Delta\omega^4\tau_p^6\xi_1^2 + \Delta\omega^8\tau_p^8 + 8\Delta\omega^6\tau_p^8\xi_1^2 + 32\Delta\omega^4\tau_p^8\xi_1^4 \tag{3.32.d}$$

$$f_{3dBe,ASK,Drop} \approx \frac{1}{2\pi\tau_p}\sqrt{\Delta\omega^2\tau_p^2 - 1 + \sqrt{2\Delta\omega^4\tau_p^4 + 2}} \tag{3.32.e}$$

For applications in which the laser is not detuned from the ring's resonance (such as phase shift keying), the ring's electro-optic bandwidth is best represented by $f_{3dB,PSK}$ for both the through and the drop response. Mainly a function of $\Delta\omega\tau_p$, which can be used as the parameter to . For small positive $\Delta\omega\tau_p$ products ($0 < \Delta\omega\tau_p \ll 1$), both expressions are bad at predicting the response bandwidth due to the proximity to the zero in each transfer function ($\mathit{\Delta}\omega\tau_p = \zeta$ for the drop and $\mathit{\Delta}\omega\tau_p \approx \frac{\sqrt{\xi_1^2\tau_p^2+\zeta^2\xi_2\tau_p}-\xi_1\tau_p}{\zeta}$ for the through) This error comes from the fact these ASK bandwidth expressions are extracted from the transfer functions with the simplifying assumption that $\zeta \approx 0$. Since there is a single zero, the bandwidth curves are asymmetric about the $\Delta\omega\tau_p = 0$ line. No assumptions are made regarding coupling ratio in the bandwidth estimates, whereas previous works assumed critical coupling for simplifying the transfer function even further [15].

An important insight gained from these modulation bandwidth expressions is that ring modulators with shorter photon lifetimes will be capable of larger modulation bandwidths. This makes sense, as cavities with lower photon lifetimes are able to change their state more quickly because they do not store energy for as long. However, as photon lifetime is reduced, the $FWHM$ increases, effectively reducing the amount of amplitude modulation experienced for the same magnitude of phase shift difference between levels. The tradeoff between modulation depth and modulation bandwidth is one of the fundamental design choices for resonant amplitude modulators and makes their design very application-specific [64]. For example, a ring modulator optimized to operate at 56 Gbps will never outperform one designed for 10 Gbps if both are operated at 10 Gbps.

Maximizing modulation depth is critical for optimum link performance and is what typically defines the optimum detuning of a design of an IM-DD application. In cases of small refractive index modulations, the optimum detuning point is therefore the region of the resonance with the largest $\frac{\partial P_{Out}}{\partial \phi}$ [17]. However, in large signal cases that have large enough modulations that this degree of detuning is not large enough to avoid crossing over the resonance (reducing modulation depth), the detuning should be increased accordingly; some additional detuning buffer may be preferred to avoid the zero point.

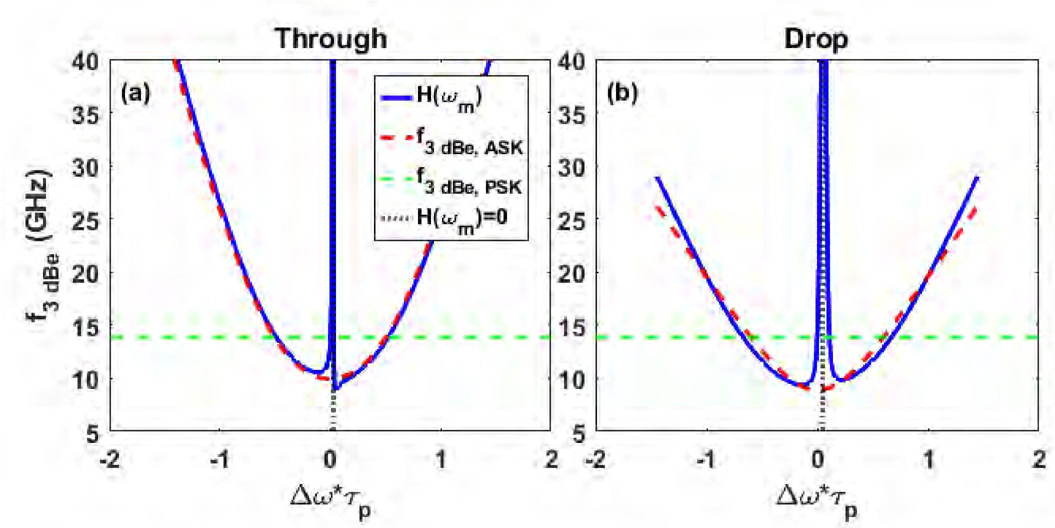

Figure 3.20: Estimated 3 dB bandwidth of the electro-optic frequency response of an add-drop ring modulator for which $\tau_p\xi_1 \approx 0.92$ using the small signal model (solid lines) and f_{3dBe} expressions (dashed lines) as a function of $\Delta\omega\tau_p$

$$\Delta\omega_{ASK} = \begin{cases} \frac{1}{\tau}\cos^{-1}\left(\frac{-1-(|\sigma_1||\sigma_2|a)^2+\sqrt{1+34(|\sigma_1||\sigma_2|a)^2+(|\sigma_1||\sigma_2|a)^4}}{(|\sigma_1||\sigma_2|a)}\right) \approx \frac{\sqrt{3}}{\tau_p}, & \text{if } \frac{\sqrt{3}}{\tau_p} > \frac{\phi_{Max}-\phi_{Min}}{2\tau} \\ \frac{\phi_{Max}-\phi_{Min}}{2\tau}, & \text{otherwise} \end{cases} \tag{3.33}$$

If the ring resonance is perfectly symmetric, detuning the carrier by $-\Delta\omega_{ASK}$ from would be an equally valid choice. However, since silicon ring amplitude modulators typically are not operating in a cold cavity regime in practice, it is preferential for the carrier to be blue shifted to minimize the extent of signal distortion from nonlinear phenomena [59].

Figure 3.21 shows the normalized frequency response of add-drop modulator design with equal coupling to the input and drop bus waveguides ($\mathcal{F} = 33.7$ and $Q = 6780$), simulated with both the dynamic large signal model and the small signal transfer function. It can be seen from this figure that these two models agree very well with each other, allowing for the most time-efficient model to be utilized in a design-space exploration with confidence that the choice of model does not impact the outcome of the simulation for this value of finesse and higher. Small degrees of detuning dampen high frequencies compared to on resonance, and there is a peaking effect introduced from sufficiently large detuning (typically for $\Delta\omega\tau_p > 1$) ; prominent peaks from large detuning have their maximum response near $\Delta\omega$. Frequency responses for the same magnitude and opposite polarity become more similar for larger detuning values; the highest disparity in frequency response by changing the polarity occurs around the zero in each transfer function (in which the positive detuning experiences a peak around $\frac{1}{2\pi\tau_p}$). It is also shown in these plots that the frequency responses of the through and drop ports exhibit similar trends but are not the same; the drop port experiences less peaking than the through port. Many of these conclusions are anticipated from Figure 3.20. Additionally, the modulation bandwidth estimation equations match as well in the given detuning ranges (as expected).

Out of the sake of curiosity, the in-cavity large signal model was also run to glean any insight on its small signal response; intuition suggests its normalized small signal response would match that of the drop port, and that is verified in Figure 3.21. Therefore, the f_{3dBe} expressions derived for the drop port also apply to the cavity, and its small signal response is a linear scaling factor of the drop response.

$$H_{EO,Circ}(\omega_m) = \frac{\eta}{\tau}\left(\Delta\omega - \zeta\left(\frac{1}{\tau_p} + j\omega_m\right)\right) = \frac{1}{\mu_2^2\tau}H_{EO,Drop}(\omega_m) \tag{3.34}$$

Finally, the overall transfer function of the device needs to include the small signal response of the electrical parasitics.

$$H_{Total} = H_{EO}H_{RC} \tag{3.35.a}$$

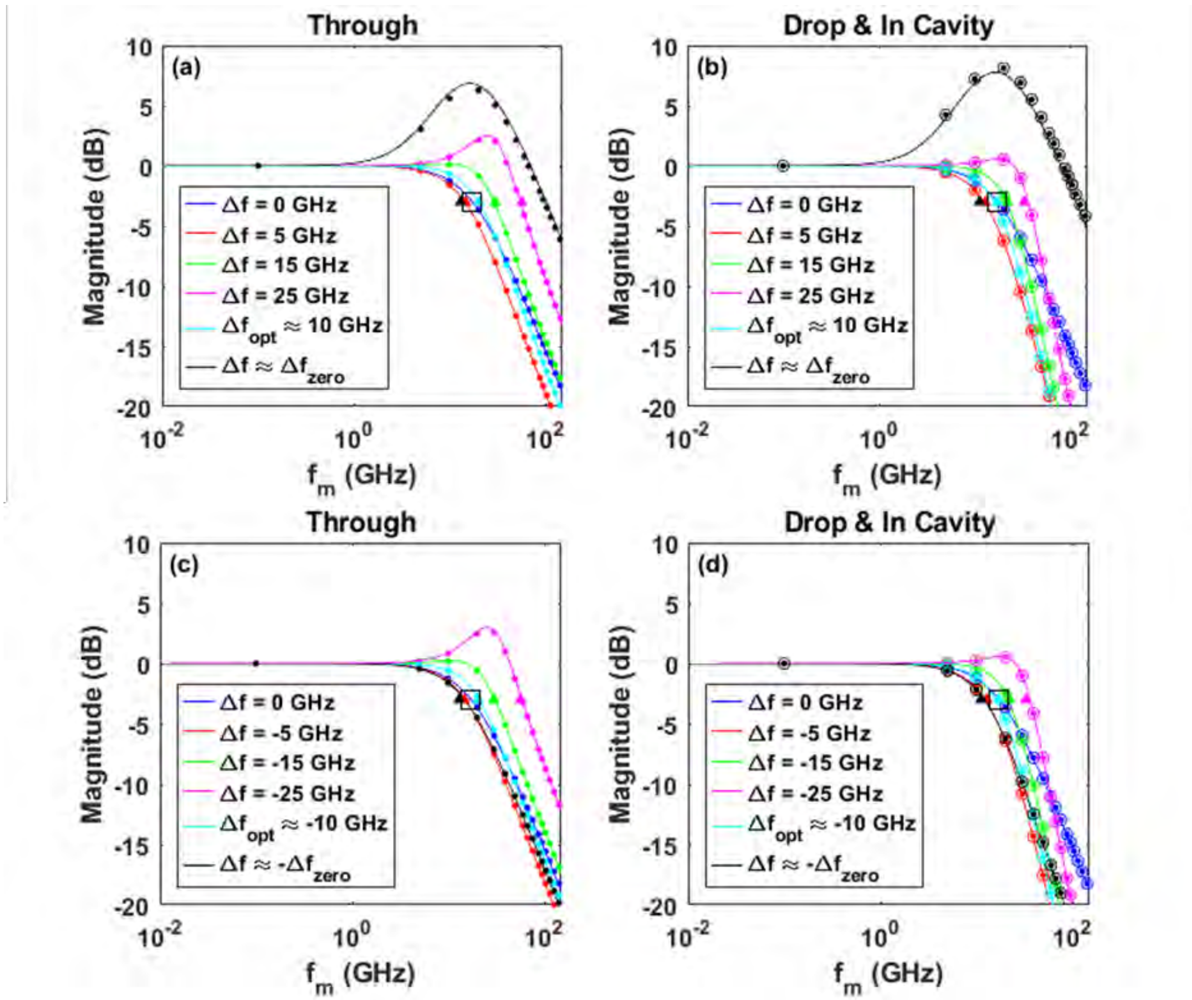

Figure 3.21: Simulated normalized electro-optic frequency responses of an add-drop ring modulator in the optical power domain using the small signal model (lines) and large signal model (solid dots) for various laser-ring frequency detunings, along with the f_{3dB} estimation (triangle and hollow squares), for both the through port (a & c) and the drop port (b & d) as well as for positive (a & b) and negative (c & d) detunings. The hollow circles depict the large signal model output for the in-cavity small signal response (b & d), and the hollow squares indicate the 0 GHz frequency detuning case for easier plot reading (a-d).

$$H_{RC}(\omega_m) = \frac{1}{1 + j\omega_m R_S C} \tag{3.35.b}$$

This returns the overall device 3 dB bandwidth [65].

$$f_{3dB} \approx \frac{f_{3dB_{RC}} f_{3dBe_{EO}}}{\sqrt{f_{3dB_{RC}}^2 + f_{3dBe_{EO}}^2}} \tag{3.36.a}$$

$$f_{3dB_{RC}} = \frac{1}{2\pi R_S C} \tag{3.36.b}$$

It can be seen from the above equation that a higher phase shifter capacitance and resistance will lower the bandwidth of the modulator and limit the maximum data rate of the device. Therefore, there exist tradeoffs between the electrical, optical, and electro-optical aspects of the device to get the best overall performance.

3.3 Device Design & Simulation

This section will put together what was learned in the previous section and apply it to the design of both ring modulators and demultiplexing filters; this section will focus on devices with integrated depletion-mode p-n junction phase shifters. Parameters relevant to the characteristics of an individual ring will be considered along with extra considerations when cascading many rings on the same bus (as what would occur in a practical WDM system). First, an individual ring modulator will be designed. Its performance as a bus will then be explored, and then a ring demux filter will be designed. It should be noted that the designs outlined in this section were not actually produced; this section merely serves as an exercise for ring-based design.

3.3.1 Ring Modulator Design

The first step into defining a ring resonator with an integrated FCPDE phase shifter is defining a waveguide geometry for the bus and ring waveguides. The waveguide geometry selected for the ring waveguide has several requirements. First, it must be able to achieve a small enough bend radius to achieve the target free spectral range; for this project, a free spectral range of 1.2 THz is needed, which corresponds to a circle with a bend radius between 9 and 10 μm for most silicon photonics platforms. This bend radius is not too demanding for a typical p-n junction phase shifter-based silicon photonics platform, so a rib waveguide geometry can be leveraged. Even tighter bend radii could prevent the use of a shallow etch on the outer diameter of the ring waveguide because it would allow the mode to leak out of the core too much and be lossy; mitigating this risk results in a more microdisk-like modulator that would require both the phase shifter anode and cathode have their via contact points be within the inner diameter of the ring, which would likely increase the electrical parasitics of the device [66, 67]. This transitions to the second aspect of ring waveguide geometry selection: minimizing electrical parasitics for the high speed phase shifter. The rib waveguide geometry is selected because of the aforementioned reasoning, although the best candidate in this regard may be a disk-like structure with a shallow etch on the outer diameter so the anode and cathode are still not introducing additional parasitics and the inner diameter electrode can have less series resistance between it and the junction [42]. The third consideration is core width. Increasing the core width (which in the extreme case becomes a microdisk) could also increase confinement to the core overall, but the mode may also spread out more and weaken the overall FCPDE for a fixed junction design; this could also add extra electrical parasitics to the junction design. Additionally, a widened core could become a multimode waveguide that requires extra care when designing the couplers, and any transitions in the cavity would need to be adiabatic to prevent higher order mode excitation. Widened cores typically also have lower coupling coefficients for the same core separation between the ring and bus waveguides, and this could also complicate coupler design.

The bus waveguide must also achieve many of the same goals as the ring waveguide geometry. Typically, the geometry chosen should be appropriately phase matched to the ring waveguide to excite coupling to the correct mode of the ring, must not constrain the implementation of the integrated phase shifter, and must be able to produce a coupler with strong enough coupling coefficients for the design while fitting into the unit cell's allocated footprint.

For both the ring and bus waveguide in this design section, a rib geometry will be selected. The device layer thickness is nominally 220 nm with a 60 nm slab thickness. The simulated energy density of the fundamental mode at a wavelength of 1300 nm is shown in Figure 3.22.b. This passive waveguide has a group index of about 4.0805 with a bend radius of 11 μm, suggesting a bend radius of about 9.74 μm to achieve a free spectral range of 1.2 THz.

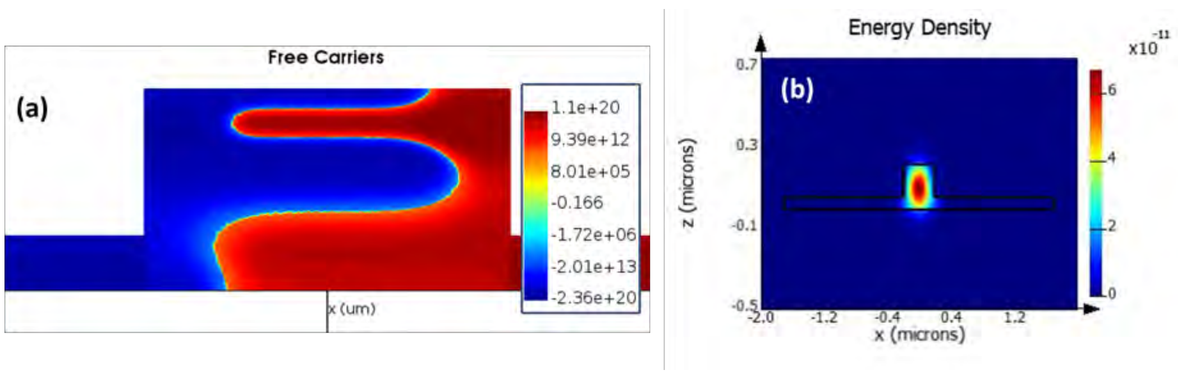

Figure 3.22: Contours of simulated of free carrier density (units cm^{-3}) in the phase shifter at a 0 V bias (a) and the energy density of the optical mode (b).

Next, an integrated phase shifter design must be chosen. When utilizing a foundry MPW offering, the ion implantation profiles are typically fixed, so this is more a matter of tailoring the FCPDE magnitude to the target application by adjusting the placement of these fixed layers and juggling it against the resultant electrical parasitics. For this particular process under exploration, the “F”-shaped junction showed in Figure 3.22.a seemed likely to maximize charge displacement with its extensive length of the depletion region that is located at the peak intensity of the optical mode. It is clear that this advanced junction shape requires finite element analysis to accurately model depleted charge as the bias voltage changes.

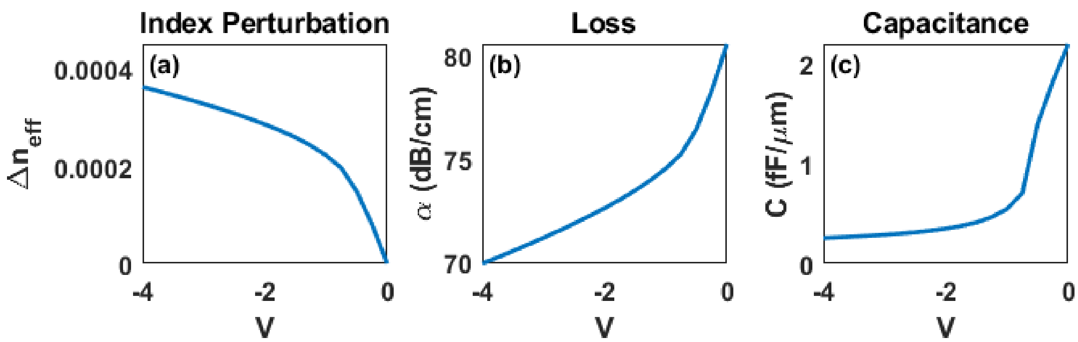

Figure 3.23: Simulation of voltage-dependent effect index (a), propagation loss (b), and capacitance (c) for a depletion-mode PN junction phase shifter on a silicon photonics platform.

Some of the electro-optic and electrical simulation results are shown in Figure 3.23; in this simulation, the anode is on the outer diameter of the ring. For comparison, this junction design is capable of about 3.3 times greater change in effective index over 4 V of applied bias with much less induced free carrier absorption when using the provided implant steps to make a more traditional phase shifter with a depletion region running straight up and down the core with charge depleted only laterally. However, this phase shifter design could still likely be outperformed by a SISCAP/MOSCAP phase shifter by a factor of 3.3 in terms of index perturbation over the same voltage range, but at the expense of more wildly varying free carrier absorption losses across that voltage span. Additionally, the change in effective index with applied voltage is not linear, which can result in uneven optical levels with even voltage levels in modulation formats with more than two symbol levels. That nonlinearity might motivate uneven spacing between driving voltage levels or split MSB and LSB phase shifters to produce a PAM-4 link with a more evenly spaced optical domain eye diagram [68, 69, 70].

The capacitance-voltage curve shown in Figure 3.23.c drops precipitously for reverse bias magnitudes greater than 1 V, suggesting that the thinner regions of free carriers that form the junction are fully depleted at about that point. The simulated series resistance is approximately 4.85 kΩ-μm at room temperature. This series resistance and capacitance lead to a parasitic electrical 3 dB bandwidth of 14.9 GHz, which may be a bit too low for a modulator targeting operation at about 27 Gbps; an overall device bandwidth closer to 20 GHz may be desired, which could be achieved with equal electrical and electro-optic bandwidths of about 30 GHz each. While the capacitance of the junction cannot be modified without affecting the index perturbation strength, there is quite a bit of room to drop the series resistance of the device. In this simulation, the Ohmic contact ion implantation layer is 1.4 μm away from the edge of the core on each side of the waveguide. The sheet resistance should lower by a factor of 7.0 on the anode side and a factor of 4.2 on the cathode side, and the original sheet resistance of the anode without the Ohmic implant is roughly twice that of the cathode without the Ohmic implant. Therefore, one way the series resistance can be roughly halved is if the Ohmic contact implant separation was reduced on each side from 1.4 μm to about 550 nm away from the edge of the core on each side. This would introduce additional free carrier absorption; looking ahead to Figure 5.5.b (although for a slab thickness of 110 nm in the C-Band instead of 60 nm in the O-Band, so an overestimate for this scenario) that tens to potentially 100 dB/cm additional free carrier absorption could be introduced by moving the implants equally. In practice, the bent waveguide will also increase free carrier absorption further on the outer diameter and reduce it on the inner diameter because the mode is pushed outward, so a lower loss penalty could be received by bringing the inner diameter Ohmic contact implant closer to the core and pulling the outer diameter implant further away to achieve the same reduction in series resistance; since the anode introduces more series resistance, this could be a strong counter-argument against having the anode on the outer diameter for FCPDE enhancement. An alternative approach to achieving the overall bandwidth target that would introduce less loss is to increase the target electro-optic bandwidth and lower the electrical bandwidth target; for example, an electro-optic bandwidth of at least 36 GHz reduces the electrical bandwidth requirement to about 24 GHz, which can be achieved with both Ohmic implants placed about 765 nm away from the edge of the core. Using Figure 5.5.b again as a rough guide, it is assumed that the additional free carrier absorption loss is small enough to be considered a negligible contribution for this device and will be ignored.

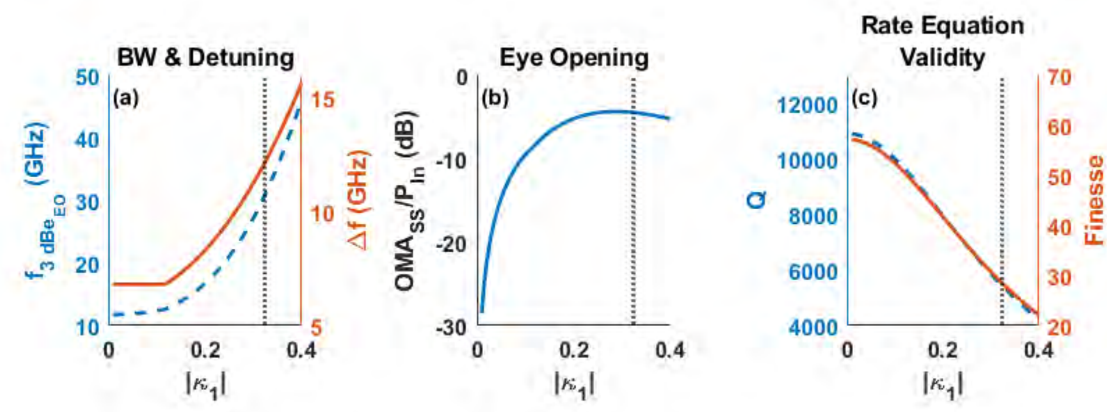

Figure 3.24: Simulation of electro-optic 3 dB bandwidth and ideal detuning (a), normalized steady state optical modulation amplitude (b), and Q & $\mathcal{F}$ (c) for a circular all-pass ring resonator with a bend radius of 9.74 μm and the depletion-mode phase shifter occupying its entire circumference. The phase shifter is reverse biased at -0.6 V with a 1.2 V peak-to-peak modulation applied. The dashed black vertical lines in each plot indicate the critical coupling point.

Now that the target electro-optic bandwidth is known, a sweep of some of the steady state and small signal expressions listed in the previous section can be conducted to find the right coupling coefficients to optimize modulator performance; since it is assumed that the drop port coupling magnitude will be much smaller than the through port to drop the amount of power needed for the control circuitry to align the ring, an all-pass ring will be first explored, and later including the drop port will serve as an exercise on how this perturbs performance. Additionally, it is assumed that the entire circumference of the ring resonator will contain the phase shifter and that the passive waveguide loss adds an additional 3 dB/cm of loss to the active regions of the cavity. The results are shown in Figure 3.24. Achieving the target electro-optic bandwidth requires $|\kappa_1| \approx 0.35$ and results in a normalized optical modulation amplitude ($OMA = P_1 - P_0$ for NRZ) of about -4.65 dB in the steady state; normalized OMA_{SS} peaks at about -4.33 dB for $|\kappa_1| \approx 0.285$ which is slightly undercoupled (as expected). In an ideal circumstance, in order to maximize OMA_{SS}, the coupling point would be chosen at this point if the overall device bandwidth would not be hindered. Therefore, it is much better to be in a condition where there is plenty of available electrical parasitic modulation bandwidth so that a coupling coefficient with a lower electro-optic bandwidth but higher OMA_{SS} can be selected. $a = 0.9475$, which means some tenths of dB can be gained at the drop port by pulling it closer to the through port when it is added. For the target coupling strength, the ring has a Q of about 5000 and a finesse of about 26.

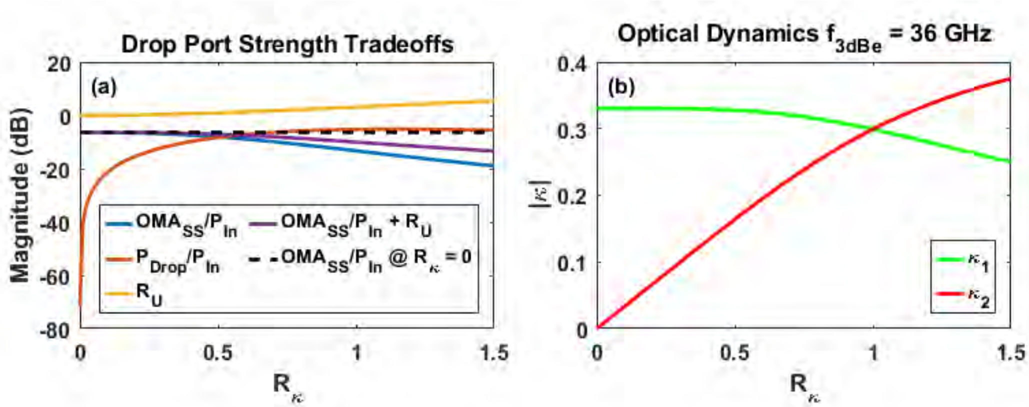

Figure 3.25: Simulation of the addition of a drop port to the ring modulator and its impact on a few steady-state characteristics (a). Coupling coefficient magnitudes of each port while maintaining the target electro-optic modulation bandwidth (b).

By now examining the small signal and steady-state equations for an add-drop ring resonator, the ideal drop port coupling strength can be chosen given the tradeoffs presented. The main utility that must be achieved in this design is providing the expected peak dropped power that the electronic controller is expecting (about 2 μW with an input power of about -5 dBm). As shown in Figure 3.25.a, this is achieved for a drop port to input port coupling magnitude ratio $R_\kappa = \frac{|\kappa_2|}{|\kappa_1|}$ of about 0.09 (or $|\kappa_2| \approx 0.03$ from Figure 3.25.b). Figure 3.25.a also shows that such a small R_κ selection does not really affect normalized OMA or $|\kappa_1|$ for this design, but increasing R_κ does generally degrade OMA. This is because there is an interplay in R_κ and maintaining the same modulation bandwidth, where higher R_κ produce a less overcoupled/more undercoupled cavity (approaching an OMA maximum if overcoupled at $R_\kappa = 0$) but also increase the $FWHM$ (decreasing the maximum achievable OMA). Increasing the $FWHM$ also increases the maximum input power before (expressed as $R_U = \frac{U(R_\kappa=0)}{U(R_\kappa)}$), which could enhance the maximum achievable OMA in certain circumstances (albeit by accepting a proportional energy efficiency reduction); to see this added benefit, the initial all-pass ring must be strongly overcoupled.

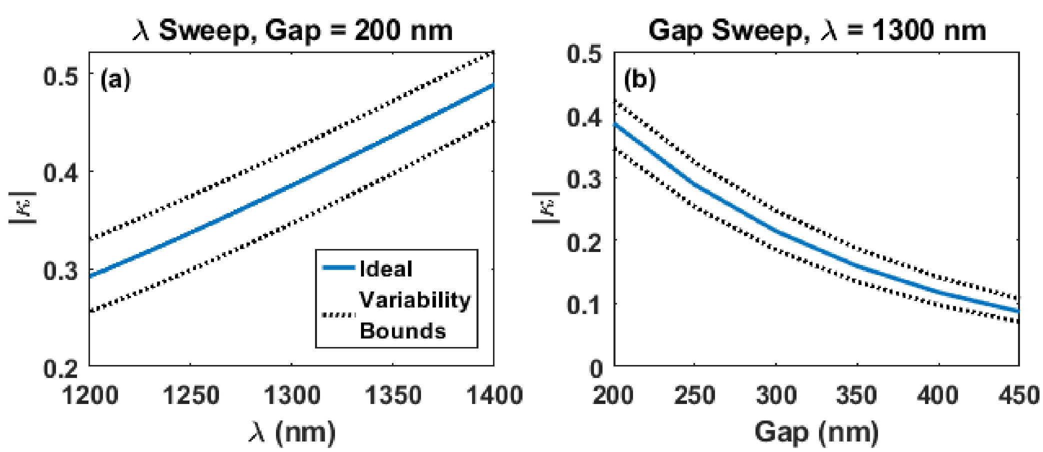

Figure 3.26: Simulation of $|\kappa|$ for a rib waveguide-based point coupler with a slab thickness of 110 nm and a rib thickness of 220 nm as a function of wavelength (a) and separation between the bus and ring waveguides (b) for an ideal, vertical shallow etch and with perturbations from the ideal. The range of variability in core width was assumed to be ±4.25 nm, device thickness ±4 nm, and shallow etch depth ±10 nm.

With the target coupling coefficients in mind, couplers must be designed with the selected ring and bus waveguide geometries. Designing the couplers usually requires

FDTD simulation, though there are analytical methods for estimating expected κ for various coupler geometries [6]. Figure 3.26 depicts the FDTD simulated coupling coefficient magnitudes for a straight bus waveguide "point" coupler (Figure 3.27.a) for a thicker slab width (for showing trends but not picking an exact value). The coupling coefficient can change dramatically over 200 nm of wavelength bandwidth, but the narrow spectral regime of this project (1.2 THz $\approx$ 6.76 nm in the O-Band) makes this not a primary concern. However, the fabrication error corner cases could contribute a stronger effect on device performance [71]; the simulations suggest $|\kappa|$ decreases most when the device layer thickness and the shallow etch depth increase (both increase core confinement without affecting gap width). Since the simulated point coupler with a slab thickness of 110 nm is only barely sufficient to achieve the needed κ_1 for the device being designed, it is likely that the target waveguide geometry with a slab thickness of 60 nm will not be able to make the through port coupler unless the gap between the bus and ring waveguide can be made smaller. If that is not possible, coupling can be enhanced by tapering the core width at the coupling region [66] or increase the interaction length of the coupler with a pulley design (Figure 3.27.b).

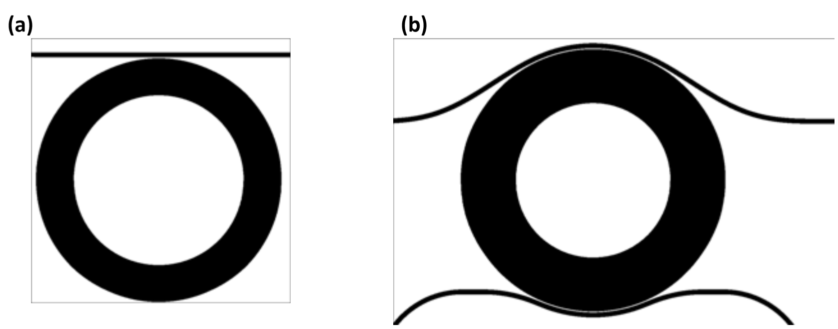

Figure 3.27: Schematic depicting rings with straight point couplers (a) and pulley couplers (b).

With all of the parts of the design cornered down, the large signal model can be used to simulate the cold-cavity output optical waveform. A PRBS7 sequence is generated with the help of a linear feedback shift register program [72]. The eye diagrams of the through and drop ports are plotted in Figure 3.28. Beyond the previously-observed opposite magnitude of ringing causing differences in the output eye for the through and drop response, the drop port eye seems to be a bit offset in time from the through port eye.

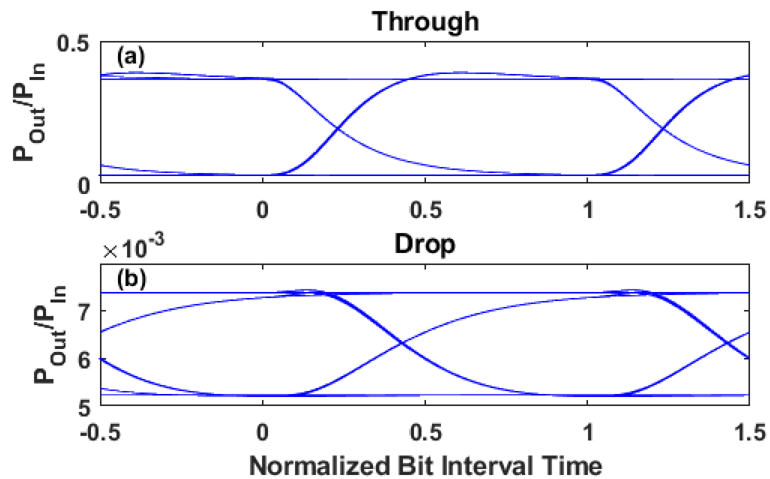

Figure 3.28: Simulated normalized optical eye diagrams for the through port (a) and drop port (b) of the designed ring modulator. The driving voltage waveform has a magnitude of 1.2 V

Figure 3.29 depicts the additional spectral content centered around the carrier frequency that modulation introduced. One interesting observation is that the magnitude of the negative frequencies appears to be greater than their positive counterparts.

While a similar ring modulator design was laid out on a silicon photonics foundry MPW run 18 months prior to the writing of this thesis, the manufactured device was not available for testing prior to writing. Tests to validate models using this device will be treated as future work.

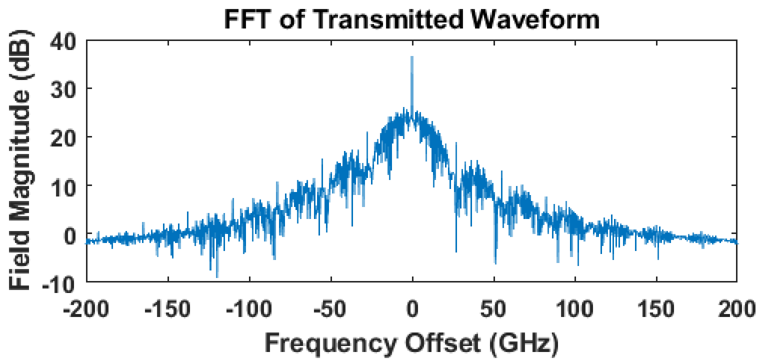

Figure 3.29: Baseband spectrum of the through port optical waveform.

3.3.2 Design Considerations for Cascaded Rings

There are many aspects of design that become more complicated when considering the design of a series of rings on a common bus. A more mundane factor common to any dense PIC is placement of the overall unit cell (ring, drop port photodiode(s), add port waveguide termination, ring coupler-to-bus transitions, etc.). With a high local area bandwidth density of 5 Tbps/mm^2 leading to a flip chip pitch of 36 μm, the unit cell would ideally fit into a footprint of 36 μm x 72 μm. This could be difficult to manage without introducing unwanted design penalties or adding complexity to metal routing of the low-speed signals out of the dense RF region (ring DC biasing, monitor photodiode electrodes). If such dense placement is too burdensome, the unit cell can be distributed over a larger area just as long as the RF region of the cell (TX modulator phase shifter and RX photodetector) is located in the high-density area to reduce high-speed signal degradation; distributing the unit cell could cost extra waveguide routing losses, however. Another thing worth considering with regards to placement is that a sudden index change at the ring coupler could introduce a weak reflection on the bus waveguide [73, 74]; cascading multiple rings together could effectively make a series of weak Fabry-Pérot cavities that could distort the optical spectrum and introduce amplitude noise as the temperature of each of these cavity fluctuates (commonly referred to as multipath interference) [75, 76, 77].

A critical aspect to the cascaded rings is that each element is appropriately aligned to the spectral grid of the system; for the target application of this dissertation, that means within a bank of 10 rings having an even resonance separation of 120 GHz to match a deinterleaved QD-MLL comb. Further, that ring "comb" needs to be aligned correctly in frequency to either the odd or even deinterleaved QD-MLL sub-comb; correct alignment is the OMA-maximizing detuning point for modulators and on resonance for demux filters. The ring ring comb in the alternate deinterleaved path must be 60 GHz offset from this comb to appropriately receive its QD-MLL sub-comb as well. Further confounding this alignment problem is that every set of odd-even and TX-RX pairs of ring buses that share a QD-MLL comb source must meet these alignment criteria at the same time to achieve the full capacity of the system. Much like as was described for the deinterleavers in the previous chapter, a ring's resonance placement in the frequency domain can be perturbed by changes in the effective length of the cavity.

$$\Delta f_0 = \Delta\nu \frac{\Delta\phi}{2\pi} = \frac{f_0}{n_g}\left(\Delta n_{eff} + n_{eff}\frac{\Delta L}{L}\right) \tag{3.37}$$

One energy efficient way to introduce passive offsets between the rings is to perturb each ring to achieve the correct resonance offset needed for the grid. This can be done by slightly changing the waveguide cross section to change the effective index or slightly changing the physical path length; it should be noted that because rings must include bends to complete the cavity, changing the path length (either through changing bend radius or including a racetrack section with varying lengths) always perturbs the average effective index too [53]. For example, if the ring modulator designed had its waveguide cross section remain the same but its radius was changed from 9.74 μm, a 60 GHz offset could be produced with a change in radius of about 3.94 nm. Unfortunately, most masks do not have sufficiently fine resolution to hit that exact target, so some manipulation of the waveguide cross section will be needed to deal with this quantization error present from the mask minimum address unit. Ideally, minimally perturbing the free spectral range in the process of changing the resonance frequency is important because it affects the required ring tuning ranges and interaction between neighboring channels. For example, applying the +3.94 nm change in radius to achieve the +60 GHz resonance frequency shift decreased the free spectral range by about 0.49 GHz, so the free spectral range would vary by about 9.8 GHz across all 20 devices with slightly different radii.

While perturbations to the effective path length was framed as a means to reduce energy consumption for grid alignment, it is also one of the fundamental hurdles to utilizing rings in PICs: their susceptibility to changes in temperature and waveguide dimension fluctuations. Since rings are infinite impulse response filters, they cannot be compensated in the same way that the deinterleaver can. The waveguide cross section can be adjusted to be more robust to these issues, but this is usually at the expense of performance [66, 78, 79]. Because of this, the rings will need some phase correction to form the spectral grid and to compensate for thermal drifts. One fortunate feature is that rings placed close to each other in the reticle are much more likely to encounter the same degree of perturbation in each dimension, so relative passive offsets like those described in the previous paragraph are relatively stable [80].

Figure 3.30 illustrates the problem outlined in the previous paragraph. If the resonance frequency of each ring design were measured across the wafer and plotted as a histogram, a distribution of resonant frequencies of each device will be present that reflects the degree of wafer-scale waveguide dimension fluctuations. The neighboring rings will have their resonances spatially correlated to the first measured device, but they will likely not exactly be located on the idealized grid separation that they were designed for. Therefore, some degree of DC tuning will be needed to first correct for the error

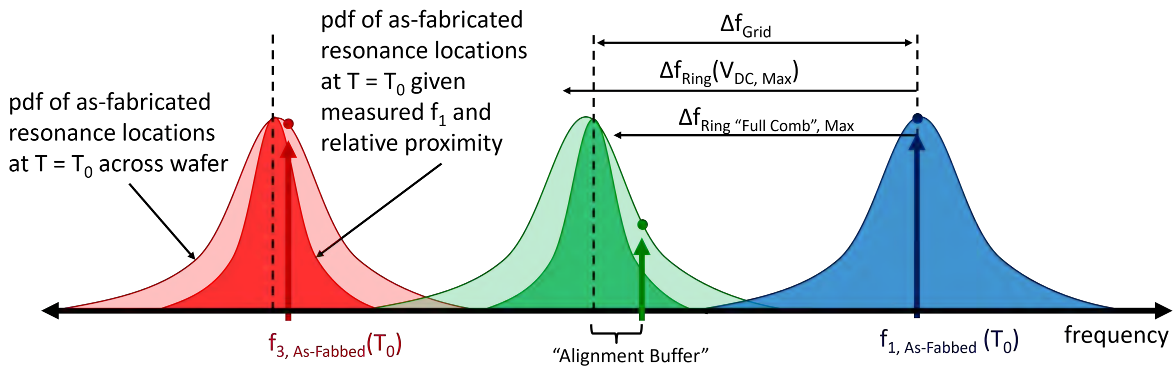

Figure 3.30: Illustration of variation in resonance frequency in a series of rings on a bus due to wafer-level dimension variations and spatial correlation.

in the grid separation, and more tuning will be needed to align that comb of rings to the QD-MLL grid and maintain that grid placement as temperature drifts; over a 60 °C temperature span, the rings would experience roughly a π phase shift that must be handled. As will be discussed in more detail in Chapter 4, utilizing the FCPDE instead of thermo-optic phase shifters as the means for DC correction of the resonances is the preferred choice in current silicon photonics foundry offerings for a barrel shifting approach to ring alignment from an energy efficiency perspective if it can supply a sufficient degree of phase shift [81, 82].

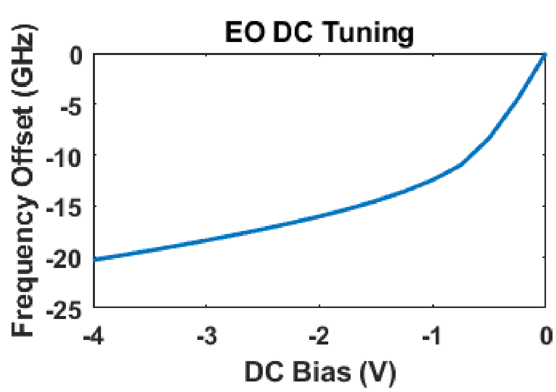

Figure 3.31: Simulated frequency shift across a 4 V span for the simulated ring modulator.

Figure 3.31 shows the expected DC tuning range of the integrated modulator is about

20 GHz, which greatly falls short of what is needed to fully realize the implementation. In general, this is not a positive sign for using standard foundry MPW offerings to make p-n junction phase shifters with the performance needed for this application; either a custom process is needed or a foundry offering with a stronger FCPDE magnitude phase shifter technology like SISCAP should be sought. In order to bridge the gap between the ideal circumstance when there is enough remaining FCPDE DC tuning range to handle all thermal drifts with just ring correction (Figure 3.32.a), the grid can be dynamically adjusted by changing the tuning of the QD-MLL and interleaver (albeit there is a much larger latency penalty for doing things this way). It is important to keep in mind that there are 16 banks of 10 rings in the proposed 2 Tbps system that must align to the same QD-MLL grid, and the the ring comb with the smallest degree of as-comb DC frequency tuning range defines that range for the whole 2 Tbps system. When that as-comb tuning range is less than an uninterleaved QD-MLL carrier separation (Figure 3.32.b), the interleavers and QD-MLL must be offset in frequency when the ring range is exhausted so that the rings can stay on the dynamic grid; if there is no as-comb ring tuning range, the interleavers and QD-MLL must be tuned continuously. When the as-comb tuning range is in between the uninterleaved and interleaved QD-MLL carrier separation (Figure 3.32.c), the QD-MLL can be left stable, and a π phase shift can be applied to the interleavers to perform a sort of cross-bar switch operation.

While the appropriately-aligned grid of ring resonators will have only 1 carrier overlap strongly with the intended resonance, there is still some steady state off-resonance loss penalty from the other 9 rings due to the normalized intensity lineshape converging to a value less than 1 at $\phi = \pi$. This leads to the other 9 resonance lineshapes on a bus of 10 ring modulators acting as “aggressors” to the “victim” carrier frequency. All ring modulators should experienced roughly equal off-resonance losses, but the demux filters will not– the first demux ring in the bus experiences no off-resonance losses, the

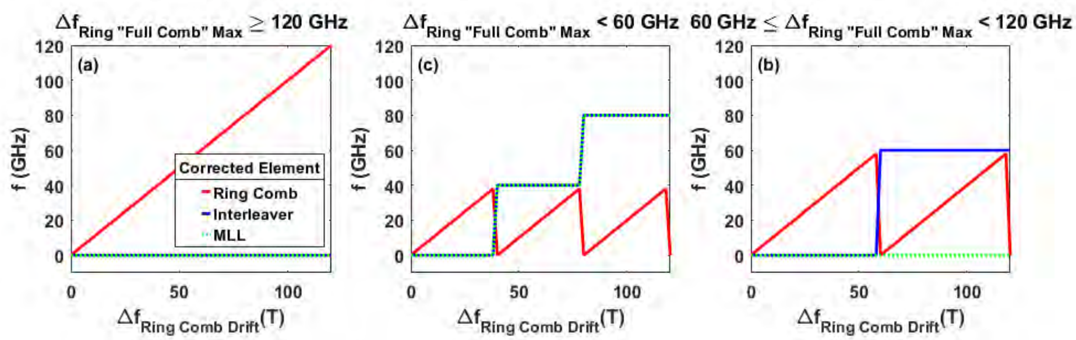

Figure 3.32: Plots demonstrating how to keep the rings, interleaver, and QD-MLL aligned as the PIC temperature changes for the 3 regimes of as-comb ring bank DC tuning range.

second ring experiences 1 off-resonance loss, and so on. The amount of off resonance loss each sequential demux filter receives depends on the order of channels dropped. The ring modulator designed in this section should expect about 0.53 dB overall off-resonance loss, and the maximum amount of off-resonance loss for the demux filter will be discussed in the next subsection.

Beyond the static power penalties incurred from off-resonance losses, there are also four forms of crosstalk the rings can induce: dropped power at the modulator, encoding by modulator, dropped power at receiver, and filtering of through response of the aggressor demux filters along the path of being dropped at its own demux filter [83, 84]. As will be shown in more detail in Chapter 4, fully quantifying dropped power-based modes of crosstalk can be difficult to estimate because it depends on the prominence of the drop resonance passband relative to the noise floor, which can be limited by things like minute coupling of higher order modes into the cavity and unguided light scattering around the PIC. The two demux filter-based crosstalk methods are in part affected by the shape of the filter response and will be a topic for the next subsection. One simple way to estimate the intermodulation crosstalk from the aggressor rings on the victim channel is to compare their cumulative aggressor OMA_{SS} to that intended from the victim channel.

$$XTalk_{TX,Interchannel} \approx \frac{\sum_{k=1}^{N_{Channels}-1} OMA_{SS,Aggressor_k}}{OMA_{SS,Victim}} \tag{3.38}$$

By this estimate, the designed ring modulator is expected to encounter about -12.5 dB of interchannel crosstalk under ideal circumstances, which is concerningly high. Generally speaking, most of these forms of crosstalk will be enhanced when $FWHM$ increases, the number of channels increases, or the frequency separation between channels decreases.

3.3.3 Demux Filter Design

While the primary tradeoff for ring modulator design is to balance maximizing OMA against having sufficient modulation bandwidth, the design challenge for the ring-based demux filter is to redirect the target data channel to the filter's drop port photoreceiver with minimal signal losses and signal distortion while also maximally rejecting the signals of the aggressor channels. In the interest of not introducing a thermo-optic phase shifter into the ring from an energy efficiency perspective, the same depletion-mode p-n junction phase shifter design will be utilized in the development of this demux filter to apply the needed frequency corrections.

Though the EO tuning electrical circuit consumes less power than the thermo-optic solution, introducing the integrated p-n junction phase shifter into the ring introduces more round-trip losses and degrades cavity Q. This Q spoiling is not an insurmountable issue for the RX ring since the Q of devices with a $FWHM$ required to adequately demultiplex a 26.4 Gbps channel is a similarly low value as that required by the modulator [85]. However, if the filter bandwidth is too large, more inter-channel crosstalk can be picked up by the filter; this can be corrected for by reducing the coupling coefficients of the rings to target at the expense of less demultiplexed power received at the drop port of the ring. Thus, there are trade-offs between tuning range, filter drop bandwidth, induced optical loss, and crosstalk.

The round-trip losses of an RX filter can be much less than those of a modulator since the time constants associated with thermal drifts are much slower than the target channel rate; this allows for changing the integrated phase shifter design by pulling high concentration implants away from the core at the expense of increased series resistance and a slower RC time constant. While this phase shifter design already has the Ohmic implants far away from the junction, losses can be driven down a bit further in this design by not running the mid level P+ and N+ implant layers to their electrodes as they currently are (they are technically just needed to form the junction). Since the same amount of charge is still depleted at the junction, these devices should have the same frequency tuning performance as the TX modulators. Additionally, forming the demux filter out of multiple cascaded rings(either as isolated or coupled cavities) can produce a flatter passband, but doing so increases the complexity of the locking circuitry, electronic and photonic footprint, and drop port losses [7, 86, 87, 88, 89, 90]; therefore, a design featuring a single ring to form each filter was selected.

After the waveguide geometries have been selected, the next task is to select the design target $FWHM$; intuition would suggest it should be at least twice the data rate to reduce filtering of the intended demultiplexed channel, but a more refined answer can be determined with system level link simulations in which $FWHM$ of the demux filter is swept to find an optimum. System simulations suggested $FWHM$ should be about 60 GHz to maximize signal integrity. Since it was established in the modelling section that maximizing dropped power occurs when critically coupled, determining the input and drop port coupling coefficients of a single-ring demux filter is a simple matter once the finesse and a targets of the design have been chosen.

$$|\sigma_1|^2 = \frac{1 - \sqrt{1 - \cos^2\left(\frac{\pi}{\mathcal{F}}\right)}}{\cos\left(\frac{\pi}{\mathcal{F}}\right)} \tag{3.39.a}$$

$$|\sigma_2| = \frac{|\sigma_1|}{a} \tag{3.39.b}$$

The result is a ring for which $|\kappa_1| \approx 0.38$, $|\kappa_2| \approx 0.22$, and $Q \approx 3800$ (lower than the Q of the modulator). It is likely the input port would need to be achieved with a pulley coupler, and a point coupler could be sufficient for the drop port. For $\psi_a = 0.5$, the excess loss penalty at the resonance of the drop port is 5.0 dB, and the maximum off-resonance loss that the last demux filter on the bus experiences is expected to be about 0.87 dB. The through and drop response of this device design are plotted in Figure 3.33.

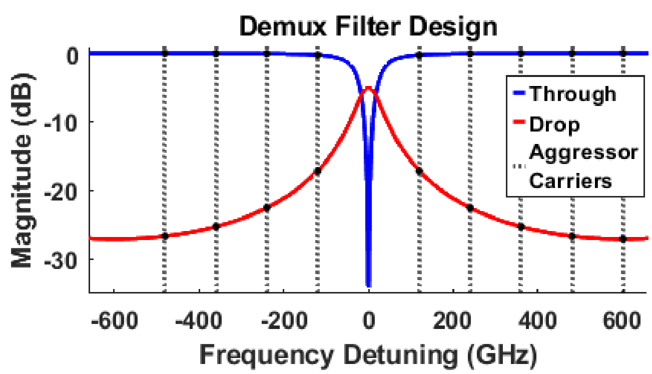

Figure 3.33: Simulated through and drop spectra for the given ring demux design with 0 V reverse bias applied to the integrated phase shifter. The frequency positions for the 9 aggressor carriers when the target channel being demultiplexed is Channel 5 is overlaid onto the spectra.

Figure 3.34 depicts the simulated eye diagrams received by the demux filter from the ring modulator. This was achieved by taking the fast Fourier transform (FFT) of the ring modulator output waveform to apply the demux filter response to the data. Most of the modulator output waveform is successfully dropped by the filter, and the waveform is minimally distorted.

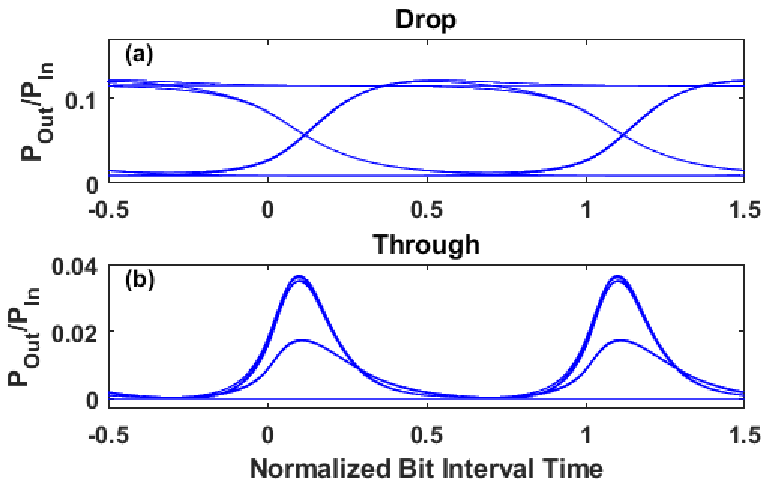

Figure 3.34: Simulated eye diagrams for the drop (a) and through (b) ports of the designed ring demux filter receiving the ring modulator through port waveform on resonance.

An attempt was made to input the modulator output waveform into the large signal model for the demux filter parameters to produce the output through and drop responses as well, and the baseband spectral content of the result is plotted in Figure 3.35, along with that of the modulator through port output and the FFT approach to the demux filter. It appears that the outcome of this attempt is that the low frequency components are overly dampened compared to the FFT approach, and the magnitudes at the intermediate frequencies match closer to the input wave than that expected from the FFT approach. The reason for this disagreement remains unclear, but it is possible that the problem lies with the current implementation for inputting the modulated waveform as if it was all occurring at one frequency, which distorts the round-trip phase relationship of the constituent frequencies in the waveform spectrum. Regardless, more study is clearly needed for implementing the large signal travelling wave model with time-varying input signals and multiple input frequencies, which is a critical aspect for capturing other effects like crosstalk and nonlinearities.

While probably not an entirely useful exercise outside of a full system simulation that

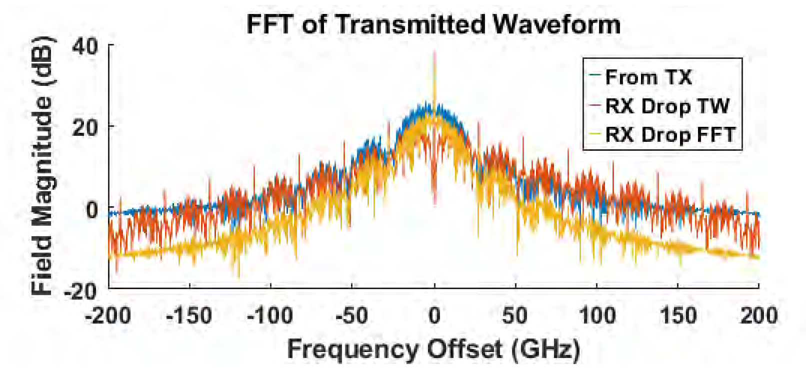

Figure 3.35: Baseband spectrum of the through port optical waveform before

captures all the dimensions of signal distortion in both the electrical and optical domains, a bit error rate BER can be estimated to the received data at the demux filter drop port. The equation for bit error rate provided in [91] can be generalized to describe the not only the BER but also the symbol error rate SER of higher-order IM/DD modulation formats such as PAM-4 and PAM-8 as well as NRZ.

$$SER = \sum_{k=0}^{2^N-1} \sum_{m \neq k} p(k) P(m|k) \tag{3.40.a}$$

$$BER = \frac{1}{N} \sum_{k=0}^{N-1} p(b_k = 1) P(b_k = 0 | b_k = 1) + p(b_k = 0) P(b_k = 1 | b_k = 0) \tag{3.40.b}$$

$$SER \approx 1 - (1 - BER)^N \tag{3.40.c}$$

In the above equations, $p(k)$ is the probability of occurrence of symbol k, $P(m|k)$ is the probability of mistaking an occurrence of symbol k for that of symbol m, N is the number of bits per symbol, and b_k is the k-th bit of the symbol. Figure 3.36 shows that, as expected, the wide-open simulated eye that captures little of the primary noise sources would have no trouble discerning between the two symbol levels. Also as expected, without the presence of noise, the ringing on the bit transitions makes a Gaussian distribution a poor fit.

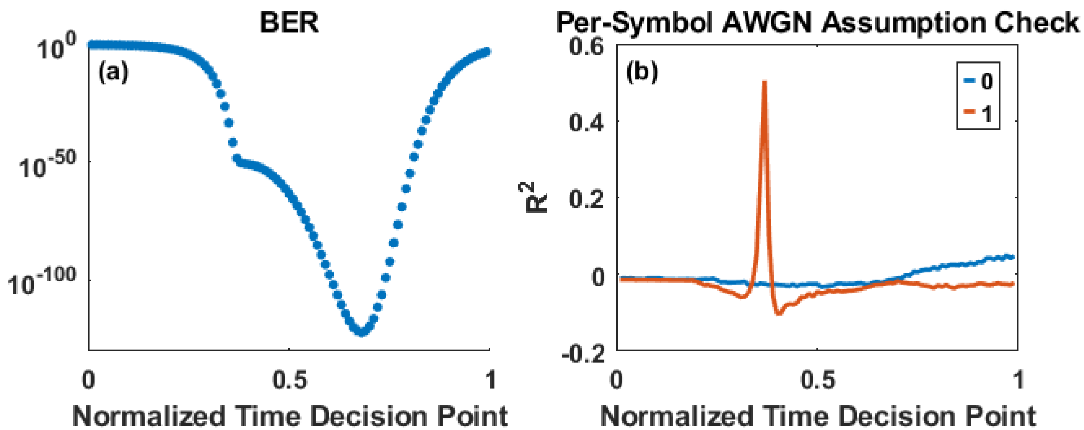

Figure 3.36: Error rate estimation for the received eye at the demux filter drop port as time decision level is swept and assuming Gaussian statistics to the symbol levels (a). Coefficient of determination of the distributions at each symbol compared to their Gaussian fits (b).

3.3.4 Design Considerations for Electronic Copackaging

Within an integrated system, there are also some interactions with the electronics to consider in the design. For example, there may be an upper limit on modulator capacitance that the driver can handle, which can put upper limits on the amount of phase shifter charge displacement or encourage segmented modulators with separate, synchronized drivers. There is also typically an upper limit in the amount of DC bias a ring alignment circuit can supply, so the required FCPDE-based DC tuning frequency displacement span must be achievable with the voltage span that the controller can supply without any onset of dielectric breakdown (these IC-based voltage sources with wide voltage span cannot handle much current). The ring alignment circuitry also must be designed with an anticipated upper bound on input photocurrent and a particular

ADC resolution, so a ring modulator's drop port coupling strength must be designed based on the amount of needed photocurrent and the anticpated amount of input power to the device.

3.3.5 Design Considerations for SISCAP/MOSCAP Phase Shifters

High charge displacement devices like SISCAP phase shifters (or perhaps high-concentration depletion p-n junctions) can have their loss characteristics change significantly enough across their full DC biasing span that their coupling condition will change appreciably; therefore, ring modulators must be designed to be overcoupled in a low accumulation regime so that OMA is optimized for the entire range of loss conditions it will experience in its operation (as shown in Figure 3.37). This dramatic change in loss conditions also has consequences for the ring alignment circuity because the optimum detuning magnitude for maximizing OMA for a modulator and the amount of power received at the drop port will change with the round-trip loss in the cavity. The amount of drop port excess loss a ring demux filter would encounter would increase with more accumulated charge and its $FWHM$ would expand. The $FWHM$ expansion would introduce voltage-dependence to other factors like crosstalk and power handling for both the modulator and demux filter.

3.4 Conclusion

The fundamentals of ring resonators and integrated phase shifters were established. Several new equations for describing ring resonators were developed in the process. Applying these fundamentals to design ring-based elements for DWDM transceiver PICs was then performed.

Given the wide range of tradeoffs present for rings used both as WDM modulators

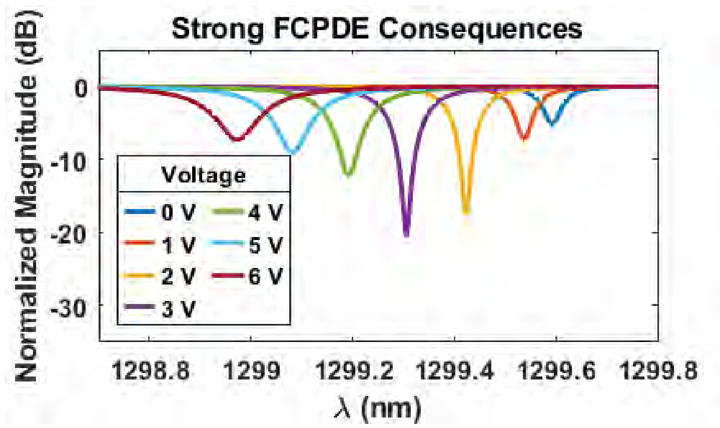

Figure 3.37: Plot of a simulated all-pass ring spectrum containing a SISCAP phase shifter as the amount of accumulated charge is increased.

and demultiplexing filters, it is clear that ring resonators should be optimized in design for their target application, and doing so requires detailed knowledge of the fabrication process and its uniformity; further, not every standard silicon photonics foundry process is capable of meeting the all needs of such a demanding project as this dissertation topic. Achieving the best design in a large system also requires an intimate knowledge of how the elements of ring design interact with the rest of the system to ensure that the entire scope of constraints on the design are well understood.

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Chapter 4

Systems

4.1 Introduction

This chapter focuses on the progress of practically implementing the short-reach optical interconnect system architecture presented in the introductory chapter. Systems arise from a collection of components, so the individual components are first evaluated. Afterwards, the progress on bringing these components together to test the viability of the system is covered.

4.2 Components

This section provides descriptions of the design and performance of the constituent photonic, electronic, and packaging elements that comprise the system in isolation of one another; additionally this section will motivate the need for forward error correction as an energy efficient means of achieving the target error rate. While the author was not directly responsible for the design and measurement for many of these components, he at the very least guided many of their designs to fit the needs of the overall system.

Regardless, a cursory outline is still warranted for analyzing the viability of the integrated system.

4.2.1 Quantum Dot Mode Locked Laser Comb

The QD-MLLs used in this system consist of a Fabry-Perot laser structure with a saturable absorber (SA) made from the same material as the gain medium. The SA is formed by electrically isolating part of the laser ridge from the gain section by etching through the p-contact and part of the p-cladding layers in the region between the gain and SA regions. By using this laser design, it eliminates the costly grating patterning and regrowth steps involved in commercial DFB fabrication. The performance of the MLL can be tuned by changing the reverse bias voltage applied. The details of the device fabrication and performance are provided in [1].

With extremely stringent power consumption requirements of short reach interconnects, the wall plug efficiency (WPE) of the laser is extremely important. Figure 4.1 shows the light-current and WPE curves for a 60 GHz QD-MLL which reaches a peak WPE of 17% free space. However, the bandwidth of the comb also affects the efficiency of generating data channels; having too narrow or too broad of a bandwidth produces channels with low power and efficiency. To track this, the twenty contiguous comb lines with the highest power are identified from a spectrum (shown in Figure 4.1.b), and the comb line with the lowest power is divided by one twentieth of the electrical power consumption of the laser. This calculates the WPE of the worst comb line that will be used as a data channel, referred to as WPE20. These devices have been verified to emit equal power from both facets so the output collected by one facet is multiplied by a factor of two in calculating WPE20. Figure 4.1.c shows the WPE20 of a device as a function of drive current and SA reverse bias to identify the most efficient comb state.

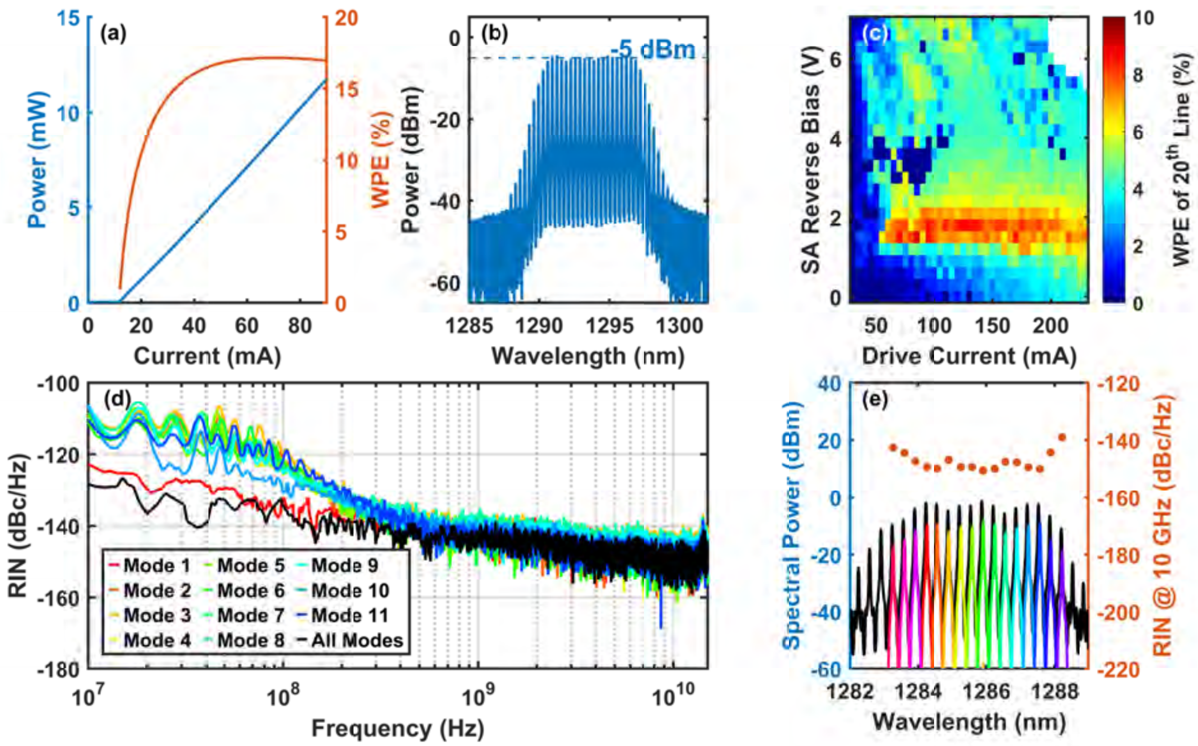

Figure 4.1: Light-current output and wall plug efficiency of a QD-MLL (a). Optical spectrum Wall plug efficiency of generating the 20th comb line assuming 20 comb lines are used for data transmission (c). Comparison of the measured RIN for different comb lines versus the entire spectrum (d). Comb state and RIN at 10 GHz for different comb lines in a QD-MLL spectrum (e). Colored spectra correspond to bandpassed individual comb lines measured in (d). *Data courtesy of Mario Dumont and Bozhang Dong.*

For IM-DD links, the relative intensity noise (RIN) of the laser is important because high RIN levels degrade the overall link-performance. The RIN characteristics of an FM comb were investigated and are shown in Figure 4.1.e. Each comb line was filtered with a tunable OBPF to evaluate the RIN of a single line versus the entire comb spectrum. In this study, the measured RIN accounts for the shot noise and the thermal noise without average [2], which is dependent on the output power. Considering the additional loss from the optical filter, the maximum fiber-coupled power of an individual comb line is limited to -9 dBm. As such, the RIN of the whole spectrum at a power level of -9 dBm was measured for a fair comparison. The entire comb spectrum has a similar RIN value to each individual line from 0.1-18 GHz, which is as low as -151 dBc/Hz at the frequency offset of 10 GHz. It should be noted that the RIN measurement is limited by the thermal noise of the photodetector when the fiber-coupled power is below 3 dBm. For our device studied, the RIN at 10 GHz of the whole spectrum further decreases to -165 dBc/Hz once the measurement is no longer limited by the thermal noise. In Figure 4.1.d, the RIN of each comb line is plotted to show that there is no change across the entire spectrum.

4.2.2 Silicon Photonics

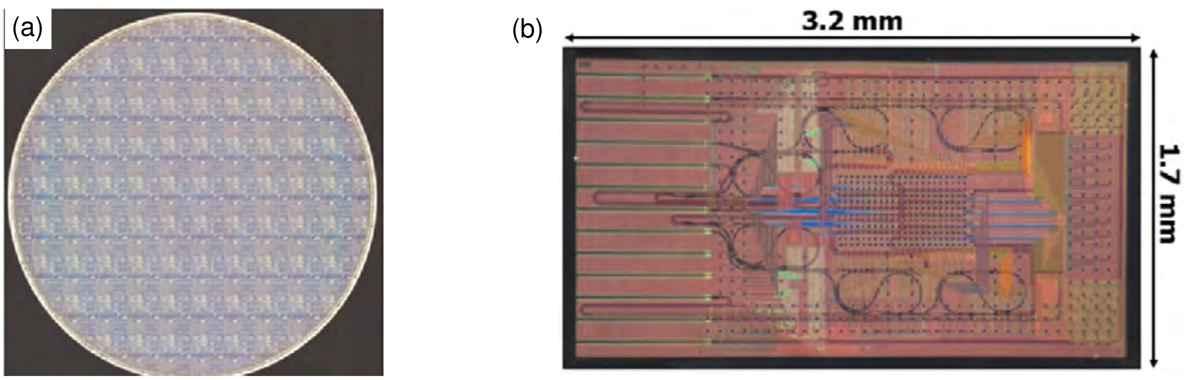

Figure 4.2: 300 mm wafer of silicon photonic transceivers (a). Micrograph of a silicon photonic 1 Tbps transceiver PIC (b).

Figure 4.2 depicts a fully processed 300 mm silicon photonics wafer and an image of an individual 1 Tbps transceiver PIC. A number of silicon photonic components needed to be designed and working in tandem for the system to be operational. This includes athermal interleavers, high-speed modulators, variable optical attenuators, low-loss edge couplers, RX demux rings, and finally photodetectors. The performance of the athermal deinterleaver used in this system, as well as techniques to optimize it for enhanced fabrication tolerance, is discussed in detail in Chapter 2. The other components will be evaluated in the following subsections.

4.2.2.1 Edge Couplers

The inverse taper edge coupler in this system is optimized for coupling to standard SMF-28 fiber, which has a mode field diameter of $\sim$10 μm. In order to support polarization multiplexed links, the edge coupler is designed for both TE and TM polarizations. The buried oxide (BOX) layer between the device layer and the silicon substrate that silicon foundries typically use is 2 μm thick [3], which is thin enough to increase loss of edge couplers that are designed to match SMF-28 fiber modes due to substrate coupling. A substrate etch and oxide deposition is performed near the start of the fabrication process in order to effectively increase the BOX thickness, as shown in the cartoon and micrograph in Figure 4.3.a. Figure 4.3.b plots measurements of excess loss of the edge coupler for each mode when coupling to SMF-28 fiber. A uniform broadband insertion loss of $\sim$1 dB was measured for each mode.

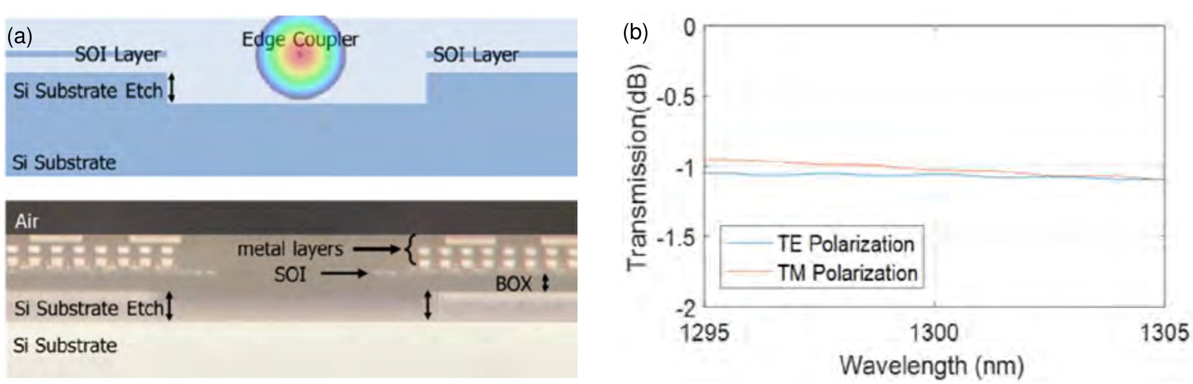

Figure 4.3: Low-loss edge coupler concept and micrograph with silicon substrate etch (a). Measured transmission of edge coupler to SMF28 fiber (b). *Data courtesy of Analog Photonics.*

4.2.2.2 Polarization Beam Splitter and Rotator

An integrated polarization beam splitter and rotator is required to polarization demultiplex the two 500G lanes at the receiver. Figure 4.4.a shows that the insertion losses

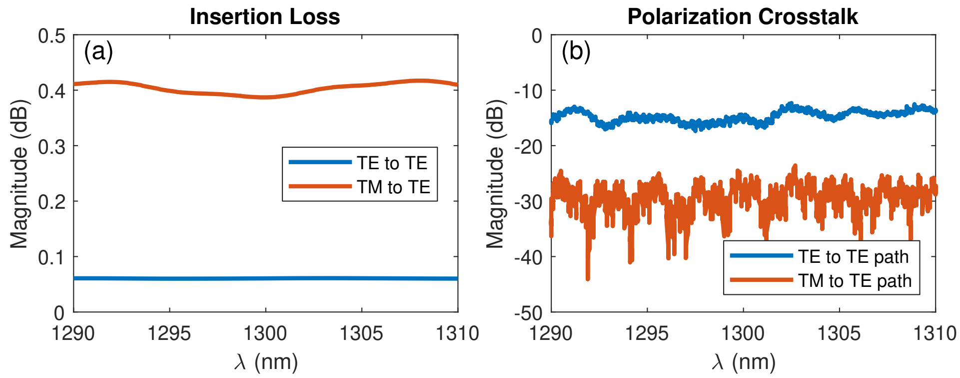

Figure 4.4: Insertion losses of the silicon photonic polarization beam splitter and rotator (a). Measurement of polarization crosstalk for each path when the undesired input polarization is excited (b). *Data courtesy of Analog Photonics.*

for TE and TM input light are about 0.06 and 0.40 dB at 1300 nm, respectively, for the fabricated device. Additionally, measured polarization crosstalk results are shown in Figure 4.4.b. The peak crosstalk magnitude for the TM input to TE output path is approximately -23.5 dB, which is likely sufficient to close the link. The crosstalk on the TE input to TE output, ranging between -13.0 and -17.3 dBm, may be significant enough to impair signal integrity.

4.2.2.3 Ring Resonators

There are two types of ring resonators: the TX-side modulator that encodes the high speed optical waveform and the RX-side filter that wavelength demultiplexes each channel. Figure 4.5.a shows an example transmission response of the ring modulators. These devices have a loaded Q of ∼4600 and a free spectral range (FSR) of 1.2 THz; this leads to a finesse of about 24, which is similar to the simulated ring modulator design in the previous chapter. As shown in Figure 4.5.b, power buildup inside the cavity introduces nonlinear losses and self-heating that limits the incident power on the ring near -5 dBm before the resonance shape distorts and redshifts [4]; this effectively limits the amount of useful power the QD-MLL can provide each carrier without splitting the comb power over multiple PICs. To encode the data onto a carrier, the resonance is redshifted by reverse biasing an integrated p-n junction phase shifter within the cavity to deplete charge; Figure 4.5.c shows the resonance can be shifted by 52 GHz over a 5 V span before exhibiting the onset of breakdown characteristics. This large DC tuning also be used to correct for low-speed wavelength misalignment from temperature drifts and fabrication deviations. Figure 4.5.d plots the small signal electro-optic transfer function of the device. The 3 dB small signal bandwidth is about 18 GHz, which is sufficient for the target data rate.

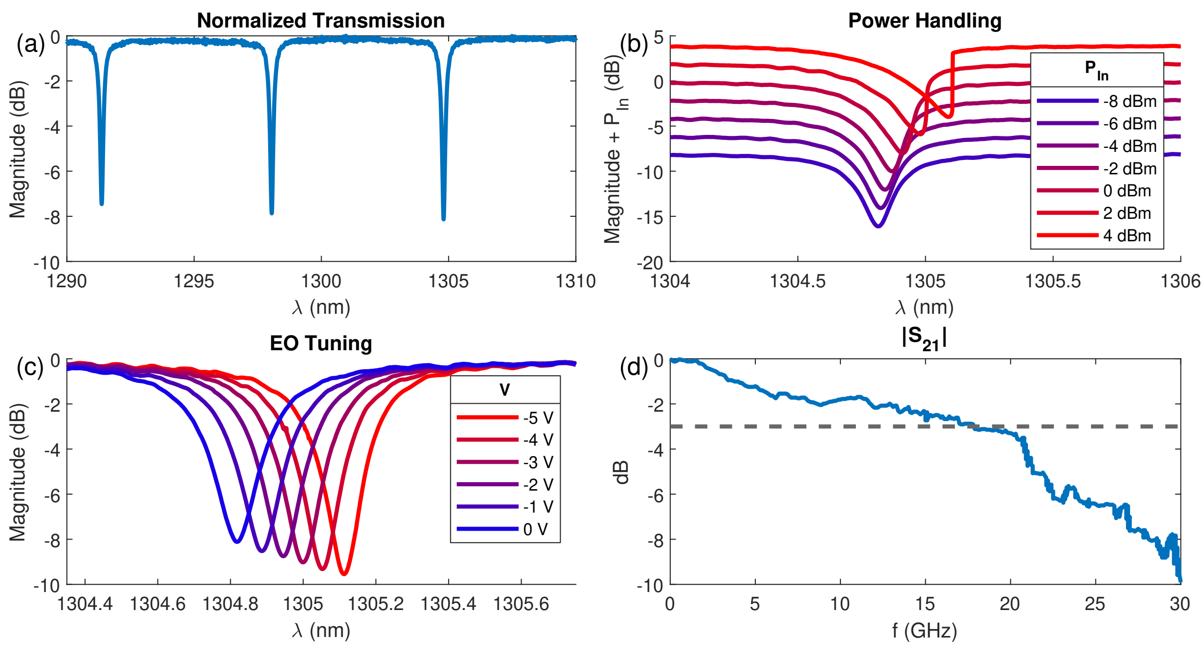

Figure 4.5: Transmission spectrum of a ring modulator (a). Transmission spectrum as input power to ring is increased (b). Transmission as integrated phase shifter is reverse biased (c). Measured electro-optic S_{21} magnitude with the carrier +32 GHz detuned from resonance (d).

The measured magnitude of frequency tuning for this modulator device is roughly twice that of the simulated device of the previous chapter while also hitting similar electro-optic bandwidth and finesse values. As can be seen in Figure 4.5.b, this device is does not experience as significant of degradation in tuning efficiency as reverse bias increases compared to the simulated device of the previous chapter. This inidicates that a different phase shifter cross section must have been utilized than was simulated in the previous chapter; since this phase shifter was fabricated in the same foundry process as the one used as the basis for device simulation in the previous chapter, it remains unclear whether this enhancement in performance is due to a better use of the established MPW process steps or is due to modifications of the process allowed by running a custom wafer; these are details not shared with the author due to being the intellectual property of a private company.

The drop port spectrum of the ring modulator is also important for characterizing the expected level of input power to the drop port for ring alignment purposes and for determining the amount of unwanted power dropped from the other channels across the device. Figure 4.6 suggests that as much as 32 percent of the power dropped on resonance could also be dropped from another channel; this crosstalk is much worse considering that the carrier of the target channel is not aligned to the resonance for a ring amplitude modulator. However, when measuring the spectrum inside the cavity from the free carrier absorption induced photocurrent inside the phase shifter, the ripples that are seen in the drop response that are killing the extinction ratio are not present. Since it would be expected that the ripples would be seen in the circulating spectrum if higher order modes were being coupled to the cavity, it might be possible there is another explanation for the measured spectrum. For example, the device under test and the input lensed fiber were not significantly laterally offset, so the ripples in the drop photocurrent response could be from light that wasn't coupled to the edge coupler scattering around the chip.

These rings are designed as a series with varied optical path lengths to introduce a passive fabricated channel separation between neighboring resonances [5]. This is seen in Figure 4.7.a where the resonance location of different ring channels is plotted and one

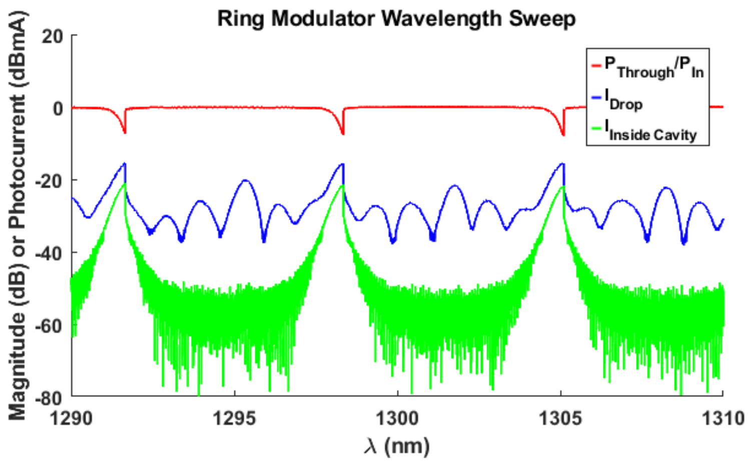

Figure 4.6: Measured through, drop, and circulating inside cavity spectrum of a ring modulator with high input power.

line is a single reticle. While the absolute resonance wavelength of a particular design varies between reticles as waveguide dimensions fluctuate across the wafer, the majority of the lines follow a monotonic trend with the expected spacing. Given the original resonance location of the ring, a high number of reticles support the tuning of all rings to their correct location even without the ability to tune a full FSR. This is shown in Figure 4.7.b where all reticles on half a 300 mm wafer can support the operation of at least 8 out of the 10 rings on the odd-deinterleaved bus at a fixed temperature without the need for integrated heaters that would consume more power, and half of all reticles can support operation on all 10 channels. State of the art substrate undercut ring modulators are currently budgeting 336 fJ/bit for TX modulator DC tuning for both fabrication errors and thermal drifts [6]; this excludes dynamic power consumption due to modulation [7] and the static power consumption of rings on the RX side of the PIC. This EO DC tuning result was performed with a p-n junction with a capacitance of 50 fF that will be driven with a high speed waveform with 1.2 V_{PP}, leading to fabrication errors being compensated for with no static power consumption and an estimated 18 fJ/bit of dynamic power consumption in the ideal case. However, to use EO tuning to also handle temperature drifts would require roughly tripling the FCPDE magnitude (which would in turn increase the capacitance of the ring modulator) and introducing a barrel shifter channel addressing circuit [8, 9, 10]. The implementation of a trimming mechanism would allow for only needing to double the tuning strength because only temperature drifts would need to be handled dynamically [11]. Factoring that an EO tuned RX ring consumes little dynamic power, it is apparent that realizing rings that do not require static thermal tuning has the potential to save hundreds of fJ/bit in a link budget even with the increased capacitance and dynamic power consumption that is introduced.

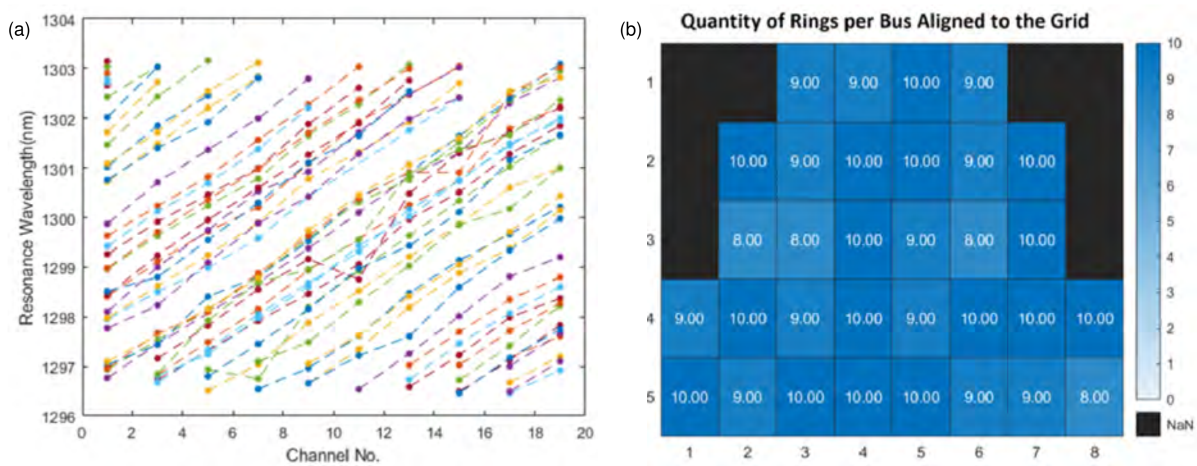

Figure 4.7: Resonance location of different ring channels (a). One line is a single reticle, showing strong correlation between different channels. Number of rings that can be tuned to the correct channel on each reticle (b). The maximum value is 10. *Data courtesy of Analog Photonics.*

Figure 4.8.a shows the drop spectrum of a measured demux filter with 0 V applied bias to the integrated phase shifter. A full width at half maximum of approximately 99.4 GHz is observed. Additionally, the spectral response at the add port was measured, which allows for extracting a backscatter spectrum. This result is shown in Figure 4.8.b and suggests crosstalk magnitudes lower than -40 dB near resonance peaks [12]. It is possible this low backscatter could allow for two parallel datastreams with identical wavelength allocations to be demultiplexed by the same ring with minimal crosstalk in the two

counterpropagating directions of the cavity; this would permit halving the number of RX rings needed in the PIC, reducing complexity, footprint, and energy consumption.

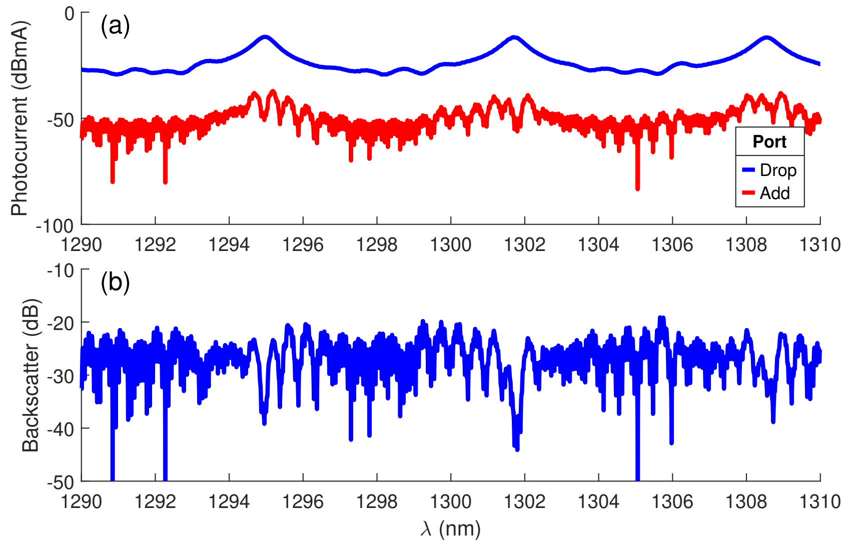

Figure 4.8: Measured spectral response of RX ring drop and add ports (a). Backscatter sprectrum estimate from the drop and add responses (b).

In a separate foundry silicon photonic MPW process, ring resonators with SISCAP-based integrated phase shifters were designed and fabricated; some measurements are featured in Figure 4.9. Much as was anticipated in the previous chapter, the amount of displaced charge is significant enough to undercouple the ring at higher forward biases. This ring is also capable of about double the frequency detuning of the measured ring modulator in this subsection with an integrated p-n junction phase shifter. The device breaks down shortly after an applied bias of +4.5 V. Internal process information suggests that performance could be enhanced by process optimizations, as this design was laid out in part of a new process. Part of these optimizations involve reducing the edge coupling loss to 3 dB per facet from the currently observed 14 dB per facet, which currently limits measurements on this chip to wavelength scan measurements in a cold cavity domain. Testing optimized devices is left as future work.

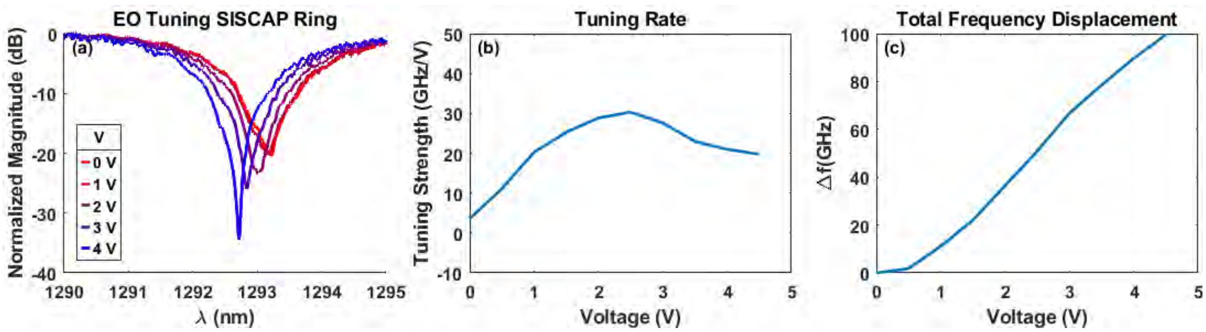

Figure 4.9: Measured spectral response a SISCAP ring resonator through response as it is forward biased (a). Instantaneous frequency detuning rate due to the FCPDE (b) and the cumulative frequency detuning (c).

4.2.2.4 Variable Optical Attenuator

The VOA is formed with a forward biased p-i-n junction in a silicon ridge waveguide; using a p-i-n junction instead of a p-n junction reduces excess optical loss in the "off" state. In order to attenuate the light (i.e. modulate the clock), it is slightly forward biased at a ∼200 MHz rate. Only a small amount of modulation is required, on the order of 1 dB, for the RX electronics to extract and divide the clock on each channel. Figure 4.10.a shows the measured IV curve and insertion loss (attenuation) of the VOA. Since it is a forward biased silicon diode, it has a turn on voltage of ∼0.7 V. There is a ∼0.3 dB excess loss at 0 V due to the optical mode interaction with the PIN junction. In order to achieve the required 1 dB modulation, the VOA needs to swing from 0 V to 0.8 V (V_{pp} = 0.8 V and V_{DC} = 0.4V). At 0.8 V, the VOA draws less than 1 mA.

Figure 4.10.b shows time domain measurements of the VOA output when a voltage input with 200 MHz sinusoid shape of 0 V to 0.8 V is applied. One can see the modulation on the optical output which enables the extraction of a clock later in the receive chain. Figure 4.10.c shows the measured EO bandwidth of the VOA is ∼125 MHz.

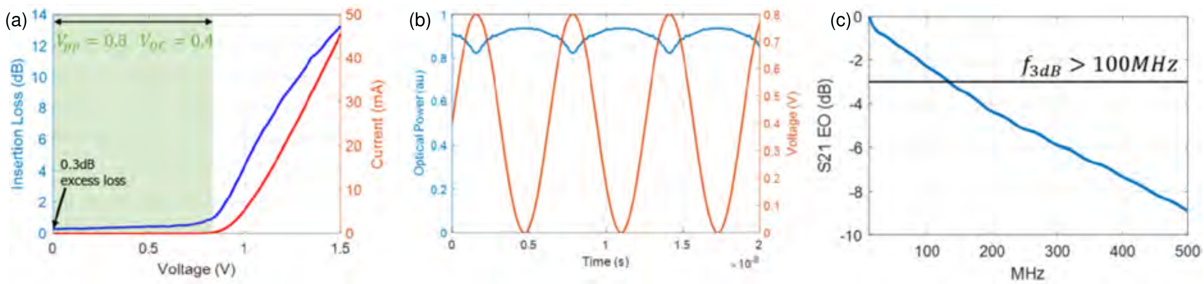

Figure 4.10: Measured IV curve and optical attenuation of the variable optical attenuator (a). Measurement of clock signal using the VOA from 0.0 V to 0.8 V (b). EO bandwidth measurement of the VOA (c). *Data courtesy of Analog Photonics.*

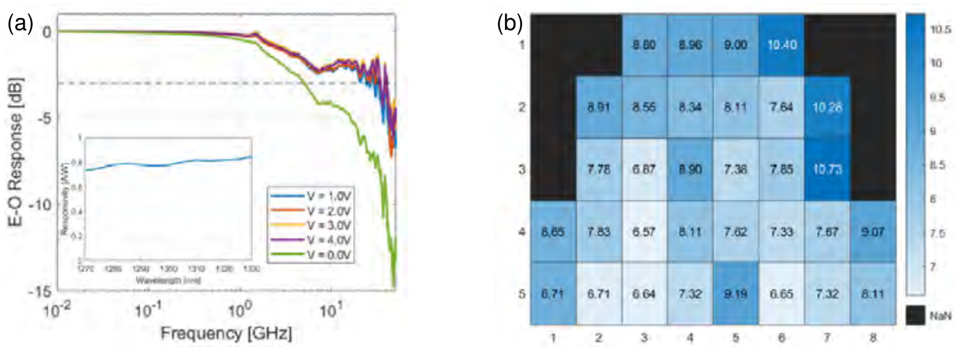

Figure 4.11: OE bandwidth measurement of the receiver photodetector. Inset shows responsivity (a). Wafer-scale measurement of receiver dark current at 1 V reverse bias in nA (b). *Data courtesy of Analog Photonics.*

4.2.2.5 Photodetector

The waveguide coupled, linear-mode vertical junction PIN photodetector used in the receiver is based off of epitaxially grown germanium on silicon [13]. Figure 4.11.a shows the measured responsivity and bandwidth of the photodiode. The bandwidth was measured as a function of reverse bias, and a bandwidth of ∼25 GHz is measured at 1 V reverse bias. A responsivity of 0.8 A/W is measured across the O-band. Figure 4.11.b shows the dark current of each PD on a reticle across the wafer at a 1 V reverse bias. The average dark current is ∼8 nA which is more than sufficient for low-noise receiver performance. To quantify this sufficiency, the sensitivity of the receiver to achieve a *BER* of 1E-9 ($Q \approx 6$) can be estimated with and without the dark current, and the two results can be compared. To simplify the expression, it will be assumed there is infinite extinction between the '0' and '1' levels and that there is no electrical or optical amplification, RIN, or timing jitter [14].

$$\overline{P}_{Rec} \approx \frac{Q\left(\sigma_s^2 + \sigma_T^2\right)^{\frac{1}{2}} + \sigma_T}{2\mathbf{R}} \tag{4.1.a}$$

$$\sigma_s^2 \approx 2q\left(2\mathbf{R}\overline{P}_{Rec} + I_d\right)\frac{B}{2} \tag{4.1.b}$$

$$\sigma_T^2 \approx \frac{4k_B T}{R_L}\frac{B}{2} \tag{4.1.c}$$

In the above equations, $\overline{P}_{Rec}$ is the receiver sensitivity power, Q is the signal to noise ratio (SNR), σ_s is the shot noise, σ_T is the thermal noise, $\mathbf{R}$ is the receiver responsivity, I_d is the dark current, B is the symbol rate, k_B is the Boltzmann constant, and R_L is the load resistance of the receiver. For p-i-n receivers, the link is typically thermally noise limited [14], meaning the shot noise contribution to the error rate is negligible. Further, looking ahead to Figure 4.15.b, it can be seen that the photocurrent of the '1' level is expected to be at least 3 orders of magnitude greater than the dark current; this means that the dark current is not expected to be a major contribution to shot noise even if the link was not thermal noise limited. Under thermal noise limits, the sensitivity is expected to be -24.9 dBm at room temperature, 27 GBaud, and a load resistance of 1220 Ω.

4.2.3 Electronics

The electronics design consists of two electronic ICs (EICs): the driver (Figure 4.12 and controller (Figure 4.13). Each chip is produced in 65 nm CMOS.

The TX on the driver EIC uses on chip PRBS sources to generate the data traffic, and the RX side of the driver converts the input PD current into a digital signal. There are two PLL blocks for TX and RX, on-chip LDOs, and 10 TX and RX blocks. The overall operation is controlled by serial peripheral interface (SPI) scan chain.

Each TX block consists of 4 serializers, a pattern generation block, and an injection-locked 8 phase oscillator. It drives 4 channels and generates various patterns including PRBS signal ($2^{31}-1$). The main phase locked loops (PLL) generates a 3GHz clock signal and it applies an injection signal to the replica oscillator for injection locking. From the injection locked replica oscillator, 8 phase clocks serialize the PRBS data and generate a 26.4 Gbps data stream for the EO driver. The driver has a V_{DD} of 1.2 V which will be the peak to peak voltage used to drive the modulator. The bandwidth of the drive signal is expected

Each RX block consists of 4 transimpedance amplifiers (TIAs), 4 deserializers, an error check block and an injection-locked 8 phase oscillator. It receives the data and checks the number of errors. The photodiode converts the received optical waveform into electrical current. In the RX block, the TIA receives this current input and generates a 26.4 Gbps data stream. To deserialize this data stream, it is passed through an 8-phase injection-locked oscillator; the reference clock of the PLL on the TX side is sent as an amplitude modulated wave, recovered and used as a reference for the RX PLL to enable deserialization of the data. Utilizing the output from this process, the pseudo-random bit sequence is employed to check for the number of errors within the received data.

The drift of the ring modulator resonance wavelength is corrected using the control EIC. The resonance frequency of each channel in the PIC is determined by the DC bias voltage applied to the ring's integrated phase shifter; this, in turn, affects the magnitude of current measured by the monitor photodiode on each ring's drop port for a fixed laser power and emission wavelength. Consequently, by accurately tracking the photodiode current, the optimal bias voltage for efficient operation can be determined. The DC bias

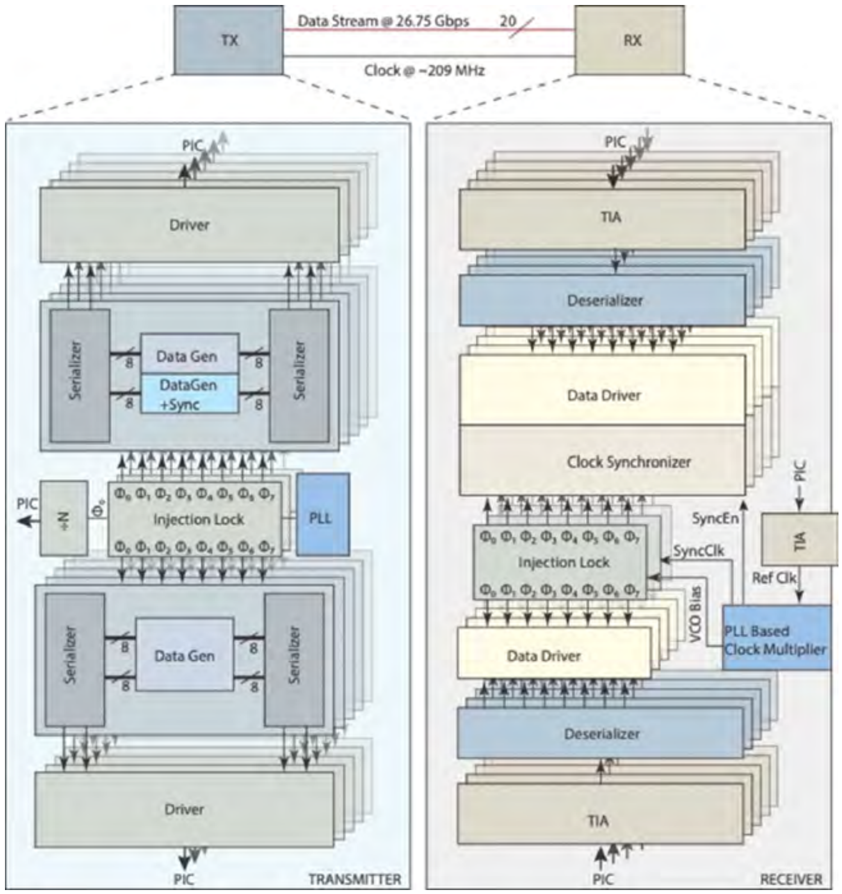

Figure 4.12: Overall Architecture of the driver IC. *Image courtesy of Luke Theogarajan.*

output is capable of reverse biasing each ring 0-6 V. The control IC chip features on chip regulators to reduce power supply noise, PLLs, 40 channel controllers and a SPI interface to control the operation using an external FPGA/microcontroller.

Fig. 4.13.a shows the schematic of a unit cell with PLL and low-dropout (LDO) regulator. Each controller has a 12-bit current sensing ADC, red/blue locking digital loop filter and high voltage EO driver.

Fig. 4.13.b shows the schematic of the photocurrent sensing ADC. The system comprises an analog front end designed to get current input, a loop filter, a voltage-controlled oscillator (VCO), and a switched capacitor-based resistor. The switched capacitor-based resistor's effective resistance is determined by the VCO's frequency. With the help of

a feedback loop in the control IC, the VCO frequency is dynamically adjusted to align with the input current, thereby achieving a balance between the input and resistor currents. The frequency is solely influenced by the input current through feedback operation, while a course/fine frequency counter converts this frequency into a digital code with a resolution of 12 bits.

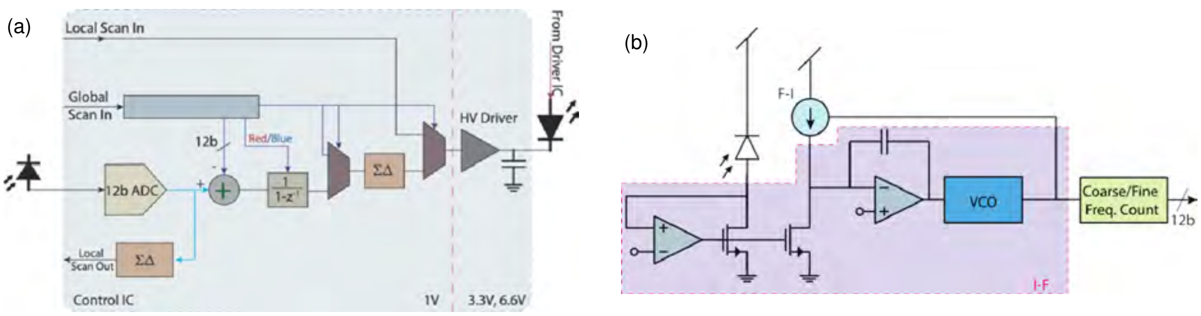

Figure 4.13: The schematic of Control IC chip (a). Schematic of the photo current sensing ADC (b). *Image courtesy of Luke Theogarajan.*

To drive a single PIC, two control chips and one driver chip are required. Each control chip drives the rings of the TX and RX channel, respectively, while the driver chip operates all 40 channels of data transmission in the PIC. Performance of the control chip is described in Section 4.3.1. Figure 4.14 shows microscope images and dimensions of singular copies of both the control and driver IC. The control IC has 248 pads that are placed around the perimeter of the chip in a wire bonding configuration, and the driver IC has 264 pads at a 36 micron flip chip pitch; 200 pads are used for driving TX-side ring modulators with the RF waveform and receiving the RX-side photocurrent waveform, and the remaining 64 pads around the outside of the pad field are for functions such as supply voltages, ground, SPI chain, and daisy chains for continuity validation. The signals in the driver IC is mirrored relative to the PIC such that proper netlist continuity is achieved to the PIC when it is flip chip bonded in the package.

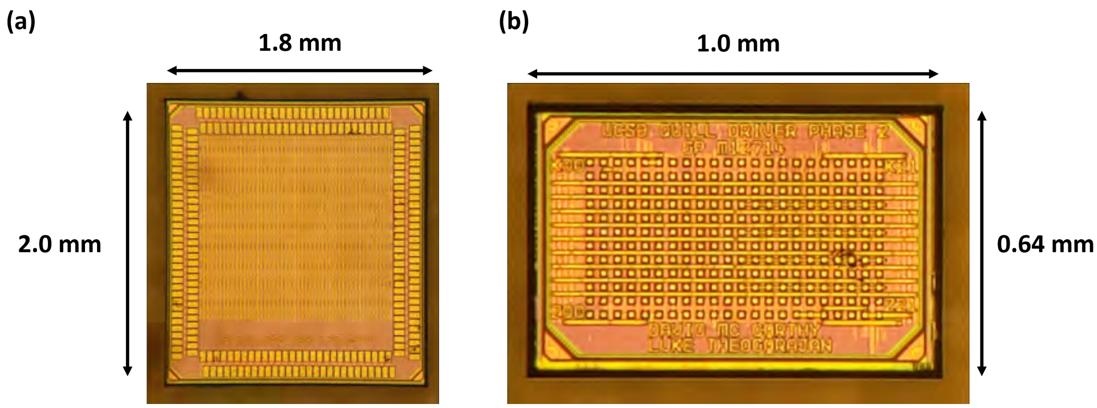

Figure 4.14: Micrographs of the control (a) and driver (b) ICs.

4.2.4 Forward Error Correction

FEC is a powerful technique that allows communication channels to get closer to the limit established by the theory of communication over a noisy channel. For short reach links, FEC would be considered feasible and beneficial to implement if it consumes less electrical power than an equivalent increase in optical signal power, if FEC encoding and decoding fit within system latency budget specification, and if the FEC circuit fit within the area of the driver IC.

Referring to Equation(4.2), the signal to noise ratio (SNR) is proportional to power squared and inversely proportional bandwidth. When thermal noise dominates, as is the case in nearly all practical communication links without optical amplification, this equation reduces to:

$$SNR = \frac{R_i P_s^2 \rho^2}{4 k_b T F_n B} \tag{4.2}$$

A $\sqrt{10} = 3.16x$ increase in power produces 10x increase in capacity. In general, short thermally limited links are best operated as fast as possible, within the bandwidth limits of available electro-optic components and available laser power. Parallelizing is not helpful as for example, 10 x10G links are 3.16x less efficient than a single 100G link. Further, since these are typically single-span links, the received signal power P_s is inversely proportional to link loss, L: $SNR \approx \frac{1}{BL}^2$. Net electrical coding gain ($NECG$), which is the SNR reduction allowed by introducing FEC, is proportional to:

$$NECG_{dB} \approx B_{dB} + 2L_{dB} \tag{4.3}$$

Thus, $NECG$ can be spent on data rate increase or on link budget but in different proportions. For example, a FEC code with NECGdB = 6 dB can be used to expand data rate bandwidth by 6 dB for an optical-power limited channel, i.e., a factor of 4x. However, the same code can only extend link loss by 3 dB.

$$\begin{aligned} NECG_{dB} =& 20log_{10}(\mathrm{erfc}^{-1}(BER_{ref}))- \\ & 20\log_{10}(\mathrm{erfc}^{-1}(BER_{in})) + 10\log_{10}(R_C) \end{aligned} \tag{4.4}$$

Practical optical links may deviate from the idealized computation presented above. Specifically, channel distortions induced by imperfect electro-optic components, finite crosstalk, etc. frequently make FEC more helpful than this computation suggests, i.e., FEC allows to clean up error floors or flaring that a simple increase in optical power is unable to overcome. For example, Figure 4.15.a shows a typical BER curve for a highly optimized laboratory instrument built using discrete components and operating as a single channel, single polarization and without optical filtering – note 2.2 dB penalty from BER 10^{-5} and 10^{-12} [15]. In contrast, highly parallelized optical systems are susceptible to bandwidth narrowing from EO components and optical filtering, to linear cross-talk between neighbors, polarizations, modes, etc. Such links have exhibited optical power penalty in excess of 18 dB at 10^{-12} BER, and 10 dB at 10^{-5} BER with 16 Gbps/λ, shown

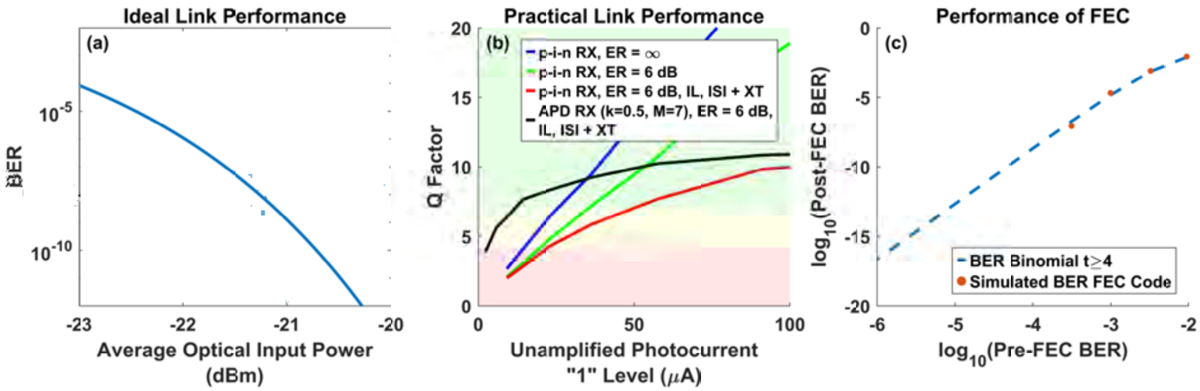

Figure 4.15: Single channel, discrete component 10G link performance (a). Simulated link performance comparison of idealized (Blue) and realistic (Red) optical links (b); the yellow region is where the BCH(511, 484) FEC code can be used to correct for all errors. Simulated FEC performance with simple algebraic decoder compared with binomial approximation (c).

in Figure 2.d of [16].

This effect can also be shown in link performance simulations, when various bandwidth and cross-talk effects are properly accounted for, shown in Figure 4.15.b. FEC performance gain on an idealized link is indeed fairly small (2.4 dB less input optical power needed for target BER), while a realistic optical link benefits from FEC more significantly (3.5 dB). FEC provides even more performance gain for an APD receiver (6.0 dB), and the APD requires 8.9 less dB input optical power than the p-i-n receiver at the FEC threshold.

We constrain ourselves to a maximum latency (excluding time of flight) of 50 ns, and we target FEC $NECG \approx 4dB$ at corrected $BER_{ref} \approx 10^{-12}$, which indicates a pre-corrected $BER_{in} \approx 10^{-5}$. Preliminary estimates of optical link QD SOA marginal power efficiency is 0.06 pJ/bit at 2 dB optical gain (i.e. $\frac{NECG}{2}$). Therefore, FEC is likely to be beneficial if its power consumption is $<$ 0.06 pJ/bit.

A relatively simple BCH N=511, K=484 code with code rate $R_c \approx 0.947$ and $NECG \approx$ 4.25 dB was selected for this link. The code has been fully implemented in Matlab and

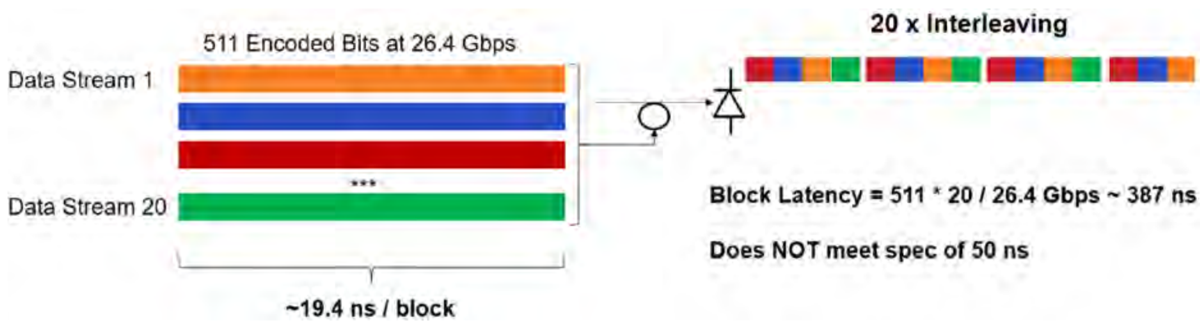

Figure 4.16: FEC latency with 20x interleaving of 511-bit blocks streamed through a single wavelength channel operating at 26.4 Gbps. *Courtesy of Mike Frankel.*

tested on various data and error sequences. This code is capable of completely correcting up to 3 errors per 511-bit block. If there are 4 or more errors per block, they are passed through without correction. Infrequent additions of 3 artificial errors are also possible when there are 4 or more real errors, but this effect is observed to have a negligible impact on performance, as shown in Figure 4.15.c.

In general, robust optical link operation in practical deployments mandates the use of FEC, which not only provides reduction in total system power consumption, but also provides link immunity against dribbling errors that may be induced by occasional control loop errors, RF channel reflections, cross-talk fluctuations, etc.

FEC encoding blocks require interleaving to provide tolerance against error bursts longer than 3 bits. However, care must be taken about how interleaving is implemented as it increases system memory depth and corresponding latency associated with FEC. FEC coding on a single wavelength tributary is not supportable due to the low latency requirements. Figure 4.16 shows a single wavelength operating at 26.4 Gbps and a 511-bit block occupying 19.4 ns. Interleaving 20 blocks increases FEC delay to 387 ns, which is considerably higher than the given latency constraint.

The system's 20 wavelengths are clock-synchronous and FEC blocks can be spread across all of these. In addition, robustness is increased further by adding 26-way time-

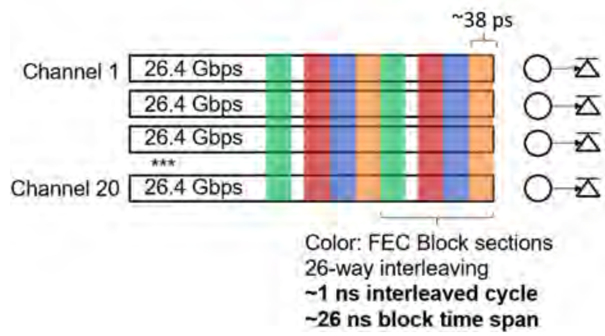

Figure 4.17: FEC latency with 20x interleaving across 20 wavelengths and 26-way time-domain interleaving of 511-bit blocks. *Courtesy of Mike Frankel.*

domain interleaving. This method is shown in Figure 4.17, and shows an interleaving latency of 26 ns.

Total FEC latency can be estimated assuming an implementation in TSMC 7 nm CMOS process. XOR gate count is 511 bits * 9 bits/syndrome * 3 syndromes = 13797 gates. FEC decoder delay involves computing third and fifth power, square root and cubic root of element in GF via 512 element look-up table (LUT). Further, addition via XOR of 9-bit sequences, product of two GF elements via LUTs, and division via 512 element LUTs are also performed. Thus, total decoder delay is due to encoder (2 ns), interleaving (26 ns) and decoder (5 ns) = 33 ns total, which is well within a latency specification of 50 ns.

This system has another specific benefit from FEC in regards to latency. EO ring tuning is restricted in range such that occasional channel switching is required over full temperature range ramp. At the same time, EO tuning can be quite fast, with tuning within 1 ns quite achievable; thermo-optic tuning, on the other hand, is orders of magnitude slower. This switching speed corresponds to 26.4 bits at 26.4 Gbps NRZ. With reasonable block interleaving, at most 1-2 errors per FEC block are expected, which are within FEC correction range. Thus, with careful channel switching algorithm design, error-free operation is expected.

In terms of consumed CMOS die area, a receiver area associated with the PIC is determined by the areal bandwidth density, which is in turn limited by the pad pitch. The system pad pitch in the high speed region of 36 μm leads to a footprint of 47000 μm^2 for a 500 Gbps RX composite. The area is largely dominated by XOR gates, and the area consumed can be estimated using published results as 0.22 μm^2 * 13797 XORs = 3000 μm^2, with some additional area for LUTs and some logic [17]. Therefore, FEC should be able to fit into the allocated area with area to spare, assuming an advanced 7 nm CMOS node.

Similar estimates of FEC power consumption indicate that $\approx$ 13 fJ/bit will be consumed by XOR operations, with some additional power for LUTs and some logic, which fits comfortably within the FEC-allocated 20 fJ/bit in the system power budget.

In summary, FEC should be considered mandatory for highly efficient and operationally resilient parallelized optical links. Simple FEC codes provide sufficient gain, mitigate the effect of many impairments, and can be realized in advanced CMOS nodes meeting specifications for energy efficiency, latency and areal density in short-reach applications.

4.2.5 Packaging of 3D Integrated Transceiver

Packaging unifies the separate electronic and photonic chips to operate together as a system and facilitates testing of a complicated system. Figure 4.18.a shows the cross section vision for a 1 Tbps unit. The PIC is flip chip bonded to an interposer containing an embedded driver IC, TSVs, backside redistribution layers (RDL) with a backside bonded contoller IC, all of which is soldered onto a daughter card PCB (shown in Figure 4.18.b); the daughter card form factor allows for edge card connection to a motherboard to produce aggregate transceiver systems with increased capacity. An aluminum nitride

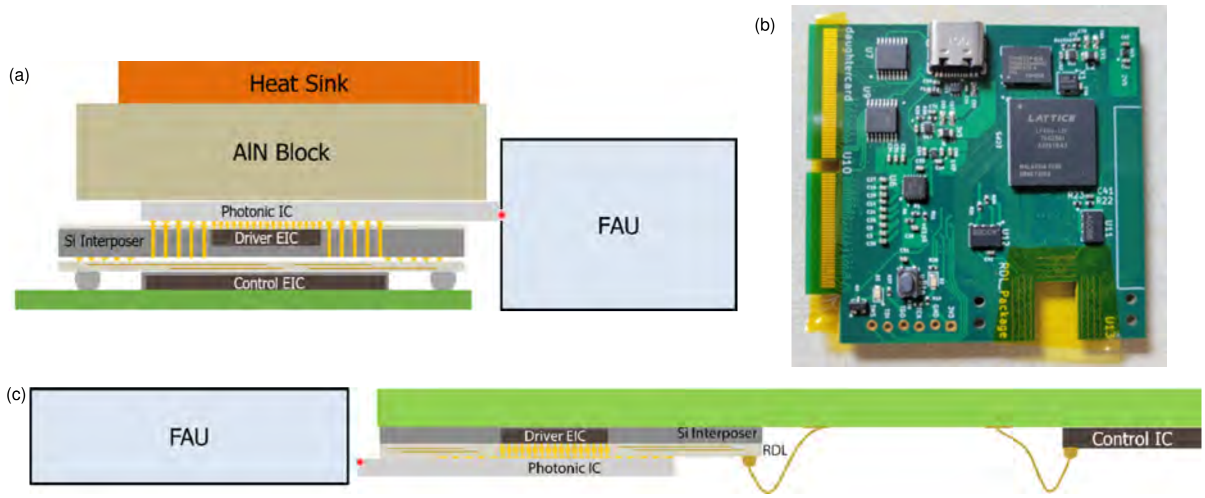

Figure 4.18: Cross section diagram for a 1 Tbps system (a). Daughter card printed circuit board for 1 Tbps system (b). Cross section diagram of simplified 25 Gbps system package (c).

block can be adhered onto the backside of the PIC to act both as a heat spreader and to increase the bond area for a fiber array, and a heat sink can attached to the other side of this block. Constructing such a package is a multidisciplinary effort that requires careful planning. Figure 4.19 shows a process flow from chip fabrication to completed package.

Since this packaging vision is quite intricate to realize, an intermediate package designed to validate the processing steps of the process is shown in Figure 4.18.c. This lower-complexity package still requires embedding the controller within an interposer with multiple RDL layers that has a PIC bonded to it; however, electrical continuity to the PCB is formed via wire bonds. Additionally, the controller IC is attached separately to the PCB and has its contacts wirebonded. A sacrifice made in this simpler package is system complexity; rather than running a full 1 Tbps link, this package could only output a single 25 Gbps channel of the system when operational. Details on some of the processing steps to form the package (TSV formation, Ohmic contacts to TSVs, multi-level RDL, interposer socket etch, driver IC embedding in to the interposer socket) can be found in [18].

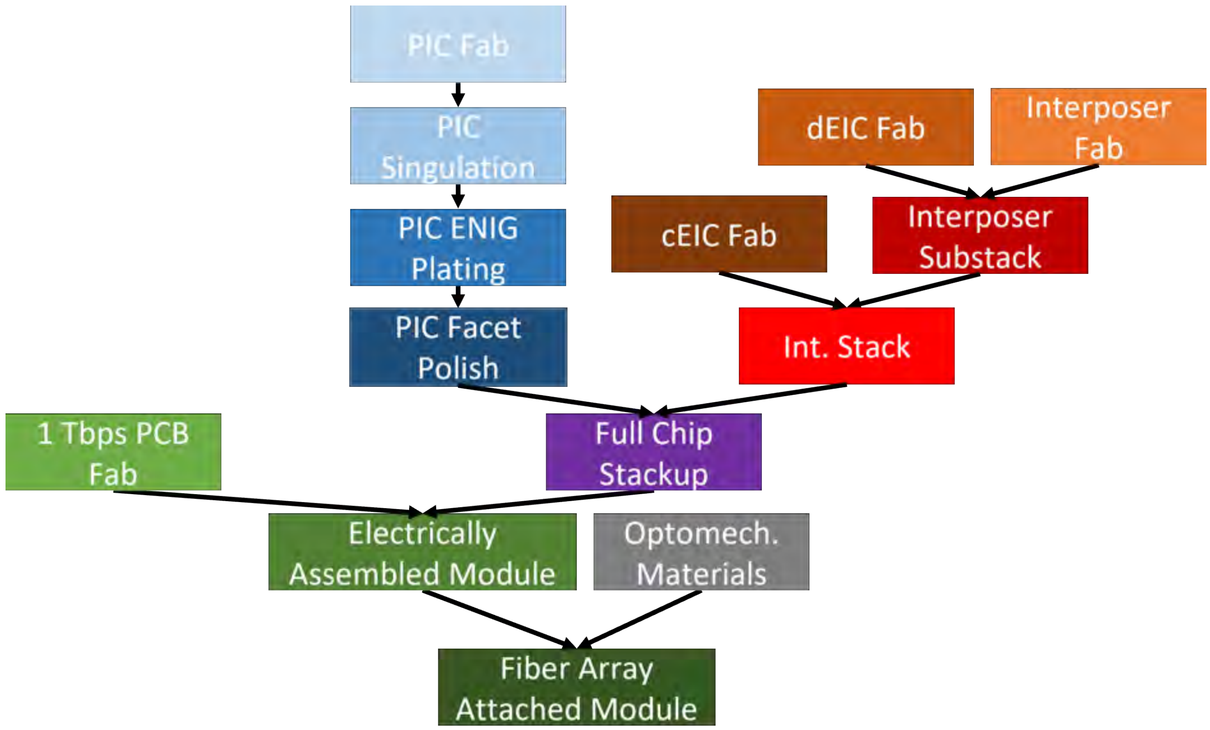

Figure 4.19: Flow chart for assembling a packaged transceiver system.

After the interposer is assembled with an embedded driver, indium is deposited onto its bond pads and those of the embedded driver IC in preparation for flip chip bonding of the PIC onto the interposer; the PICs have a pad pitch of 36 μm in the RF region that bonds to the driver IC and 72 μm for connections to TSVs on the full-complexity interposer. Prior to flip chip bonding, the PIC undergoes several post-processing steps in preparation. The silicon photonics wafer leaves the foundry unsingulated with bare aluminum pads that need to be gold plated for the flip chip bonding procedure. Wafer-scale electroplating was performed on the silicon photonics wafer after it had been cored to 150 mm. Laser stealth dicing was used to singulate the die over saw dicing to ensure a cleaner pad surface and minimize impact on chip-to-chip bonding; pad quality post-singulation is shown in Figure 4.20.a. PICs are then facet polished to remove a ledge on the optical interface that would otherwise prevent a standard fiber array from being aligned and attached to the package; the overpolishing is limited to at most 5 microns, which should only perturb the edge coupler performance to a small degree. Figure 4.20.b demonstrates the cleanliness of the facet after polishing. The interposer and PIC are then aligned on the stage of the flip chip and bonded, and one such completed single channel package is shown in Figure 4.20.c.

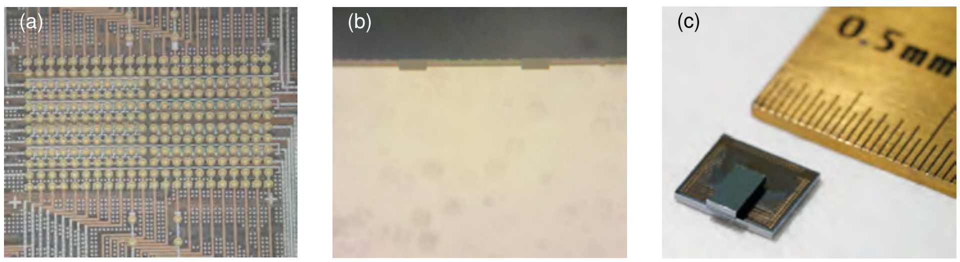

Figure 4.20: PIC pads that bond to the driver IC after plating and singulation (a). PIC optical facet for fiber coupling after facet polishing (b). An assembled 25 Gbps package (c).

That interposer package is then attached to a printed circuit board (PCB). The 25 Gbps demonstration is then wire bonded to the PCB, and the results are shown in Figure 4.21.a & b. After assembly, the unit can be mounted into its test station, as shown in Figure 4.21.c-e; the fiber array can then be aligned to package using overhead and side view cameras along with two red lasers and a six axis stage (Figure 4.21.f & g). Unfortunately, no optical modulation was observed in this first package when looking at its optical output and the power supplies turned on. The only clue as to what might have gone wrong was that a rather large current draw was observed when the power supplies to the PCB were turned on, suggesting shorts somewhere in the system; it is suspected this may be occurring in the RDL.

For the 1 Tbps packages, a fiber array can be directly epoxied to the PIC after it the interposer has been attached to a PCB; additional fixtures are included to preserve the integrity of the fiber attach process. An example of a successful fiber attach, along with the additional optomechanical and thermal hardware, is shown in Figure 4.22.a.

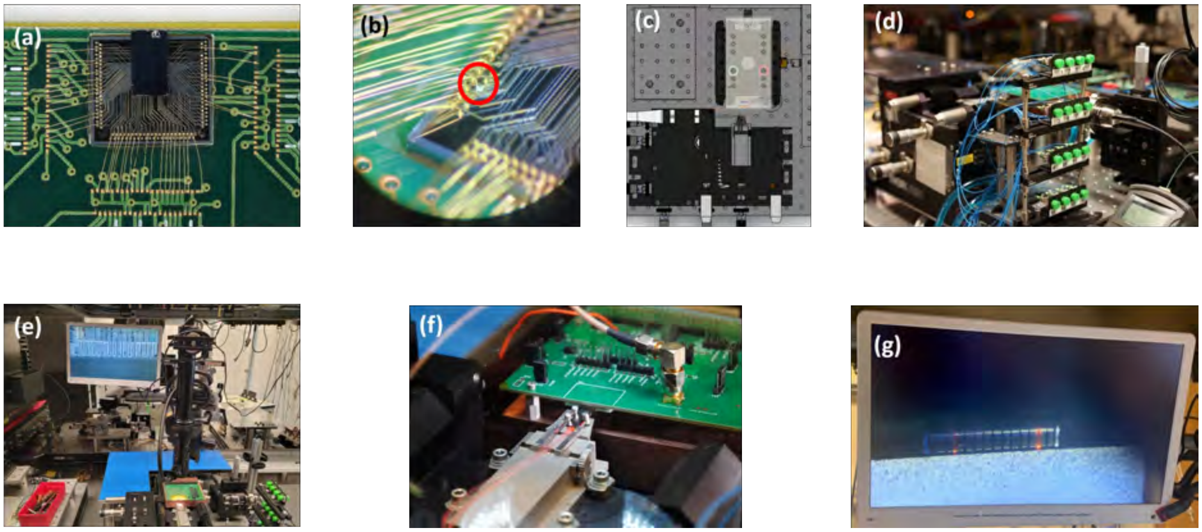

Figure 4.21: 25 Gbps demo package after wire bonding (a). Fixing wire bond failures with careful application of silver epoxy (b). SolidWorks model of the packaged demonstrator test station (c). Side view (d) and front view (e) of test station. Top-down view (f) and overhead microscope view (g) of 25 Gbps demonstrator mounted to test station and fiber array aligned.

One such packaged device was placed into an oven and underwent wavelength scans from temperatures ranging between 20-80° C, and the results are shown in Figure 4.22.b. The data shows that the insertion loss is stable across wavelength and temperatures ranges of interest. With a loss of about 4.2 dB in the optical pathway consisting of two edge couplers with 1 dB per facet loss and 8.1 mm of integrated silicon photonics waveguides, the quality of the facet polishing and fiber attach are confirmed. The small ripples in the transmission spectrum are assumed to be due to minor polarization fluctuations occurring during the scan, as the fibers in the fiber array attach test were SMF-28 rather than PM fibers. The optical pathway on the PIC includes bends that would filter out any TM light that may be present at any moment.

While much of the work on the package is promising, there are still minor issues that exist in the first generation that require addressing before full system tests can be conducted. Namely, improvements are needed in eliminating shorts present in the RDL and for increasing the flip chip bond yield between the PIC and the driver EIC (as seen in Figure 4.23). The 25 Gbps package also requires optimization to improve wire bond yield.

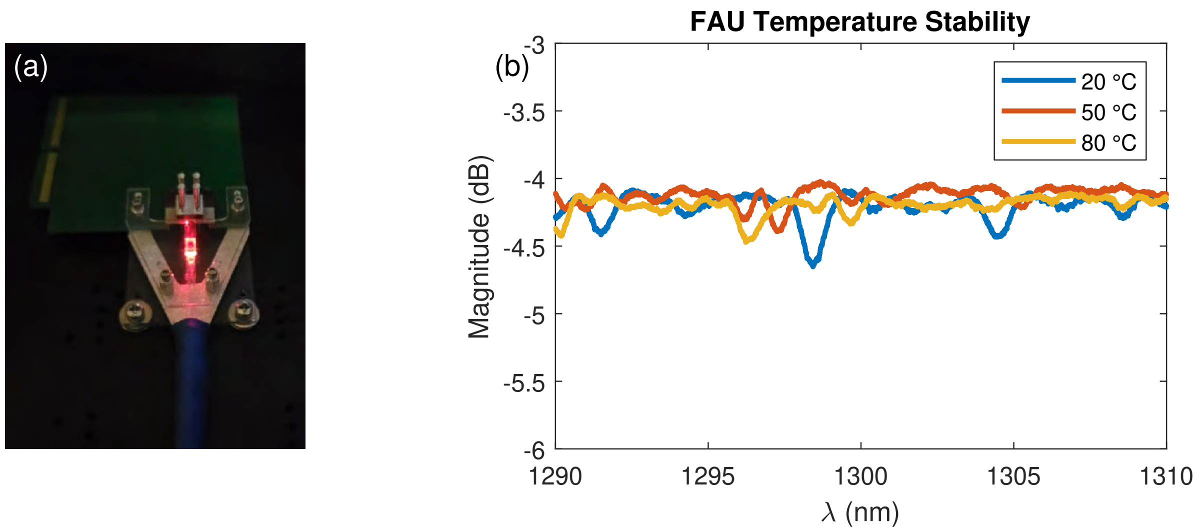

Figure 4.22: FAU attach hardware secured to a daughter card (a). Insertion loss through FAU and PIC alignment loopback across wavelength and temperature (b).

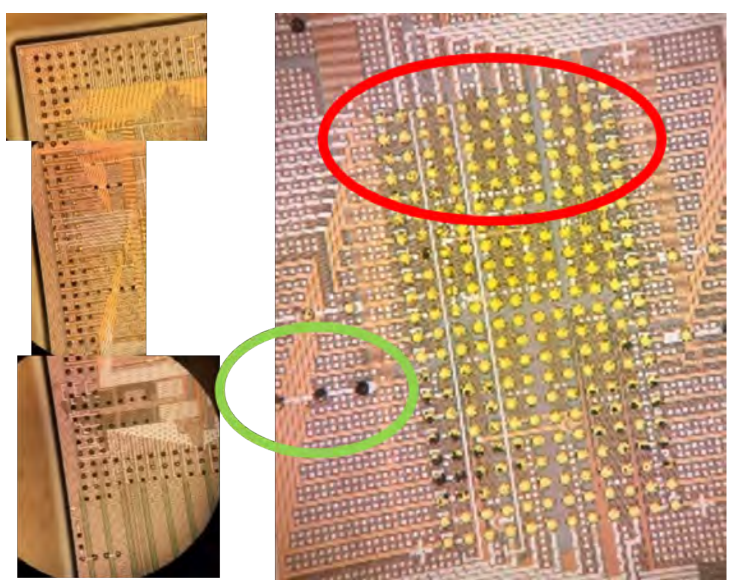

Figure 4.23: Micrographs of the flip chip bond pads of a PIC after it had detached from an interposer. Gold-colored pads (like those in the red oval) indicate regions of unsuccessful bonding, while darkened pads (like those in the green oval) indicate remaining indium on the chip surface and successful bonding.

4.3 Subsystem Testing

There were two main experiments conducted of electronic-photonic systems. The first is a demonstration of a controller IC evaluation board successfully interacting with a silicon photonic ring modulator chip, and the second details our efforts in co-packaging the photonics and electronics for a fundamental validation of all sub-components functioning in a single-wavelength 27 Gbps optical link.

4.3.1 Ring Locking

Figure 4.24.a show a ring modulator chip that is optically and electrically probed in a manner allowing for light to be passed in and out of the PIC with the capability of applying an EO bias to the phase shifter and to read the monitor photocurrent on the drop port of the ring. These electrical inputs are connected to a PCB with a packaged control IC, shown in Figure 4.24.b. Figure 4.24.c shows that the resonance wavelength shifted according to the EO driver voltage generated by the control IC.

The next objective after verifying that the controller can shift the ring resonance with an applied voltage is to verify the controller can convert the monitor photocurrent into an appropriate ADC value and see a semblance of a ring lineshape. This is successfully shown in Figure 4.24.d, in which a tunable laser wavelength is set to be on the red side of the resonance at a controller drive voltage of 0 V; as the drive voltage increases, the ring resonance is red shifted, which causes an initial increase in the ADC value as monitor photocurrent reaches its maximum when the laser is now aligned with the ring resonance. Further increases to the driver voltage past this point lead to a decay in the photocurrent as the laser is further redshifted away from the ring resonance.

Finally, locking the ring is done by instructing the controller to achieve an input photocurrent ADC value on either the red or blue side of the resonance. For a full 1

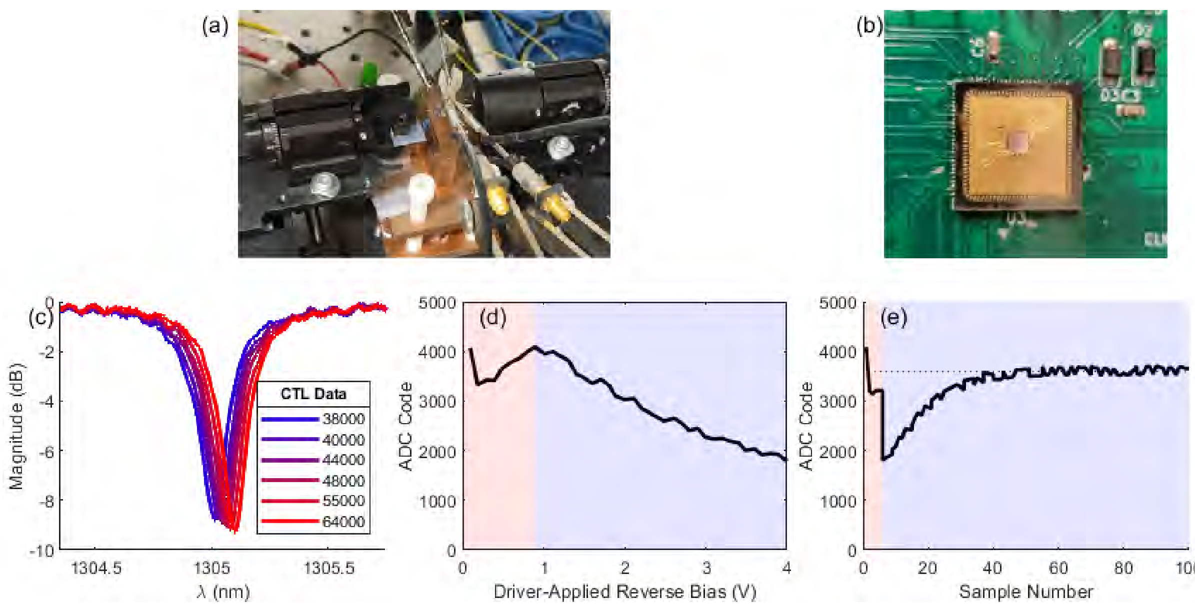

Figure 4.24: Ring modulator fiber coupled and DC needle probed on its p-n junction phase shifter and its monitor photodiode (a). The packaged control IC chip (b). Ring frequency response shifting according to the applied bias voltage change from the control IC (c). Scanning a ring modulator resonance by stepping the EO phase shifter bias and reading its monitor photocurrent both with the contol IC (d). Locking a laser that begins on the red side of a ring resonance to a photocurrent ADC value of 3600 (dotted line) on the blue side of the resonance (e). Blue and red regions in (d) and (e) indicate whether the laser is on the blue or red side of the ring's resonance, respectively. While not recorded in this measurement, the time step between samples is expected to be about 100 ms in (e), but that is not known with enough certainty to warrant a time domain conversion of the x axis; locking begins at sample 0.

Tbps system, it is required that all ring modulators will lock to the same side of the ring resonance, preferably on the blue side of the resonance [4]. However, it is likely that some rings will have their MLL channel start on the red side of the resonance. Figure 4.24.e demonstrates that the locking circuit is capable of identifying that it is on the red side of the resonance from the amplitude derivative and switches to the highest possible reverse bias output to get on the blue side of the resonance. While there is some fluctuation in the read ADC value even after locking after about 50 samples, it is not necessarily a sign of trouble with the circuitry because the sample rate was incredibly slow in this proof of concept experiment (on the order of 10 Hz); these ripples in the ADC value could be onset from vibrations of the input lensed fiber on this time scale. Unfortunately, these control IC demo boards proved to be fragile, and all were damaged beyond use before further investigation could be undertaken. To that end, no practical experiments to estimate power consumption were undertaken.

4.3.2 Discrete 1-λ Link with QD-MLL Source

Figure 4.25 shows the experimental setup diagram and results for a single-channel modulation experiment. One line of a packaged QD-MLL has data encoded onto it with an integrated ring modulator driven by an arbitrary waveform generator (AWG) producing a 27 Gbps NRZ signal. This driving signal has a $V_{PP} = 1$ V and is pre-emphasized to compensate for cable losses. The optical signal is amplified with a commercial QD-SOA, and a tunable optical filter is then used to remove the unmodulated comb lines; the modulated line is coupled into a PD that has a low-noise amplifier (LNA) on its backend that is connected to an oscilloscope for analysis. The achieved bit error rate (BER) in the preliminary experiment of 2.9E-5 is close to the system's FEC threshold of 1.3E-5; however, the simplified TX photonic element used in the experiment lacks a deinterleaver. The

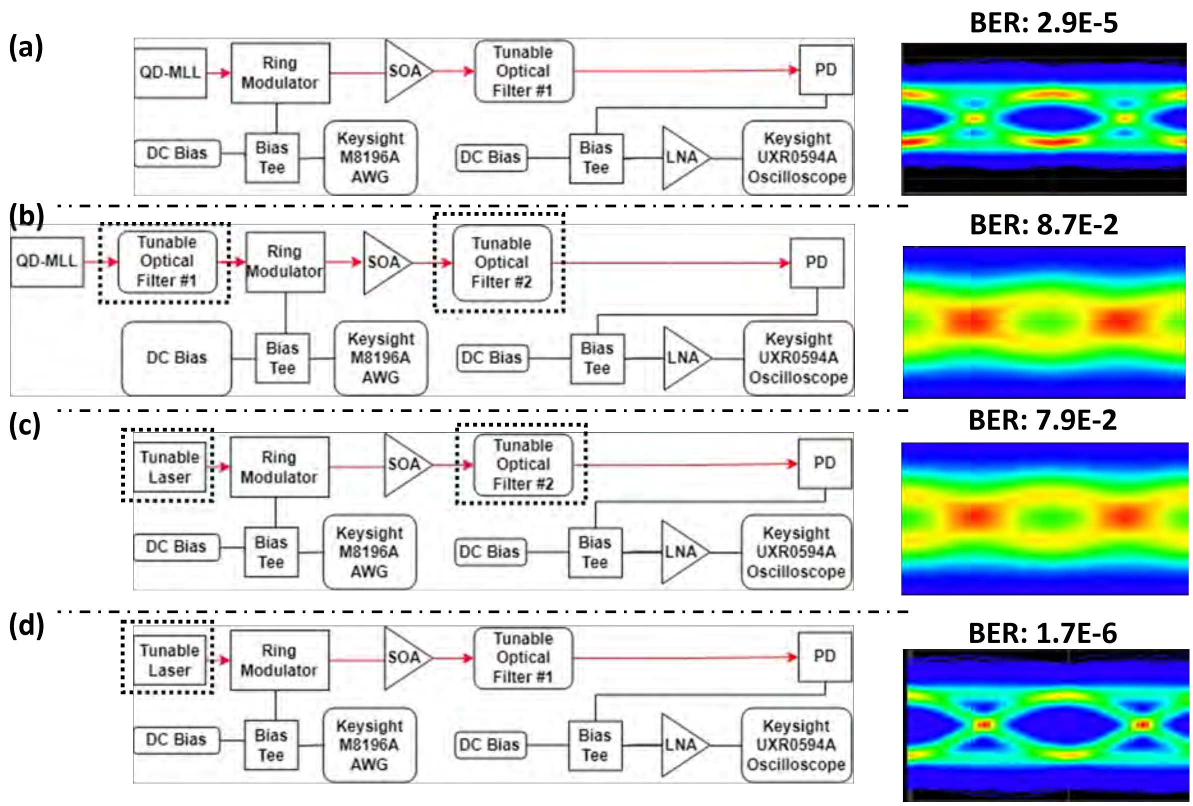

Figure 4.25: Link experiments and resultant eye diagrams. Elements enclosed within a dashed box in (b), (c), and (d) indicate variations from the original experimental setup in (a).

absence of a deinterleaver increases the number of comb lines that couple power into the modulator, and the excess input power from the additional comb lines causes self-heating of the ring and degrades signal integrity. To prevent self-heating, a second iteration of the experiment is conducted in which the QD-MLL is filtered down to a single carrier before passing into the MRM (Figure 4.25.b). This iteration experiences a much worse BER, but this is likely due to the extra loss insertion loss introduced by the second filter; Tunable Optical Filter #1 has an insertion loss of 5 dB, and Tunable Optical Filter #2 has an insertion of 3.5 dB. There are also 3 PIC edge coupling operations (into and out of the TX along with into the RX via lensed fiber) that each have insertion losses of about 3 dB; the edge couplers in this experiment are not the same 1 dB per facet design as used in the system and instead prioritize compactness over losses. This hypothesis is confirmed by substituting the QD-MLL with a commercial tunable laser with the same wavelength and power conditions, which achieves a similar *BER* (Figure 4.25.c); this tunable laser carrier is capable of a *BER* almost an order of magnitude smaller than the FEC threshold with an incident power on the ring modulator of about 1 dBm (Figure 4.25.d). The single-channel link experiment conducted here introduces 6 dB more loss than the fully-integrated WDM demo. Therefore, an appropriately deinterleaved QD-MLL comb source with -5 dBm per line is expected to be sufficient for a 1 Tbps link.

4.4 Results and Discussion

While a fully copackaged link has not been shown, it is still expected that the constituent components are likely viable once capable of being brought together. Some of the figures of merit of concern for this link are power consumption and areal bandwidth density.

Figure 4.26 projects the energy consumption of a 1 Tbps link based upon the MLL and

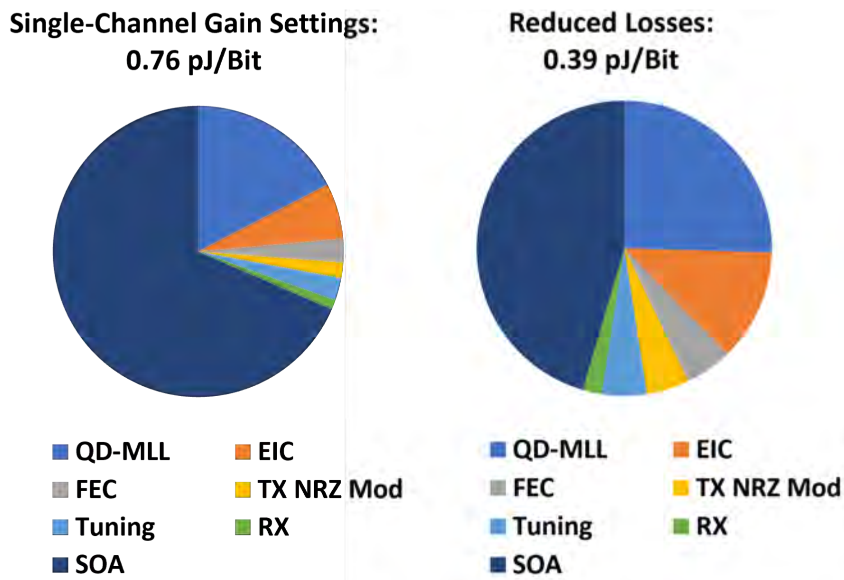

Figure 4.26: Energy budget extrapolations for a 1 Tbps system utilizing a QD-SOA.

SOA conditions used in the single-wavelength demo as 0.76 pJ/bit. This will be broken down for the experimental conditions in Figure 4.25.a, which was argued in the previous section would close the link had a deinterleaver been present. In this circumstance, the QD-MLL gain section consumed 257.1 mW (I_{Gain} = 150 mA and V_{Gain} = 1.71 V) and its saturable absorber consumed 8.04 mW (I_{SA} = 6.7 mA and V_{SA} = −1.2 V); since the QD-MLL would be used to supply carriers for 2 Tbps of capacity when deployed, its energy per bit is halved relative to the rest of the components in a 1 Tbps system. The QD-MLL was stabilized at a temperature of 42 °C, and the power consumption of this is not factored into the result as it is expected that this value can be less than 100 fJ/bit with better package design. The QD-SOA consumes 520 mW of power (I_{SOA} = 400 mA and V_{SOA} = 1.3 V).

However, if the losses in this experiment matched those expected for the copackaged 1 Tbps link, the energy consumption of the link is expected to reduce to 0.39 pJ/bit due to needing less optical amplification; while every other loss in the system can be found throughout the Silcon Photonics subsection and accounted for by following the path in the demonstration figure in the introduction chapter, the excess loss of the (de)-interleaver is about 0.12 dB. There is also expected to be about 0.9 dB of loss due to waveguide propagation thoughout the PIC. Beyond lower losses than were achieved in the single wavelength demonstration, a 1 Tbps link would likely experience a higher signal to noise ratio due to the benefits of a flip chip bonded driver chip instead of RF probing, lower input power into the ring modulators, and ring stabilization circuitry; this may further reduce power consumption expectations in a full system demonstration.

While there are many approaches that could be leveraged to further drive down power consumption, Figure 4.26 indicates one of the most substantive ways to do so would be to reduce the amount of optical amplification needed to close the link. One such approach to do so would be to replace the optical gain of QD-SOAs with the electrical gain of integrated avalanche photodiode (APD) receivers; APDs with a gain-bandwidth product of at least 200 GHz would enable removing the QD-SOAs for this application [19]. APDs provide a substantial link loss gain (8 dB) for only marginal increase in bias circuit power consumption. Since this method of gain amplifies each channel individually, it may lead to improved signal integrity by avoiding inter-channel crosstalk mechanisms QD-SOAs can introduce like cross gain modulation [20]. Additionally, use of APDs could reduce the amount of power needed to be tapped to monitor photodiodes and the optical clock; since both of these circuits operate at much slower speeds than the data rate, it is possible that they could be biased at a higher gain point since lower bandwidths are needed. Without an APD, marginally better performance could likely be expected from using a praseodymium-doped fiber amplifier as an alternative to a QD-SOA [21]; the downside is that such a form of optical amplification is not in the spirit of a short-reach interconnect as it cannot currently be introduced into a PIC in an integrated form (whereas QD-SOAs can be integrated) [22].

In the driver IC bond region of the PIC, the contiguous area that the 1 Tbps worth of ring modulators and RX demux filters and PDs occupy is about 0.19 mm^2. This leads to the local area bandwidth density in the RF region is 5.3 Tbps/mm^2; local bandwidth density is currently the commonly reported figure of merit [23].

Despite the high local bandwidth density, the overall PIC footprint has an area 28.6 times larger than the RF region; this disparity can be driven down by iterating on the PIC footprint allocation. The PIC discussed in this work is limited by metal routing and flip chip pitch, which could be addressed with pitch reductions and introducing additional metal routing layers [24]. However, the photonic footprint allocation could also be reduced. For example, a simple change to the architecture would be to perform the TX deinterleave operation before power splitting. Deinterleavers are much bigger than power splitters, and they can also require phase shift correction; this therefore also can reduce the number of pads, corresponding drive circuitry, and energy per bit. Integrating the MLL and gain sections to distribute one comb source over many more 500G unit cells would mean needing only 1 deinterleaver on the TX side per MLL, but this may not be the best overall choice for link performance and energy efficiency [25, 26, 27].

4.5 Conclusion

The approach taken by this system appears to be a promising path towards highly energy efficient and compact optical interconnects that could be leveraged in the on-board and in-package length scales. However, much more work remains in building a practical demonstration in order to truly verify its viability.

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Chapter 5

Lithographic Overlay Error Estimation

5.1 Introduction

In order to be commercially viable, the production of complex photonic integrated circuits, such as the one of focus in this dissertation, requires all of its constituent integrated photonic elements to have reliable, state-of-the-art performance within a reticle, across a wafer, and between lots. Many of these components are formed through several separate processing steps, like the ion implantation of a shallow-etched silicon waveguide to form a FCPDE phase shifter or multi-level waveguide tapers for edge coupling and polarization rotation. In reality, the lithographic alignment between the layers that form these more complicated structures is not perfect, and this will introduce a probability distribution function (pdf) of the degree of error in how each layer overlays one another. This overlay error distribution imparts tolerances on the device performance (e.g., ring modulator loss, resonant wavelength, resistance, capacitance, tuning efficiency, power handling, etc.) and ultimately imparts a pdf on the critical system parameters (bit error rate, energy per bit). Optimizing a system design is therefore both about optimizing the expected value and shrinking the standard deviation of the critical figures of merit, and doing so requires knowledge of the variability of each dimension (of which there are many dimensions) and the ability to efficiently compute their effect on device and system performance [1]. At many times, designers are combating these tolerances to make the best designs, but they are without any knowledge to the extent each variable is impacting them. This must be remedied.

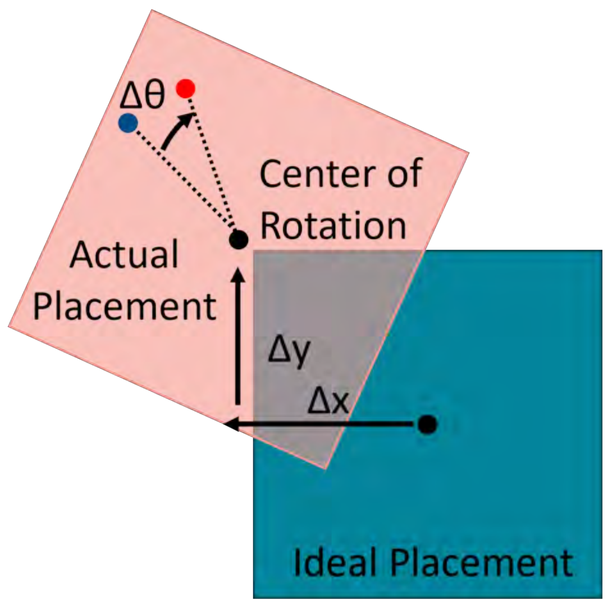

Figure 5.1: Schematic of overlay error affecting the placement of a mask

The amount of overlay error, much like tolerances in waveguide dimensions, is a critical parameter that a foundry may or may not disclose; foundry nondisclosure would require a designer to develop methods to deduce these errors from measurements taken of a chip or destructively cross-sectioning a chip to observe these errors themselves. Within a foundry, overlay metrology can be performed with techniques such as bright field imaging or electron microscopy [2, 3], and there are many contributing factors to the degree of overlay experienced [4, 5, 6]. Process nodes with finer resolution also require tighter control on overlay errors [7]. Unlike waveguide dimension tolerances [8], developing experiments that allow for extracting overlay error from photonic integrated circuits nondestructively has not been explored with rigor. This chapter focuses on experimental designs which one may use to estimate the degree of overlay error. A primary focus will be the overlay error between ion implantation layers and a silicon waveguide, but methods for observing overlay error between different waveguide material layers and waveguide etch layers will be discussed. Though there are 3 dimensions in which overlay error can occur (2 translational and 1 rotational, as in Figure 5.1), the translational overlay error estimation will be the primary focus of this chapter, but extracting rotational errors will be briefly discussed as well. Some basic geometric rules will be outlined for understanding the impact overlay error can have on ring resonators with integrated depletion p-n junction phase shifters.

5.2 Ion Implantation Overlay Error Estimation

Simple measurements in both the electrical and optical domain were developed to attempt the extraction of overlay error between an ion implantation layer and its implanted waveguide layer.

5.2.1 Electrical Method

A common technique that can be used to estimate the dopant concentrations of a p-n junction is to measure its capacitance-voltage curves in the reverse bias regime [9]. In the parallel plate approximation of a p-n junction, $\frac{\partial\left(\frac{C}{A}\right)^{-2}}{\partial V} = -\frac{q}{2}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)$ regardless of any intrinsic gap between the n and p regions and regardless of the reverse bias magnitude, allowing for easy extraction of the dopant concentrations. However, when the parallel plate approximation is invalid (such as with a thin diode formed in a silicon photonics waveguide) the significant fringing capacitance term makes the measured $\frac{\partial\left(\frac{C}{A}\right)^{-2}}{\partial V}$ dependent both on the intrinsic gap and the reverse bias voltage. This was verified experimentally by measuring the C-V curves of a series of p-n junction diodes of varying intrinsic region widths on the Tower PH18MA process. The diodes were also placed in two different orientations on the mask. As shown in Figure 5.2, $\frac{\partial\left(\frac{C}{A}\right)^{-2}}{\partial V}$ of each device was different and not a constant across the measurement range.

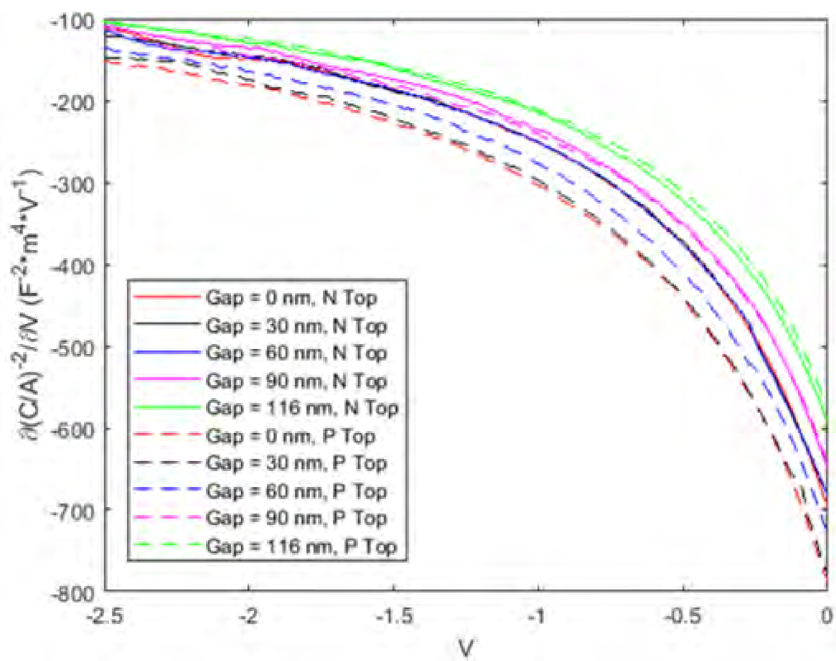

Figure 5.2: Plotting of the measured capacitance-voltage slope for a series of diodes intended to estimate lithographic overlay error.

There are several hurdles to overcome to translate this experimental result to implant-waveguide overlay error. Firstly, a highly accurate 2-D electrical model would be needed to translate this result into the true intrinsic gap between the p and n layers. Secondly, extracting the true intrinsic gap with the support of simulation would extract the overlay error between the p and n layers that formed the junction, not the overlay error between each implant layer and the waveguide layer.

An additional implication of this result is that attempting to extract carrier concentrations of ion implanted dopant layers in silicon photonics processes using the C-V method is fundamentally flawed and will yield inaccurate results.

5.2.2 Optical Method: Simplified

The principle of the test structure is as follows. Two identical silicon racetrack ring resonators are doped via ion implantation on opposite sides of their racetrack regions with equal distance between the implant geometry and the waveguide in the ideal case, as illustrated in Figure 5.3.a. However, if there is any vertical misalignment between the implant and waveguide layers during fabrication, the dopants on one ring structure will be brought closer to the waveguide and further away on the other ring. This in turn changes the round-trip optical loss of the two resonators, which will alter key aspects of each microring's spectral response such as its extinction ratio and full width at half maximum ($FWHM$) [10]. Plotting one of these characteristics of the microring response for a series of implant-waveguide separations should yield identical curves that are spatially offset from each other by double the amount of implant-waveguide misalignment.

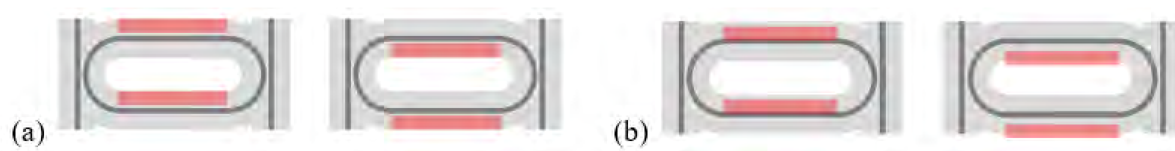

Figure 5.3: Schematic of racetrack resonator with red rectangles indicating ion-implanted regions. The case of ideal implant placement is shown in (a), while (b) shows implant region placement with a die-level vertical misalignment to the waveguide. The dark gray regions indicate full-thickness silicon, while the light gray regions denote partially etched silicon

A series of such ring resonator devices were fabricated on the Tower Semiconductor PH18MA silicon photonics process. Add-drop microrings were selected instead of all-pass devices to increase the number of ring structures that are nearly critically coupled. The ion implantation step used in this test is a high-concentration n-type dopant layer used for Ohmic contacts. All devices are oriented such that the racetrack region of the devices is parallel to the x-axis of the mask, so measured misalignment will be along the y-axis. The structures with implant windows placed below the waveguide have a varied mask-level waveguide separation spanning from 200 nm to 900 nm, and the structures with implant windows above the waveguide utilize implant-waveguide separation value ranging from 200 to 250 nm in 5 nm steps. For each device, the frequency response of the drop port was measured using a C-Band tunable laser source and photodetector; the $FWHM$ of the drop port for the ring resonance closest to 1555 nm is then extracted from these measurements, with the results shown in Figure 5.4.a.

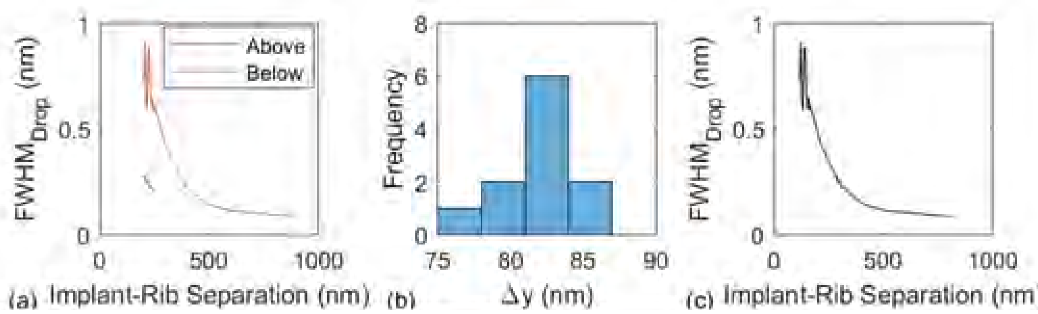

Figure 5.4: $FWHM$ of the drop response of a racetrack resonator as a function of mask-level (a) and corrected (c) separation between the nearest edges of the ion implantation region and rib waveguide. Histogram of all misalignment values extracted from fitting the implant window above the waveguide dataset to the implant below dataset (b).

It is clear from Figure 5.4.a that there is a significant offset between the two curves, suggesting there was indeed misalignment between the implant and the waveguide on this sample. The directionality of the misalignment can also be determined from this plot. Since the devices whose implant regions were placed above the waveguide have a narrower $FWHM$ at the same mask level separation compared to those devices implanted below the waveguide, the implanted regions above the waveguide must be further away than those below, and the misalignment must be in the $+y$ direction. To determine the magnitude of misalignment, the $FWHM$ data of the devices with implants placed above the waveguide are interpolated to fit the data for the implant below curve to get their effective separation if those points were in the implant below dataset, s_{interp}; the misalignment Δy can be found with the following expression:

$$\Delta y = \frac{s_{interp} - s_{mask}}{2} \tag{5.1}$$

where s_{mask} is the as-drawn separation between the implantation region and the rib waveguide. The result of performing this operation on all available data points is shown in Figure 5.4.b; the mean extracted misalignment value is +81.8 nm in the y-axis with a standard deviation of 2.3 nm. This mean misalignment value is used to correct the separation values of both the implant above and implant below datasets and consolidate them into one dataset, shown in Figure 5.4.c.

5.2.3 Optical Method: Refined

While the simplified optical method outlined in the previous subsection is promising, some of its assumptions may not be entirely valid. Primarily, the simplified approach assumed that the losses introduced from ion implantation would be equal for all orientations of ion implant windows; this is likely not true because ion implantation into silicon is typically done with a nonzero tilt angle to reduce channelling effects [11]. Figure 5.5.b shows that for the simulated implant conditions, the interpolation method of determining overlay error could introduce up to 20 nm of error; this is because the twist angle changes whether the ions are aiming towards or away from the core and to what extent, changing the distribution of dopants in the waveguide and the losses. Effectively, a more rigorous method would need to align two or more curves to one another by using a figure of merit that doesn't directly maximize the overlap between the two curves. Therefore, the interpolation approach utilized with the simplified method may not be the best curve matching technique to utilize, either.

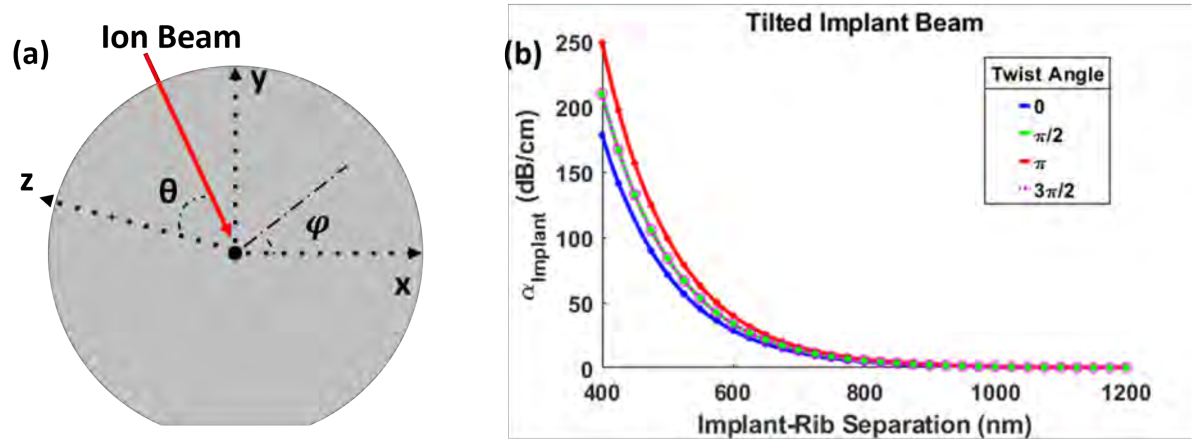

Figure 5.5: Illustration of a wafer implanted with a tilt angle θ and a twist angle φ (a). Plot of simulation results showing the affect on relative twist angle for an implant tilt angle of 7 degrees for a rib waveguide with a 220 nm rib height, a 110 nm slab thickness, a 400 nm-wide core, and $\lambda = 1550$ nm (b).

Secondly, the simplified approach ignores waveguide dimension fluctuations that could perturb $FWHM$ from the changing coupling coefficient this would induce. This can be removed by extracting the propagation loss and coupling coefficients from the resonance measurement. Waveguide dimensions affecting core confinement and losses from the ion implantation layer cannot be eliminated, but placing the series of rings in the experiment as close to each other as possible will mitigate this as much as is feasible.

In an attempt to solve the curve alignment problem, two approaches were developed. The first approach involves examining what happens to the waveguide losses as the implant step reaches past the core center. As shown in Figure 5.6.a, the overall loss function no longer appears exponential and instead has a sigmoid shape; the generalized logistic function fits well to it and other similarly low-concentration ion implant steps [12]. To estimate overlay error, the sigmoid shape is copied, flipped, and appended to make a rectangular pulse shape, as in Figure 5.6.b. The same is done to its counterpart loss curve from the data of the losses from the opposite orientation; the two pulses are

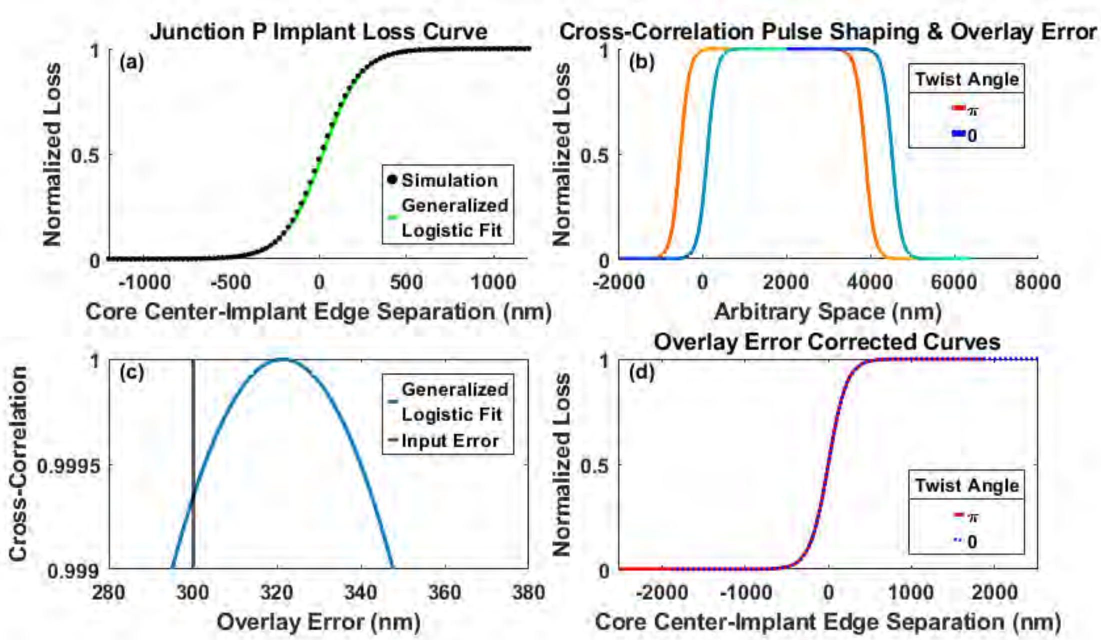

Figure 5.6: Simulation and fitting to the normalized losses of a p-type implant step for forming a p-n junction overlapping with the waveguide and an implant twist angle of π (a). Plot illustrating the formation of the rectangular pulses for cross-correlation alignment using the logistic function fits to data (b). The pulses line color is linearly interpolated to aid in showing how it is stitched together, and an overlay error of 300 nm is applied between the two pulses. Comparing the cross-correlation alignment technique between datasets with twist angles of 0 and π for the implant to the actual input error (c). Normalized simulated loss curves with the cross-correlation maximized overlay error translation applied (d); this is shown to be the incorrect translation value in (c).

cross-correlated, and it is assumed the curves will be aligned at the position with the maximum cross-correlation coefficient. Figure 5.6.c shows this method outputs a value of overlay error that is exactly 20 nm greater than the value applied to the simulated data and maximizes the overlap of the two curves instead of having the desired effect of correctly offsetting them (Figure 5.6.d). Larger tilt angles should separate the curves even more and introduce more error in the extracted overlay parameter, as would higher implant energies causing deeper penetration into the device layer.

Slightly different results are achieved on the opposite end of the spectrum for implant conditions: Ohmic contact doping steps. As can be seen in Figure 5.7.a & b, fitting and

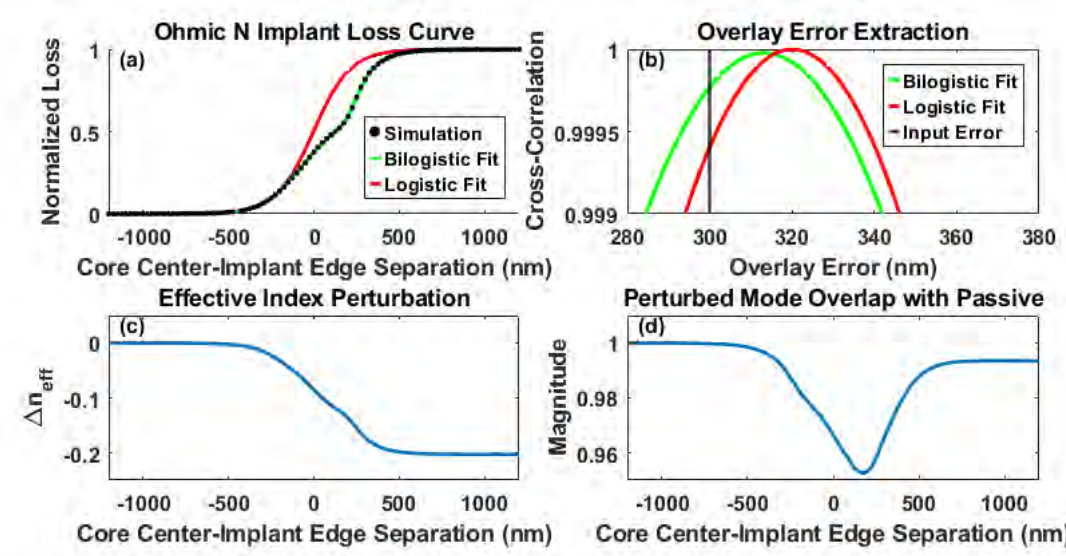

Figure 5.7: Simulation and fitting to the normalized losses of an Ohmic n-type implant step overlapping with the waveguide and an implant twist angle of π (a). Comparing the cross-correlation alignment technique between datasets with twist angles of 0 and π for the high concentration implant to the actual input error for the two attempted fitting methods (b). Simulation of the degree effective index is perturbed for the Ohmic contact implant (c). Simulation of mode overlap of the Ohmic contact implanted waveguide to an unperturbed waveguide (d).

cross-correlation alignment technique also has a bit of error in high concentration implant cases. It is suspected that some of its differences in results stem from the large dopant concentration strongly perturbing the mode, which distorts the loss curve to no longer appear like a logistic function; this can be seen in the simulation results of Figure 5.7.c & d. In order to remedy this, using a function that introduces a better fit to the loss curve, like the bilogistic function [13], was used. That does reduce the alignment error in the simulation by 35 percent, but that is still a 13 nm error (which may be enough precision for an Ohmic contact, depending on the application). Further, if the mode overlap and effective index perturbations are explored, strongly-doped waveguides will introduce a large reflection and high overlap losses in this experiment, introducing peak splitting and perturbing the measured round trip losses of a ring resonance. Therefore, another experimental approach for more precise analysis of overlay error in degenerately-doped semiconductor layers may be needed.

The second attempted approach for aligning dissimilar curves was inspired by observing a 2π-periodic nature with twist angle in Figure 5.5.b. This is confirmed by simulating losses for a fixed implant separation and sweeping the twist angle, and the results are shown in Figure 5.8.a. The plot shows that while similar to a sinusoid, it is not an exact fit. The act of measuring overlay error test structures oriented in the $\pm\hat{x}$ and $\pm\hat{y}$ orientations is to sample this sine-like function at $\frac{\pi}{2}$ intervals (referred to as points **A**,**B**,**C**, and **D** in this work) without knowledge of the offset twist angle at point **A**, φ_0; these 4 sampling points have a mean value μ. Instead of attempting to align curves from sampling position **A** to position **C** and position **B** to **D** (as what had been attempted previously), perhaps aligning to a ratio of these values and their mean could be of value. A selection of ratios that can be constructed from the 5 known data sets and would be relevant to a continuous periodic function (e.g., $|\mathbf{A}-\mathbf{D}| = S|\mathbf{C}-\mathbf{B}|$, where $S=1$ for all φ_0 in a perfect sinusoid) are plotted in Figure 5.8.b. The ratios that did not feature discontinuities were deemed the more practical choices.

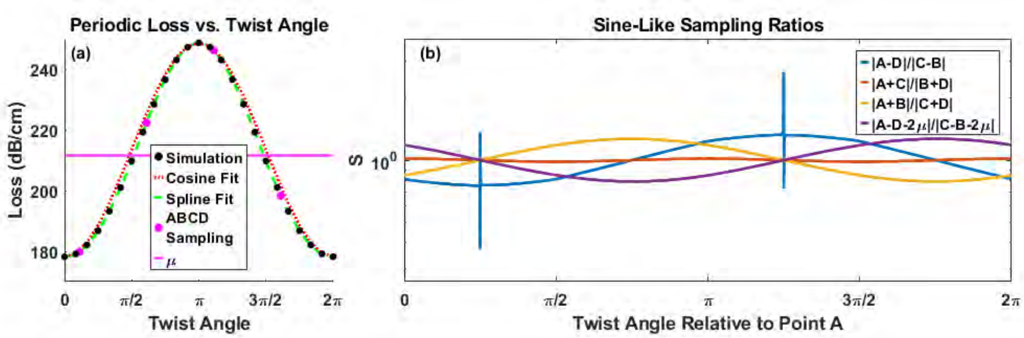

Figure 5.8: Simulation, fitting, and sampling losses of an aligned implant loss curves with a tilt angle of 7 degrees for a fixed offset between the implant layer and the waveguide core as a function of twist angle (a). Plotting various ratios that can be constructed for a sine-like function (b).

To perform the alignment with this technique, a 2-D sweep of offsetting the $\hat{x}$ curves (**A** and **C**) and the $\hat{y}$ curves (**B** and **D**), recomputing the μ curve, generating the ratio curves and comparing it to the input value of S with the R^2 coefficient of determination function to establish the best fit and associate it with an overlay error. The R^2 contours for the 3 ratios that did not have discontinuities in Figure 5.8.b are plotted in Figure 5.9.a-c for $S = 1$. What is observed from these contours is that there is infinitely many combinations of overlay error coordinate pairs that maximize R^2, which explains the difficulty in developing a method in aligning dissimilar curves. However, by multiplying together two of the contours to get a composite contour (shown in Figure 5.9.d), a single global maximum is achieved; unfortunately, that maximum occurs at the same incorrect location that the interpolation and cross correlation methods output. This is because of the choice of ratio scaling factor $S = 1$.

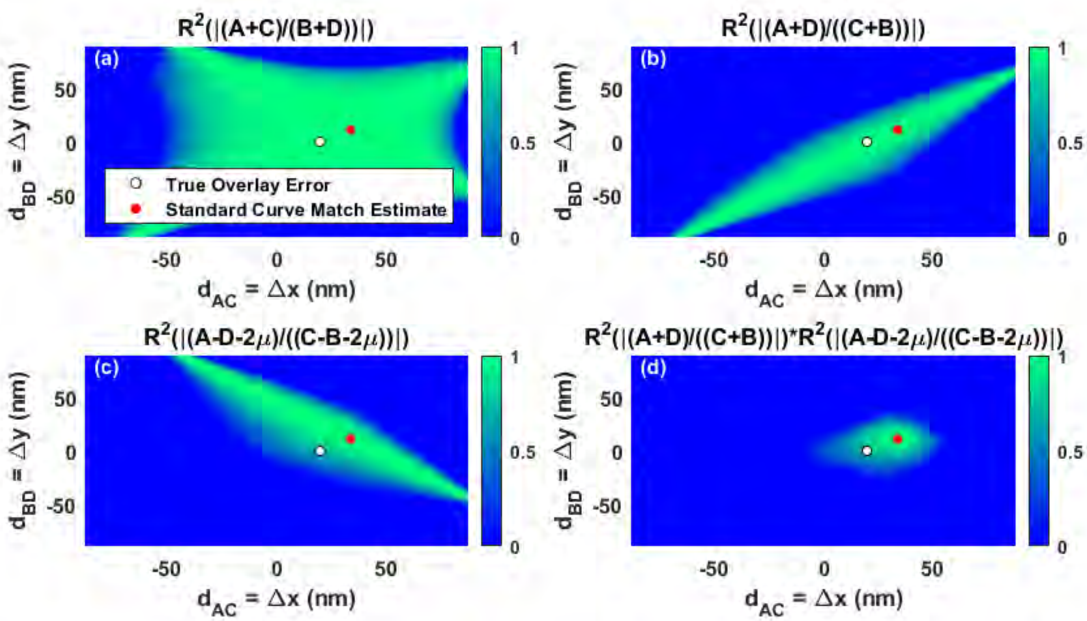

Figure 5.9: Plotting coefficient of determination contours while sweeping the alignment of the simulated loss curves for a variety of sine-like ratios and $S = 1$ (a-c). Plotting of a composite contour of (b) and (c) (d).

An example of how the scaling factors can be used to translate the composite contour is shown in Figure 5.10.a. This resembles a domain that has polar coordinates in the exponential with a rotational offset from the Cartesian grid that can be expressed in terms of coordinates (S_1, S_2).

$$S_1 = S^{\mathbf{r}cos\left(-\varphi+\frac{5\pi}{4}\right)} \tag{5.2.a}$$

$$S_2 = S^{-\mathbf{r}sin\left(-\varphi+\frac{5\pi}{4}\right)} \tag{5.2.b}$$

In the above equations, it is assumed $S^{\mathbf{r}} > 1$; the inclusion of the separate exponent term $\mathbf{r}$ is not strictly necessary but illustrates how the "radius" in polar coordinates can be adjusted. As shown in 5.10.b, the composite coefficient of determination contour maximum can be translated to the correct location with these scaling factor coordinates. Knowledge of the magnitude of error between the true overlay error and that measured from interpolation-style curve matching methods produces a circle around the coordinates of the interpolation style extracted overlay error point. Knowledge of φ_0 results in a ray of available options extending from the interpolation style extracted overlay error point at an angle of $\pi - \varphi_0$ relative to the x axis; the true overlay error coordinate is at the intersection of the ray and the circle.

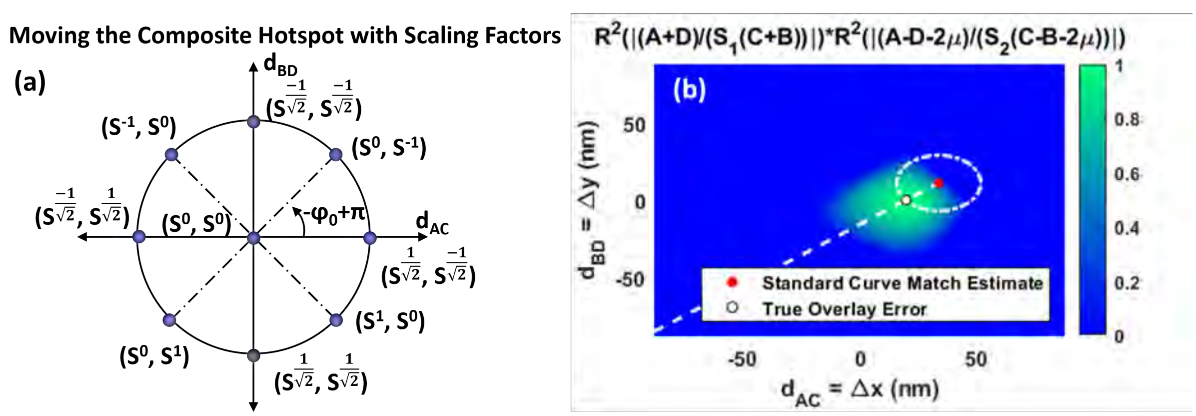

Figure 5.10: Illustration demonstrating how to translate the global maximum of the composite R^2 contour by adjusting the scaling factors of the constituent ratios that form the composite contour (a). Example of applying the scaling factors to translate the maximum of the contour to the location of true overlay error (b).

Ultimately, this approach was deemed unable to be used for curve alignment on its own, as it would require knowledge of what the scaling factors should be (which requires that the curves have already been aligned by another method). However, this technique does extract a useful parameter: the ion implantation twist angle $\varphi = \varphi_0$. Therefore, if the implant curves can be appropriately aligned by another method, this analysis shows the phase angle in overlay error space between the correct alignment and the incorrect "most similar" alignments is directly related to the implantation twist angle. This line of analysis also shows that the tilt angle of the aligned curves could be estimated by fitting a sinusoid to the 4 data points of the aligned curves at a particular point along the curves and comparing that to simulation results.

Overall, both new approaches appear to have failed to develop a robust method for extracting the overlay error when there is a tilt to the ion implantation step. However, if the tilt and twist angle remained uniform across a 300 mm wafer, determining the error in the distribution of results across a wafer with a statistically significant sample size could aid in applying a correction factor; one might expect that the true expected value of the distribution to be 0, for example. However, it seems possible that uniformity of both implant tilt and twist angle may not occur in practice (to preserve tilt angle uniformity across the wafer, the twist angle may need to be adjusted) [14]. This limits the options available for correctly extracting overlay errors when there is an additional confounding variable that is changing, and no definitive solution presents itself to the author at the moment on how to resolve the matter. Perhaps sampling at $\frac{\pi}{4}$ intervals instead of $\frac{\pi}{2}$ could help by having results that mix together Δx and Δy to add additional equations to the analysis, but that is not certain at the moment. Another approach could be to destructively analyze a single test site, which could allow for a wafer-scale correction factor to the measurements.

Frankly, the failure of the cross-correlation alignment technique was not realized until the writing of this thesis, so an experiment in which it would serve as the basis for aligning losses had been designed and partially measured. The remainder of this subsection will detail methods for extracting losses from those measured ring resonators.

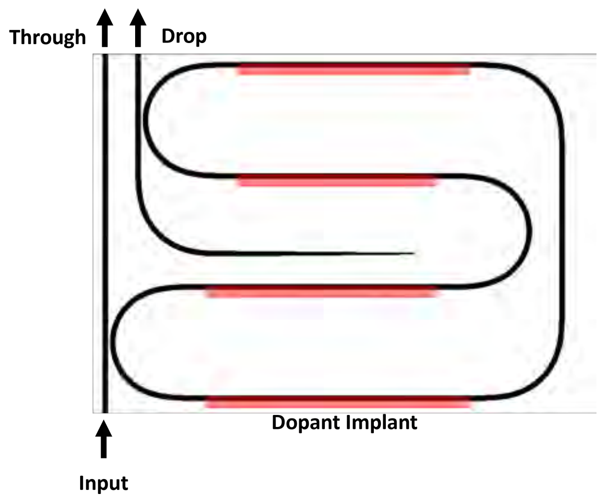

Figure 5.11: Sketch of the shape of the ring resonator geometry utilized to test the refined theory of overlay error extraction of an implant dopant layer in the $-\hat{y}$ orientation.

Figure 5.11 is a mask level drawing of a ring resonator laid out on a silicon photonics foundry process in a series of devices to extract overlay error in the $\hat{x}$ and $\hat{y}$ dimensions; this particular device is a part of the series for generating a loss curve for the $-\hat{y}$ orientation. The ring is bent around in a horseshoe-like shape so that the through and drop ports are closer together and oriented in the same direction, increasing the likelihood that the coupling coefficients the ports are the same (asserting $\sigma_1 = \sigma_2 = \sigma = \sqrt{1-\kappa^2}$ is a core part of the utilized loss extraction technique [15]). The dopant implant windows are stepped across rings from fully uncovered to entirely overlapping the waveguide in order to produce logistic function-like extracted loss curves. For the cases with little to no implant overlap with the waveguide, it is anticipated that the Q of those cavities will be high enough that backscatter-induced peak splitting is possible. Additionally, it is clear from Figure 5.11 that the drop port is is not placed at the halfway point of the physical length of the cavity, and the losses are also not evenly distributed throughout the cavity; therefore, $\psi_a \neq \frac{1}{2}$ for most conditions the ring will be in (whereas most models assume $\psi_a = \frac{1}{2}$). A thorough analysis technique would then consider how to adjust the loss fitting equations for this scenario and consider the degree of error introduced by using equations that assert $\psi_a = \frac{1}{2}$ anyway.

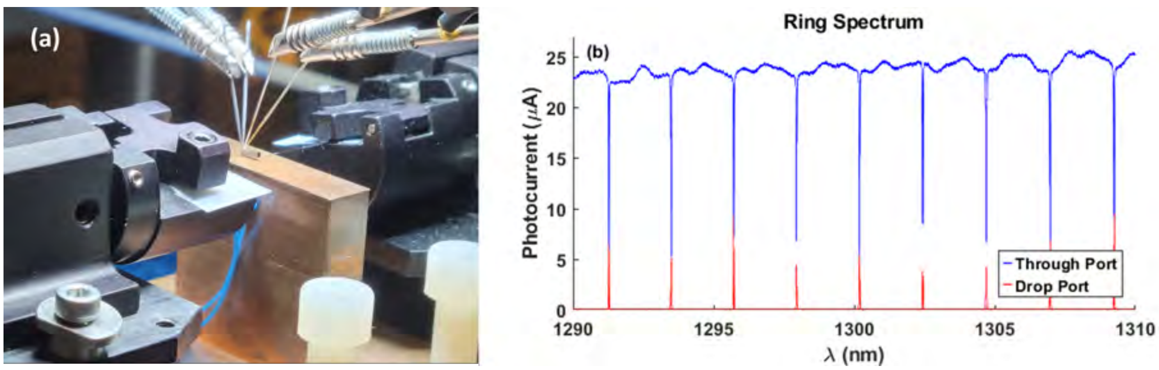

Figure 5.12: Experimental setup for measuring spectra of overlay error ring test structures (a). Resultant wavelength scan example (b).

Figure 5.12.a shows a chip containing the overlay error experiment on the test station. Light is coupled into the chip using a lensed fiber, and the spectra at the through and drop ports is measured electrically with integrated photodiodes that are probed and connected to a commercial photocurrent meter, the EXFO PCM-2; this allows for simultaneous measurement of the drop and through response with only one input fiber, which in turn means that both port measurements experience the same amount of fiber coupling loss due to alignment error and vibrations. It is expected this will reduce errors into fitting to the drop port. To extract the $FWHM$ of the resonances, each through and drop port resonance shape is fit to using the rate equation model with peak splitting [16].

$$\frac{\partial A_{CW}}{\partial t} = \left(j\omega_0 - \frac{1}{\tau_p}\right) A_{CW} - j\mu_{BS} A_{CCW} - j\mu_1 E_{In} \qquad (5.3.a)$$

$$\frac{\partial A_{CCW}}{\partial t} = \left(j\omega_0 - \frac{1}{\tau_p}\right) A_{CCW} - j\mu_{BS} A_{CW} \tag{5.3.b}$$

$$E_{Through} = E_{In} - j\mu_1 A_{CW} \tag{5.3.c}$$

$$E_{Drop} = -j\mu_2 A_{CW} \tag{5.3.d}$$

In the above equations, A_{CW} and A_{CCW} are proportional to the clockwise and counterclockwise propagating field amplitudes inside the cavity, and μ_{BS} is the mutual coupling rate between the clockwise and counterclockwise modes. This model assumes that the amplitudes of the split peaks will be the same, which is sufficient for this application; additional terms could be included to capture the asymmetry in the split peaks (typically attributed to backcoupling) [16]. It is suspected from the travelling wave model that $\psi_a \neq \frac{1}{2}$ would also cause peak asymmetry. An example of a fit to a split peak resonance is shown in Figure 5.13. While the coefficient of determination is quite good at 0.996, it is likely that the fluctuations in the passband (seen in Figure 5.12.b) are introducing error into the fit that will be propagated into the extracted loss terms.

To estimate losses, the finesse extracted from the split peak rate equation fitting will be input into the travelling wave model:

$$\left(\left(|\sigma|^2 a\right)^2 + 1\right) \cos\left(\frac{\pi}{\mathcal{F}}\right) - 2\,|\sigma|^2 a = 0 \tag{5.4}$$

Solving for $|\sigma|^2 a = \aleph$ yields:

$$\aleph = \frac{1 - \sin\left(\frac{\pi}{\mathcal{F}}\right)}{cos\left(\frac{\pi}{\mathcal{F}}\right)} \tag{5.5}$$

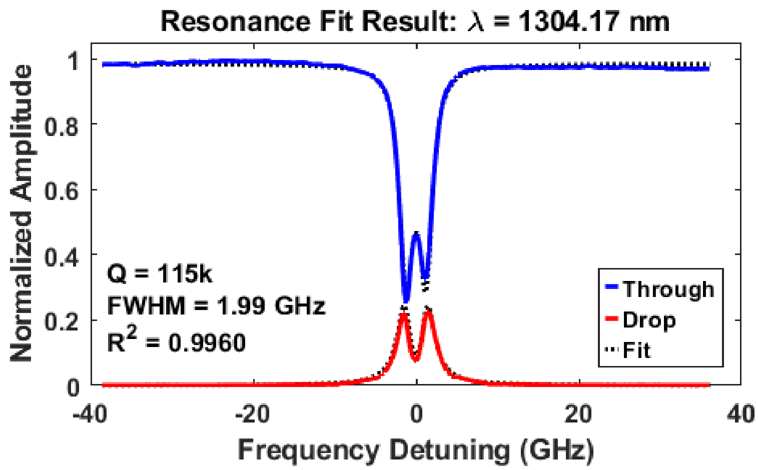

Figure 5.13: Fitting to the measured through and drop port with a split peak resonance.

A polynomial equation in terms of $|\sigma|$ can then be formed from the extinction ratio of the drop port .

$$ER_{DropMax} = \frac{P_{Drop}(\phi = 0)}{P_{Through}(\phi = \pi)} = \frac{\left(1 - |\sigma|^2\right)^2 \left(\frac{\aleph}{|\sigma|^2}\right)^{2\psi_a}}{(1-\aleph)^2} \frac{(1+\aleph)^2}{\left(\frac{\aleph}{|\sigma|} + |\sigma|\right)^2}$$

$$\Longrightarrow \quad |\sigma|^2 + \frac{\sqrt{ER_{DropMax}}\,(1-\aleph)}{(1+\aleph)} \left(\aleph^{1-\psi_a} |\sigma|^{2\psi_a - 1} + \frac{|\sigma|^{1+2\psi_a}}{\aleph^{\psi_a}}\right) - 1 = 0 \quad (5.6)$$

While most values of ψ_a require numerical methods to find the zeros of the function, there exists an easily-acquirable solution for the standard case.

$$|\sigma|_{\psi_a = \frac{1}{2}} = \frac{\sqrt{1 - \frac{(1-\aleph)}{(1+\aleph)} \sqrt{\aleph ER_{DropMax}}}}{\sqrt{1 + \frac{(1-\aleph)}{(1+\aleph)} \sqrt{\frac{ER_{DropMax}}{\aleph}}}} \quad (5.7)$$

While an exact solution for specific value of ψ_a, it does not provide much insight into the degree of sensitivity to ψ_a on the extracted coefficients. This insight can be gained by assuming that $\frac{P_{Through}(\phi=\pi)}{P_{In}} \approx 1$.

$$ER_{DropMax} \approx \frac{P_{Drop}(\phi = 0)}{P_{In}} = \frac{|\kappa|^4 a^{2\psi_a}}{\left(1 - |\sigma|^2 a\right)^2} = \frac{\left(1 - |\sigma|^2\right)^2 \left(\frac{\aleph}{|\sigma|^2}\right)^{2\psi_a}}{(1 - \aleph)^2}$$
$$\implies |\sigma|^2 + \frac{\sqrt{ER_{DropMax}}\,(1 - \aleph)}{\aleph^{\psi_a}} |\sigma|^{2\psi_a} - 1 = |\sigma|^2 + M\,|\sigma|^{2\psi_a} - 1 = 0 \quad (5.8)$$

There are three easily-acquirable solutions for the standard case of ψ_a and its two extremes.

$$|\sigma|_{\psi_a = \frac{1}{2}} \approx \frac{\sqrt{M^2 + 4} - M}{2}\,; \qquad M \geq 0 \quad (5.9.a)$$

$$|\sigma|_{\psi_a = 1} \approx \frac{1}{\sqrt{M + 1}}\,; \qquad M \geq 0 \quad (5.9.b)$$

$$|\sigma|_{\psi_a = 0} \approx \sqrt{1 - M}\,; \qquad 0 \leq M \leq 1 \quad (5.9.c)$$

Figure 5.14.a shows how $|\sigma|$ extracted can vary strongly for the same value of M if ψ_a is not correct. In the context of an overlay error experiment, increasingly more error from the fit occurs if the ψ_a value isn't dialed in for each ring, distorting the extracted logistic function. However, with knowledge of the ring round trip losses without the loss perturbations from the implants, this loss extraction technique can be iteratively solved to refine ψ_a and $\alpha_{Implant}(s)$. The urgency of this iterative procedure depends on the value of $|\sigma|$ extracted, as shown in Figure 5.14.b. Much less error is introduced for small coupling coefficients. In the particular rings measured in this experiment $|\sigma_{Extracted}| \approx 0.994$ for all devices, so Figure 5.14.b suggests the amount of error introduced is negligible for these devices and this iterative refinement procedure can be ignored.

Figure 5.15 shows the extracted loss curves in all 4 coordinate directions for the mea-

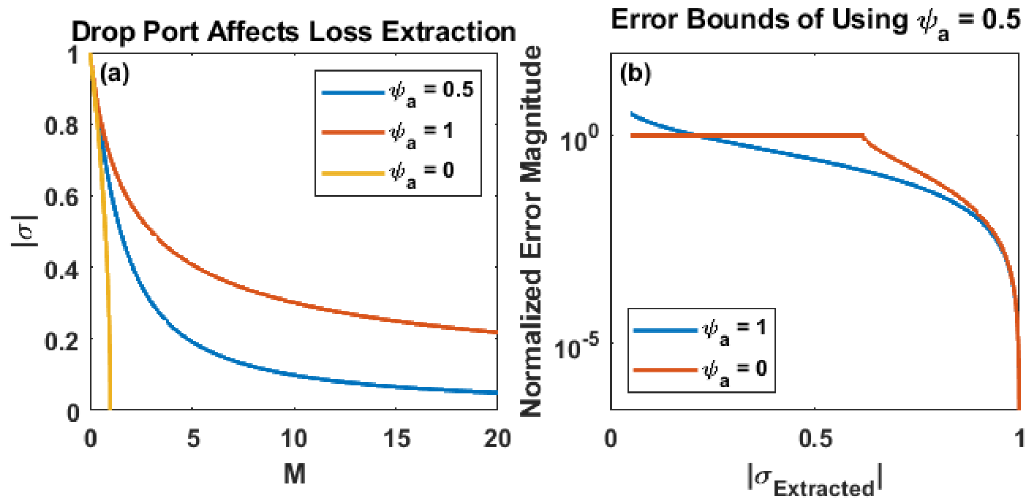

Figure 5.14: Depiction of how the extracted $|\sigma|$ can vary for an input M given an assumption of ψ_a (a). Reframing this in terms of the maximum expected error in $|\sigma|$ extracted from the fitting when assuming $\psi_a = \frac{1}{2}$ (b).

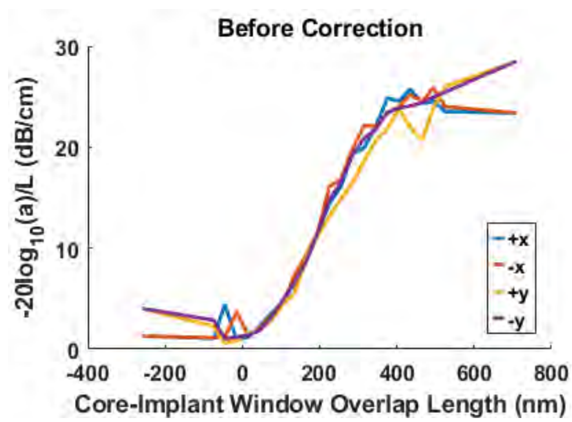

Figure 5.15: Extracted losses of a series of 84 ring resonators with ion implantation windows stepped over the core in a series without an overlay error correction applied.

sured chip; since no trustworthy curve alignment method is available for an unknown implant tilt angle, no attempt to correct for any potential overlay errors is performed. The expected logistic function shape to the curves is readily apparent but slightly distorted from measurement and computational nonidealities. The 4 curves are strongly overlapping without any correction; if it was known that there was no tilt angle to the ion implantation, this would be indicative of a highly precise alignment between the ion implant and waveguide mask layers in this sample. Further examination of all test structure die in the wafer would be needed to produce a distribution to verify the distribution of overlay error in this process.

5.3 Inter-Waveguide, Waveguide Shallow Etch, and Degenerate Doping Overlay Errors

While the large degree of index perturbation a high concentration dopant introduces could be seen as a detracting aspect for extracting the loss of a ring, it opens up an additional way to use rings as an overlay error sensing structure. As has been established previously, resonance peak splitting occurs when there is backscatter inside the cavity to excite both the clockwise and counterclockwise modes of the cavity. The frequency separation between the split peaks is proportional to the backscatter rate. Introducing a reflection into the cavity from an effective index perturbation should induce backscatter, and larger index perturbations should induce larger magnitude reflections which in turn should have a higher backscatter rate and split resonance peaks with a greater degree of separation. Therefore, it could be possible to estimate overlay error from the resultant split peak separation as a perturbing particle is swept across the waveguide. This reflection could come from a strong enough index perturbation introduced by ion implantation, an etching of the waveguide, or a second waveguide layer. Confounding variables would be variations in peak splitting due to variations in background backscatter and backcoupling rates [16, 17].

Figure 5.16 shows how a silicon waveguide's effective index is perturbed by a silicon nitride particle of various widths placed above it. Some observations gained from this figure is that the index perturbation profile is symmetric (assuming symmetry in the etch

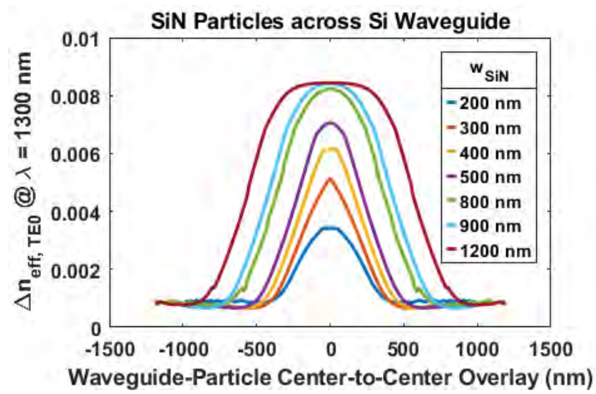

Figure 5.16: Plot of effective index perturbation of a 310-nm wide, 220-nm thick rectangular Si waveguide on 2 μm-thick buried oxide as a 220-nm thick silicon nitride particle of various widths is placed at different locations relative to the silicon waveguide core center. The vertical separation between the two material layers is 200 nm.

profiles of each waveguide element), and that increasing the particle size increases the magnitude of the perturbation with diminishing returns. It is suspected that narrowing the waveguide core would be another means to increase the degree of perturbation. It is also possible that a larger perturbation would be experienced if the particle were in silicon perturbing a nitride waveguide or if the perturbation to the silicon waveguide was an etch of the waveguide. Such an experiment was designed and laid out for the AIM Photonics Lincoln MPW run; in it, a series rectangular waveguide silicon ring resonators are perturbed by a "particle" of 110 nm shallow waveguide etch that has its placement stepped across the core of each ring so that the peak splitting as a function of particle placement can be quantified. The offset in maximum peak splitting compared to the expected location of that curve would be equal to the degree of overlay error. Validation of this hypothesis will be postponed to a later date after the backend processing of these samples is completed to allow for testing.

Much like the loss extraction and alignment technique, it is expected that a tilted ion implantation beam (or asymmetric perturbing particles more generally) will obfuscate the findings of this method until an appropriate analysis technique is established.

5.4 Rotational Overlay Error Estimation

If there were a rotational error $\Delta\theta$ present in the overlay of a mask, the extracted Δx and Δy values would be nonuniform across the reticle without much perceptible twisting between the mask layers; in other words, the Cartesian overlay error measured in that region of the mask would not necessarily be the translational overlay error that the center of rotation of the mask (located at coordinates $[x_0, y_0]$) encountered (Δx_0 and Δy_0).

$$\begin{aligned}\Delta x(x,y) &= \Delta x_0 + \sqrt{(x-x_0)^2+(y-y_0)^2} \\ &\qquad \left[\cos\left(\tan^{-1}\left(\frac{y-y_0}{x-x_0}\right)\right) - \cos\left(\tan^{-1}\left(\frac{y-y_0}{x-x_0}\right) - \Delta\theta\right)\right] \\ &= \Delta x_0 - 2\sqrt{(x-x_0)^2+(y-y_0)^2}\left[\sin\left(\frac{\Delta\theta}{2}\right)\sin\left(\tan^{-1}\left(\frac{y-y_0}{x-x_0}\right) - \frac{\Delta\theta}{2}\right)\right] \\ &= \Delta x_0 - \Delta R \sin\left(\theta - \frac{\Delta\theta}{2}\right) \qquad (5.10.a)\end{aligned}$$

$$\Delta y(x,y) = \Delta y_0 + \Delta R \cos\left(\theta - \frac{\Delta\theta}{2}\right) \qquad (5.10.b)$$

Three insights can be drawn from these equations. Firstly, putting an overlay experiment near the center of the mask will reduce the impact that rotational overlay error has on the result; for instance, an overlay experiment placed in the top right corner of a 20 mm x 20 mm reticle would experience a pertubation in the extracted overlay error of about 7 nm in both dimensions compared to the center of rotation for a rotational error of 1 microradian if the center of rotation during that exposure was the perfect center of the mask. Secondly, by placing the same overlay error experiment at 3 distant points in the reticle (such as 3 of the corners of the reticle), triangulation can be performed to find the center of rotation of the mask, the rotational overlay error, and the true translational overlay errors of the mask. Finally, this allows for computing the overlay error field across the entire reticle once all the relevant parameters have been extracted; this allows for even more precise parameter extraction and modelling of devices.

5.5 Impact on Depletion p-n Ring Resonators

Forming a p-n junction phase shifter usually involves at least 4 ion implantation steps: 2 for Ohmic contacts and 2 for forming the junction [18]. Each individual implantation layer will have its own overlay error associated with it. As shown in Figure 5.17, a perfectly circular geometry of radius $\mathcal{R}$ with a small overlay error can be reimagined as a shape still centered at the intended placement but with a rotationally-dependent radius $\mathcal{R}_{eff}(\theta)$

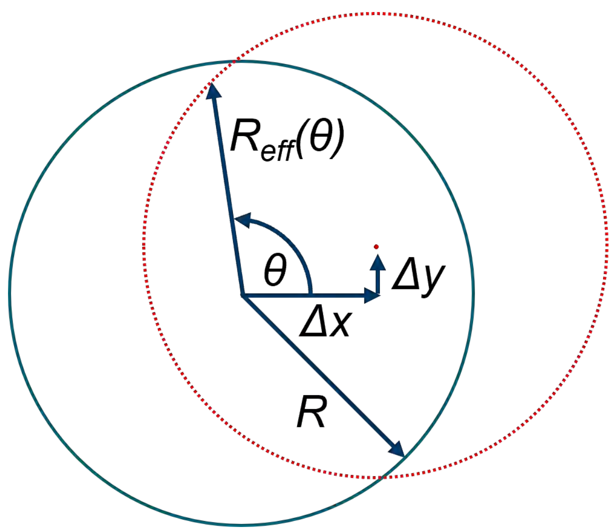

Figure 5.17: Sketch of envisioning an overlay error of a circle as a rotational perturbation of its radius.

$$\mathcal{R}_{eff}(\theta) = \mathcal{R} + \sqrt{\Delta x^2 + \Delta y^2}\sin\left(\theta + \tan^{-1}\left(\frac{\Delta y}{\Delta x}\right)\right) = \mathcal{R} + \Delta\mathcal{R}\sin\left(\theta + \delta\theta\right) \quad (5.11)$$

The above expression could also be leveraged for more advanced ring geometries, such as racetrack resonators or adiabatic bends like Euler bends instead of circular bends, by making $\mathcal{R}_0$ a function of θ. This reframing of the overlay error as a geometric distortion allows for simpler computation and simulation of phase shifter characteristics. Instead of needing a full 3D simulation to capture the impact of overlay error, several 2-D simulations can be conducted (or analytical expressions of 2D cross sections) and interpolated between to set up a path integral of the cavity. Two important parameters related to the strength of the FCPDE that can be described through the effective radius technique are the intrinsic gap w_i of the p-n junction and the offset between the center of the junction and the center of the waveguide core x_{Offset}. These two values are formed by the placement of the two implant layers that form the junction with radii $\mathcal{R}_{In}$ and $\mathcal{R}_{Out}$; the center of the waveguide core is at $\mathcal{R}_{Center}$ and is assumed to not impacted by overlay error.

$$w_i(\theta) = w_{i_0} + \mathit{\Delta} w_i \sin\left(\theta + \delta\theta_{w_i}\right) \tag{5.12.a}$$

$$w_{i_0} = \mathcal{R}_{Out_0} - \mathcal{R}_{In_0} \tag{5.12.b}$$

$$\mathit{\Delta} w_i = \sqrt{\mathit{\Delta}\mathcal{R}_{Out}^2 + \mathit{\Delta}\mathcal{R}_{In}^2 - 2\mathit{\Delta}\mathcal{R}_{Out}\mathit{\Delta}\mathcal{R}_{In}\cos\left(\delta\theta_{R_{Out}} - \delta\theta_{R_{In}}\right)} \tag{5.12.c}$$

$$\delta\theta_{w_i} = \tan^{-1}\left(\frac{\mathit{\Delta}\mathcal{R}_{Out}\cos(\delta\theta_{R_{Out}}) - \mathit{\Delta}\mathcal{R}_{In}\cos(\delta\theta_{R_{In}})}{\mathit{\Delta}\mathcal{R}_{Out}\sin(\delta\theta_{R_{Out}}) - \mathit{\Delta}\mathcal{R}_{In}\sin(\delta\theta_{R_{In}})}\right) \tag{5.12.d}$$

$$x_{Offset}(\theta) = x_{Offset_0} + \mathit{\Delta} x_{Offset}\sin\left(\theta + \delta\theta_{x_{Offset}}\right) \tag{5.12.e}$$

$$x_{Offset_0} = \mathcal{R}_{Out_0} - \mathcal{R}_{Center} - \frac{w_{i_0}}{2}; \tag{5.12.f}$$

$$\Delta x_{Offset} = \sqrt{\Delta\mathcal{R}_{Out}^2 + \frac{\Delta w_i^2}{4} - \Delta\mathcal{R}_{Out}\Delta w_i \cos\left(\delta\theta_{R_{Out}} - \delta\theta_{w_i}\right)} \tag{5.12.g}$$

$$\delta\theta_{x_{Offset}} = \tan^{-1}\left(\frac{\Delta\mathcal{R}_{Out}\cos(\delta\theta_{R_{Out}}) - \frac{\Delta w_i}{2}\cos(\delta\theta_{w_i})}{\Delta\mathcal{R}_{Out}\sin(\delta\theta_{R_{Out}}) - \frac{\Delta w_i}{2}\sin(\delta\theta_{w_i})}\right) \tag{5.12.h}$$

The result of these expressions for a particular set of radii and overlay error values is plotted in Figure 5.18. Negative values of w_i lead to charge compensation, which adds complications to the analysis that must consider the concentrations of implanted doping fields [19, 20].

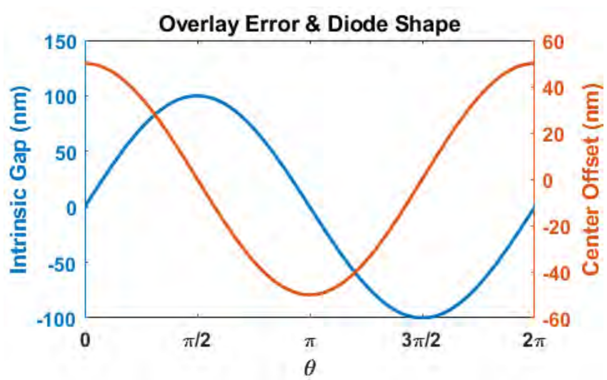

Figure 5.18: Plot of intrinsic gap width and junction-core offset for a circular p-n junction phase shifter with perfectly horizontal charge depletion for which $\mathcal{R}_{Out_0} = \mathcal{R}_{In_0} = \mathcal{R}_{Center}$, $\Delta x_{Out} = \Delta y_{Out} = \Delta x_{In} = 50$ nm, and $\Delta y_{In} = -50$ nm.

Overall, a simple way to mitigate these impacts is to displace charge vertically instead of horizontally [21].

5.6 Conclusion

This chapter has outlined several successful and attempted techniques for extracting lithographic overlay error between critical layers in silicon photonics platforms using relatively simple and nondestructive measurement techniques. These techniques have the capability to describe the statistics of both the lithography machine and some details about the processing tool that was utilized after masking. This opens up avenues for chip designers to have a more complete description of the tolerances they must design within to maximize device and system performance. Knowledge of the availability of these experiments could also encourage a greater degree of transparency on the part of foundries regarding critical parameters that are, as this chapter shows, impossible to be kept entirely secret anyway.

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Chapter 6

Summary and Future Work

This dissertation presents innovations in compact, energy-efficient short-reach transceiver architectures, along with outlines for optimizing subcomponent designs for such a system and proposing a new method of analyzing a less-explored dimension of variability in integrated photonics.

6.1 Future Work

There are many avenues through which future work can be conducted. For starters, realizing the proposed athermal and fabrication tolerant deinterleaver designs in practice would be an important step in reducing the need for static-power heaters in integrated photonic systems. On the other end of the spectrum of this compensation technique lies another interesting device that remains unexplored: the broadband, fab stable, MZI-based photonic thermometer. Most integrated photonic thermometers operate by observing the thermal drift of a ring resonance or an interference dip in a uMZI and therefore either require a particular and stable wavelength for correct fixed-wavelength operation or wavelength scans to detect peak drift. If an MZI could be made with full fabrication dimension phase compensation with no group length difference between the two paths and unequal thermal phase drifts between the paths (perhaps out of silicon and silicon nitride), there would be spectrally broadband temperature-dependent output responses of the MZI; this means the thermometer could be read with a fixed wavelength where the input wavelength does not need to be very precise or stable for an accurate temperature reading, and the performance between devices should be similar at wafer-scale (all making it very cheap to deploy compared to other methods).

In terms of work for the theory of ring resonators, building on the dynamic travelling wave ring models to capture phenomena like power handling, crosstalk, and bidirectional propagation would be of value. Additionally, there is plenty of work to be done in producing ring designs capable of the expected RF and DC electro-optic charactertics for such power stringent systems.

The most immediate task for the system would be to resolve the issues in system assembly and packaging to facilitate a practical link experiment, as there's plenty of more undiscovered kinks to work out between the current state of the system and a fully-operational one. In a more general sense, any innovations in improving insertion loss, thermal stability, fabrication tolerances, and footprint of the PIC (at either a system or subcomponent level) will lead to a more capable system; the improvements could be gained from modifying the fabrication process of the silicon photonics foundry offering or iterating on device design to optimize performance. Some ideas otherwise not presented throughout the dissertation that would be interesting to pursue are:

- Developing thermal models of the fully-assembled system as well as comprehensive electrical and optical system simulations.
- Increasing overall PIC capacity by treating the 1 Tbps PIC as a unit cell that is tiled multiple times on one chip would likely lead to a smaller overall system

because some components in the system would be made redundant; this may result in bonding several driver ICs to one PIC to reduce overhead costs on electronic ICs. The ability to increase capacity of an individual PIC will likely be limited by a maximum port count on the fiber array. It is currently advised to limit fiber array channel count to at most 64.

- Instead of encoding the optical clock waveform with a variable optical attenuator, it would probably be more compact and lower loss to do so with a push-pull dual-drive Mach-Zehnder modulator configuration.
- Utilizing many QD-MLL comb sources with different comb center frequencies to achieve a sort of coarse-dense WDM and adding a band interleaving stage(s). This would increase the amount of capacity per fiber and reduce port count.
- Integrating bandpass filters to remove the unwanted parasitic QD-MLL comb lines.
- The odd-even interleavers on the TX and the odd-even deinterleavers on the RX could be replaced with polarization splitter-rotator elements to use polarization multiplexing as a psuedo-interleaver. This doubles the amount of ports between the TX and RX (negatively impacting shorline density) at the benefit of making the PIC more compact (improving area density).

There is still more work to do with sorting out the issues with extracting overlay error of ion implantation layers with a tilted beam/asymmetric perturbations and developing estimates on the technique's overall precision due to fluctuations in waveguide dimensions and measurement noise. In terms of making the experiment more compact, there is also likely work that can be done in optimizing the points of the logistic function to sample to improve the quality of a fit with fewer sampling points.